TUSB1211 Stand-Alone USB Transceiver Chip

1 Device Overview

1.1 Features

- USB2.0 PHY Transceiver Chip, Designed to Interface With a USB Controller Through a ULPI Interface, Fully Compliant With:
  - *Universal Serial Bus Specification* Rev. 2.0
  - *On-The-Go Supplement to the USB 2.0 Specification* Rev. 1.3
  - *UTMI+ Low Pin Interface (ULPI) Specification* Rev. 1.1
- DP/DM Line External Component Compensation (Patent #US7965100 B1)
- Interfaces to Host, Peripheral, and OTG Device Cores; Optimized for Portable Devices or System ASICs With Built-in USB OTG Device Core
- Complete USB OTG Physical Front-End
- USB Battery Charger Detection Feature
- USB HS Start-of-Frame Clock Output Feature Available on SOF Pin Can be Used to Synchronize Another Application, for Example Audio, With the USB Packet Stream
- ULPI Interface:
  - I/O Interface (1.8 V) Optimized for Non-Terminated 50-Ω Line Impedance
  - ULPI CLOCK Pin (60 MHz) Supports Both Input and Output Clock Configurations
  - Fully Programmable ULPI-Compliant Register Set
- Full Industrial-Grade Operating Temperature Range from –40°C to 85°C
- Available in a TFBGA36 Ball Package

1.2 Applications

- Mobile Phones
- Portable Computers
- Tablet Devices
- Video Game Consoles
- Desktop Computers
- Portable Music Payers

1.3 Description

The TUSB1211 device is a USB2.0 transceiver chip, designed to interface with a USB controller through a ULPI interface. The device supports all USB2.0 data rates (high-speed 480 Mbps, full-speed 12 Mbps and low-speed 1.5 Mbps), and is compliant to both Host and Peripheral modes. The TUSB1211 also supports a UART mode and legacy ULPI serial modes.

The TUSB1211 device supports the OTG (Ver1.3) optional addendum to the USB 2.0 Specification, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). TUSB1211 also supports USB Battery Charging Specification Ver1.1 integrating a charger detection module for sensing and control on DP/DM lines, and ACA (Accessory Charger Adapter) detection and control on ID line.

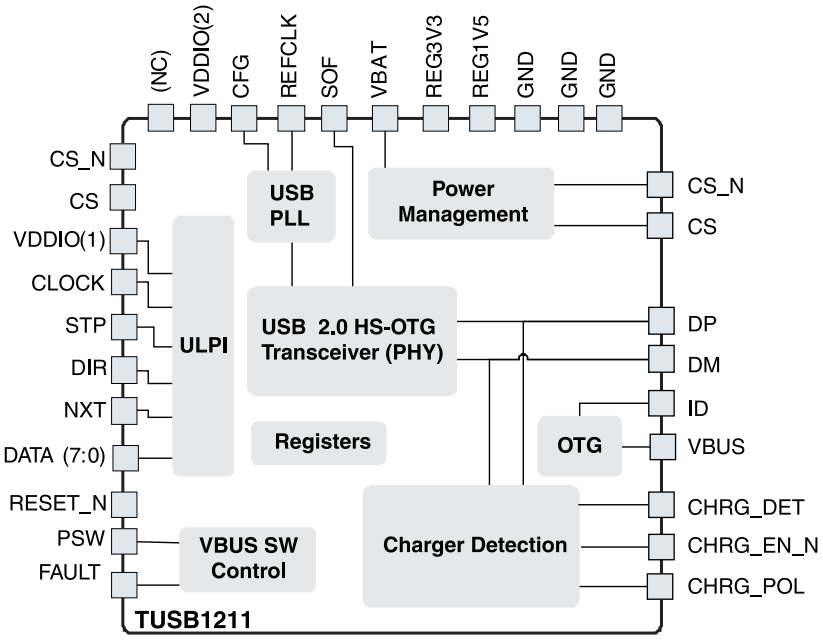
The DP/DM external component compensation in the transmitter compensates for variations in the series impendence to match with the data line impedance and the receiver input impedance, to limit data reflections and, thereby, improve eye diagrams.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB1211	BGA MICROSTAR JUNIOR (36)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1.4 Functional Block Diagram



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2 Revision History

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• Deleted some of the features per the submitted sources	1
• Changed the document to the new TI standard layout	1
• Changed pin F5 from A to D in the A/D column	6
• Added the Analog Output Pins section	9
• Added the word Non to the tile Non-ULPI Pins and replaced the *Digital I/O Electrical Characteristics – Non-ULPI Pins* table data	10
• Added the Timers and Debounce section	13
• Added the OTG VBUS *Specifications*	14
• Added the *Pullup and Pulldown Resistors* table	17
• Added Section 4.26	17
• Added the *OTG ID Electrical* table	17
• Added the *ULPI Interface* section	20
• Added the *Power-On Timing Diagrams* section	20
• Added the Internal Clock Generator (32 kHz)	23
• Added the Power Provider section	24
• Changed the location of paragraphs from *Description* to *Detailed Description*, subsection *Overview*	26
• Added the LS/FS Single-Ended Receivers section	28
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• Added the Autoresume section	29
• Added the Register Map section	32
• Added the *Application and Implementation* section	70
• Deleted two List Items from the *Unused Pins Connection* section	71
• Added the *Layout* section	72
• Added the *Power Supply Recommendations* section	73

3 Pin Configuration and Functions

3.1 Pin Diagram

ZRQ Package
36-Pin TFBGA
Bottom View

TFBGA36 PACKAGE
(BOTTOM VIEW)

	1	2	3	4	5	6
F	CHRG_ POL	CHRG_ DET	VBAT	VBUS	REFCLK	SOF
E	CHRG_ EN_N	FAULT	REG3V3	GND	DIR	REG1V5
D	DP	GND	ID	PSW	NXT	STP
C	DM	NC(1)	CS_N	RESET_N	GND	DATA7
B	DATA0	VDDIO	CS	CFG	VDDIO	DATA6
A	DATA1	DATA2	DATA3	CLOCK	DATA4	DATA5

(1) NC = Not Connected

(2) The size of the device should be 3.5 mm ±0.1 mm by 3.5 mm ±0.1 mm. Height is 1.0 mm typical 1.15 mm max including the solder balls. The pitch of the device is 0.5 mm. Ball width 0.3 mm ±0.05 mm.

3.1.1 Pin Attributes

Pin Functions

NO.	PIN(1)	NAME	A/D(2)	TYPE(3)	LEVEL(4)	DESCRIPTION
1	D5	NXT	D	O	V_{DDIO}	ULPI NXT output signal
2	B1	DATA0	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
3	A1	DATA1	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
4	A2	DATA2	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
5	A3	DATA3	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
6	A5	DATA4	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
7	A6	DATA5	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
8	B6	DATA6	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
9	B3	CS	D	I	V_{DDIO}	Active-high chip select pin. When low the IC is in power down and ULPI bus is tri-stated. When high (and CS_N pin iTie to VDDIO if unused.s low) normal operation.
10	E6	REG1V5	A	POWER	V_{DD15}	1.5 V internal LDO output. Connect to external filtering capacitor.
11	C6	DATA7	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK

(1) Pin = Package Pin coordinate of
(2) A/D: A = Analog pin, D = Digital pin
(3) TYPE: I = Input pin type, O = Output pin type, I/O = Input/Output pin type, POWER = Power supply pin type, GROUND = Ground type pin
(4) LEVEL = Pin power supply level

Pin Functions (continued)

NO.	PIN(1)	NAME	A/D(2)	TYPE(3)	LEVEL(4)	DESCRIPTION
12	B4	CFG	D	I	V_{DDIO}	REFCLK clock frequency configuration pin. Two frequencies are supported: 19.2 MHz when 0, or 26 MHz when 1.
13	D1	DP	A	I/O	V_{DD33}	DP pin of the USB connector
14	C1	DM	A	I/O	V_{DD33}	DM pin of the USB connector
15	E3	REG3V3	A	POWER	V_{DD33}	3.3 V internal LDO output. Connect to external filtering capacitor.
16	F3	VBAT	A	POWER	V_{BAT}	Input supply voltage or battery source. Nominally 3.3 V to 4.5 V
17	F4	VBUS	A	I/O	V_{BUS}	VBUS pin of the USB connector
18	D3	ID	A	I/O	V_{BUS}	Identification (ID) pin of the USB connector
19	A4	CLOCK	D	I/O	V_{DDIO}	ULPI 60-MHz clock on which ULPI data is synchronized. 2 modes are possible: Input Mode: CLOCK defaults as an input (this is the default clock mode) Output Mode: When an input clock is detected on REFCLK pin then CLOCK will change to an output
20	C4	RESET_N	D	I	V_{DDIO}	Active low chip reset pin. Minimum pulse width 100 µs. When low all digital logic (except 32-kHz logic required for power-up sequencing and charger detection state-machine) including registers are reset to their default values. ULPI bus is in “ULPI Synchronous mode power-up PLL OFF” state as described in Table 5-5. When high normal USB operation.
21	D6	STP	D	I	V_{DDIO}	ULPI STP input signal
22	E5	DIR	D	O	V_{DDIO}	ULPI DIR output signal
23	B5	VDDIO	A	I	V_{DDIO}	External 1.8-V supply input for digital I/Os. Connect to external filtering capacitor.
24	B2	VDDIO	A	I	V_{DDIO}	External 1.8-V supply input for digital I/Os. Connect to external filtering capacitor.
25	C5	GND	A	GROUND	GND	Ground
26	D2	GND	A	GROUND	GND	Ground
27	E4	GND	A	GROUND	GND	Ground
28	F5	REFCLK	D	I	V_{DDIO}	Reference clock input. Input reference clock frequency must be indicated by CFG pin. Two frequencies are supported: 19.2 MHz (when CFG = 0), and 26 MHz (when CFG = 1).
29	F6	SOF	D	O	V_{DDIO}	HS USB SOF (Start-of-Frame) output clock. (feature controlled by SOF_EN bit, disabled and output logic low by default.). HS USB SOF packet rate is 8 kHz.
30	C2	NC	—	—		Not connected
31	C3	CS_N	D	I	V_{DDIO}	Active-low chip select pin. When high the IC is in power down and ULPI bus is tri-stated. When low (and CS pin is high) normal operation. Tie to GND if unused.
32	E1	CHRG_EN_N	D	I	V_{BAT}	Active low input pin used to enable Battery Charging Detection in Dead Battery Charger Detection mode. This pin is ignored in ACTIVE mode. Connect to GND to activate. Connect to VBAT when charger detection not required.
33	E2	FAULT	D	I	V_{BAT}	VBUS fault detector input used as EXTERNALVBUSINDICATOR in TUSB1211. The link must enable VBUS fault detection through the USEEXTERNALVBUSINDICATOR register bit, and the polarity must be set through the INDICATORCOMPLEMENT register bit. INDICATORPASSTHRU bit can be used to qualify FAULT with the internal vbusvalid comparator. Connect to GND if not used. This pin is 5-V tolerant.
34	F1	CHRG_POL	D	I	V_{BAT}	When connected to GND then CHRG_DET output pin is active low. When connected to VBAT then CHRG_DET output pin is active high.

Pin Functions (continued)

NO.	PIN(1)	NAME	A/D(2)	TYPE(3)	LEVEL(4)	DESCRIPTION
35	F2	CHRG_DET	D	O	V_{BAT}	When CHRG_POL pin is at GND then CHRG_DET is in active low open-drain mode with external RCHRGDET (100K) connected to VBAT. When CHRG_POL pin is at VBAT then CHRG_DET is in active high open-source mode with external RCHRGDET (100K) connected to GND. This pin is 5-V tolerant.
36	D4	PSW	D	O	V_{BAT}	Controls an external, active high, VBUS power switch or charge pump. Open source output on VBAT supply when PSW_OSOD bit is 0 (default), open-drain active-low output when PSW_OSOD bit is 1. Requires an external RPSW (100K) pulldown/pullup resistor to GND/VBAT.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{BAT}(2)	Main battery supply voltage	Continuous	0	5.0	V
	Main battery supply voltage pulsed	The product will have negligible reliability impact for pulsed voltage spikes of 5.5 V for a total (cumulative over lifetime) duration of 5 milliseconds		5.5	V
V_{DDIO}	IO supply voltage	Continuous		1.98	V
	Voltage on any input except V_{DDIO}, V_{BAT}, and V_{BUS} pads	Where V_{DD} represents the voltage applied to the power supply pin associated with the input	–0.3	1.0 × V_{DD} + 0.3	V
	DP, DM, ID high voltage short circuit	DP or DM or ID pins short-circuited to VBUS supply, in any mode of TUSB1211 operation, continuously for 24 hours		5.25	V
	DP, DM, ID low voltage short circuit	DP or DM or ID pins short-circuited to GND in any mode of TUSB1211 operation, continuously for 24 hours	0		V
	V_{BUS} input(3)		–2	20	V
T_A	Ambient temperature		–40	85	°C
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 4.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If VBAT exceeds above rating a device to drop down the voltage before applied to the device.
(3) If VBUS exceeds above rating an external voltage protection on the line is mandatory between the VBUS line and the TUSB1211.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{BAT}	Battery supply voltage	VBAT_ACTIVE	2.7	3.6	4.8	V
V_{BAT_CERT}	Battery supply voltage for USB 2.0 compliancy (USB 2.0 certification)	When V_{DD33} is supplied internally	3.15			V
		When V_{DD33} is shorted to V_{BAT} externally	3.05			
V_{BAT_DB}	Battery supply voltage for charger detect in “dead-battery condition”	VBAT_DB	2.4			V
V_{DDIO}	IO supply voltage	VDDIO_ACTIVE	1.62	1.8	1.95	V
T_A	Ambient temperature range		–40		85	°C
T_J	Junction temperature	For parametric compliance	–40		125	°C

4.4 Power Consumption Summary(1)(2)

MODE	CONDITIONS	SUPPLY	TYPICAL POWER CONSUMPTION	UNIT
OFF	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, CS = 0 V	IV_{BAT}	8	µA
		IV_{DDIO}	1.8	
		I_{TOTAL}	**9.8**	
Suspend	V_{BUS} = 5 V, V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, VCHRG_EN_N = 0 V, no clock	IV_{BAT}	251	µA
		IV_{DDIO}	21	
		I_{TOTAL}	**272**	
HS USB Mode	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, active USB transfer	IV_{BAT}	46.4	mA
		IV_{DDIO}	1.3	
		I_{TOTAL}	**47.7**	
FS USB Mode	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, active USB transfer	IV_{BAT}	31.4	mA
		IV_{DDIO}	1.3	
		I_{TOTAL}	**32.7**	

(1) Describes the power consumption depending on the use cases.
(2) Typical power consumption is obtained in nominal operating conditions of the TUSB1211 device.

4.5 Electrical Characteristics – Analog Output Pins

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHRG_DET OUTPUT PIN						
$R_{CDETPUOD}$	CHRG_DET external pullup resistor to VBAT	When CHRG_POL pin = GND, that is, in open-drain mode (active-low)	60	100		kΩ
VOH_{CDETOD}	CHRG_DET minimum high-level output voltage	When CHRG_POL pin = GND, that is, in open-drain mode (active-low)	0.7 × V_{BAT}			V
IOH_{CDETOD}	CHRG_DET maximum current from VBAT	When CHRG_POL pin = GND, that is, in open-drain mode (active-low)			2	mA
$R_{CDETPDOS}$	CHRG_DET external pulldown resistor to GND	When CHRG_POL pin = VBAT, that is, in open-source mode (active-high)	60	100		kΩ
VOL_{CDETOS}	CHRG_DET maximum low-level output voltage	When CHRG_POL pin = VBAT, that is, in open-source mode (active-high)			0.3 × V_{BAT}	V
IOH_{CDETOS}	CHRG_DET minimum current from VBAT	When CHRG_POL pin = VBAT, that is, in open-source mode (active-high)	–2			mA
PSW OUTPUT PIN						
$R_{PSWPUOD}$	PSW external pullup resistor to VBAT	When configured in open-drain active low mode	60	100		kΩ
VOH_{PSW}	PSW minimum high-level output voltage	When configured in open-drain active low mode or CMOS mode	0.7 × V_{BAT}			V
IOH_{PSWOD}	PSW maximum current from VBAT	When configured in open-drain active low mode			2	mA
$R_{PSWPDOS}$	PSW external pulldown resistor to ground	When configured in open-source active high mode (default)	60	100		kΩ
VOL_{PSW}	PSW minimum high-level output voltage	When configured in open-source active high mode (default) or CMOS mode			0.3 × V_{BAT}	V
IOH_{PSWOS}	PSW maximum current from VBAT	When configured in open-source active high mode (default)	–2			mA

4.6 Electrical Characteristics – Analog Input Pins

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHRG_EN_N INPUT PIN						
VILCDETENN	CHRG_EN_N maximum low-level input voltage				0.3	V
VIHCDETENN	CHRG_EN_N minimum high-level input voltage		1.0			V
CHRG_POL INPUT PIN						
VILCHRG_POL	CHRG_POL maximum low-level input voltage				0.3	V
VIHCHRG_POL	CHRG_POL minimum high-level input voltage		1.0			V
FAULT INPUT PIN						
VILFAULT	FAULT maximum low-level input voltage				0.3	V
VIHFAULT	FAULT minimum high-level input voltage		1.0			V

4.7 Digital I/O Electrical Characteristics – Non-ULPI Pins

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK						
V_{OL}	Low-level input voltage	Frequency = 60 MHz, Load = 10 pF			0.4	V
V_{OH}	High-level input voltage		V_{DDIO} – 0.45			V
STP, DIR, NXT, DATA0 to DATA7						
V_{OL}	Low-level input voltage	Frequency = 360 MHz, Load = 10 pF			0.45	V
V_{OH}	High-level input voltage		V_{DDIO} – 0.45			V

4.8 Digital I/O Electrical Characteristics – Non-ULPI Pins

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CS, CFG, RESETB INPUT PINS						
V_{IL}	Maximum low-level input voltage				0.35 × V_{DDIO}	V
V_{IH}	Minimum high-level input voltage		0.65 × V_{DDIO}			V
RESET_N INPUT PIN TIMING SPECIFICATION						
$t_{w(POR)}$	Internal power-on reset pulse width		0.2			µs
$t_{w(RESET)}$	External RESET_N pulse width	Applied to external RESET_N pin when CLOCK is toggling.	8			CLOCK cycles

4.9 Electrical Characteristics – REFCLK

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
V_{IL}	Low level input voltage				0.35 × V_{DDIO}	V
V_{IH}	High level input voltage		0.65 × V_{DDIO}			V

(1) V_{DDIO} voltage level = 1.8 V

4.10 Electrical Characteristics – CLOCK Input

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK input duty cycle		40%		60%	
F_{CLOCK} CLOCK nominal frequency			60		MHz
CLOCK input rise/fall time	In % of CLOCK period T_{CLOCK} (= $1/F_{CLOCK}$)			10%	
CLOCK input frequency accuracy				250	ppm
CLOCK input integrated jitter				600	ps rms

4.11 Electrical Characteristics – REFCLK

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFCLK input duty cycle		40%		60%	
FREFCLK REFCLK nominal frequency	When CFG pin is tied to GND		19.2		MHz
	When CFG pin is tied to V_{DDIO}		26		
REFCLK input rise/fall time	In % of REFCLK period T_{REFCLK} (= $1/F_{REFCLK}$)			20%	
REFCLK input freq accuracy				250	ppm
REFCLK input integrated jitter				600	ps rms

4.12 Electrical Characteristics – CK32K Clock Generator

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output duty cycle		48%	50%	52%	
Output frequency		23	32.7	38	kHz

4.13 Thermal Characteristics

THERMAL METRIC(1)		TUSB1211 ZRQ (BGA MICROSTAR JUNIOR) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	69.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)(4)	41	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(4)(5)	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance or junction-to-pin thermal resistance(6)	42	°C/W
Ψ_{JT}	Junction-to-top of package (not a true thermal resistance)(7)	0.9	°C/W
Ψ_{JB}	Junction-to-board (not a true thermal resistance)(8)	71	°C/W

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics* (SPRA953).
(2) Measurement method: EIA/JESD 51-1
(3) Top is surface of the package facing away from the PCB.
(4) No current JEDEC specification (see the application report, *Semiconductor and IC Package Thermal Metrics* (SPRA953).
(5) Bottom surface is the surface of the package facing towards the PCB.
(6) Measurement method: EIA/ JESD 51-8
(7) Measurement method: EIA/JESD 51-2
(8) Measurement method: EIA/JESD 51-6

4.14 REG3V3 Internal LDO Regulator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{INREG3V3}$	Input voltage	V_{BAT}	$V_{OUT(typ)}$ + 0.15	3.6	4.8	V
VV_{DD33}	Output voltage ACTIVE mode	On mode – REG3V3_VSEL<2:0> = ‘000	2.4	2.5	2.6	V
		On mode – REG3V3_VSEL<2:0> = ‘001	2.65	2.75	2.85	
		On mode – REG3V3_VSEL<2:0> = ‘010	2.9	3.	3.1	
		On mode – REG3V3_VSEL<2:0> = ‘011 (default)	3	3.1	3.2	
		On mode – REG3V3_VSEL<2:0> = ‘100	3.1	3.2	3.3	
		On mode – REG3V3_VSEL<2:0> = ‘101	3.2	3.3	3.4	
		On mode – REG3V3_VSEL<2:0> = ‘110	3.3	3.4	3.5	
		On mode – REG3V3_VSEL<2:0> = ‘111	3.4	3.5	3.6	
VV_{DD33_DB}	Output voltage hardware charger detection (dead battery) mode	$V_{BAT\_DB} < V_{BAT} < 3.1$ V	V_{BAT} – 0.05	V_{BAT}	$V_{BAT + 0.05}$	V
		$V_{BAT} > 3.1$ V	3	3.1	3.2	
I_{REG3V3}	Rated output current	V_{BAT}: ACTIVE mode, Hardware charger detection (dead battery) mode			15	mA
I_{REG3V3_SUSP}	Rated output current: IREG3V3_SUSP	Suspend mode/reset mode			1	mA

4.15 REG1V8 Internal LDO Regulator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{INREG1V8}$	Input voltage	On mode : $V_{INREG1V8} = V_{BAT}$	2.4	3.6	4.8	V
V_{REG1V8}	Output voltage		1.75	1.87	1.98	V
I_{REG1V8}	Rated output current	On mode			30	mA

4.16 REG1V5 Internal LDO Regulator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{INREG1V8}$	Input voltage	On mode : $V_{INREG1V8} = V_{BAT}$	2.4	3.6	4.8	V
V_{REG1V8}	Output voltage		1.45	1.56	1.65	V
I_{REG1V8}	Rated output current	On mode			50	mA

4.17 Timers and Debounce

over operating free-air temperature range (unless otherwise noted)

PARAMETER		NB CK32K CYCLES	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TDEL_CS_SUPPLYOK	Chip-select-to-Supplies ok delay	N/A			4.19		ms
TDEL_RST_DIR	Resetb to PHY PLL locked and DIR falling-edge delay	N/A			0.42		ms
TVBAT_DET	VBAT detection delay	N/A			10.0		µs
TBGAP	Bandgap power-on delay	N/A			2.0		ms
TPWONREG1V5	REG1V5 power-on delay	N/A			100.0		µs
TPWONREG1V8	REG1V8 power-on delay	N/A			100.0		µs
TPWONVREG3V3	REG3V3 power-on delay	N/A			1.0		ms
TPWONCK32K	32KHz RC-OSC power-on delay	N/A			125.0		µs
TDELRSTPWR	Power control reset delay	2		52.6	61.0	87.0	µs
TDELMNTRVIOEN	Monitor enable delay	3		78.9	91.6	130.4	µs
TMNTR	Supply monitoring debounce	6		157.9	183.1	260.9	µs
TDELREG3V3EN	REG3V3 LDO enable delay	3		78.9	91.6	130.4	µs
TDELRESET_N	RESET_N internal delay	4		105.3	122.1	173.9	µs
TPLL	PLL Lock time	N/A			300.0		µs
TERROR_DELAY	PWR FSM ERROR state delay	Min 4100 Max 8196		107.9	125.1	356.3	ms

4.18 OTG VBUS Electrical

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{BUS} COMPARATORS							
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid	RVBUS = 0 Ω and R1KSERIES = 0		4.4	4.5	4.625	V
		RVBUS = 1000 Ω ±10% and R1KSERIES = 1		4.4	4.5	4.625	
		RVBUS = 1200 Ω ±10% and R1KSERIES = 1		4.4	4.5	4.625	
		RVBUS = 1800 Ω ±10% and R1KSERIES = 1		4.4	4.5	4.675	
V_{SESS_VLD}	A-device session valid			0.8	1.4	2.0	V
$V_{B\_SESS\_VLD}$	B-device session valid			2.1	2.4	2.7	V
$V_{B\_SESS\_END}$	B-device session end			0.2	0.5	0.8	V
V_{BUS} LINE							
$R_{VBUS\_IDLE\_A}$	A-device V_{BUS} input impedance to ground	SRP (V_{BUS} pulsing) capable A-device not driving V_{BUS}, For $V_{BUS} < V_{SESS\_VLD}$, (When bit $R_{ABUSIN\_EN=1}$ $_{RVBUS\_IDLE\_A}$ / $R_{VUS\_IDLE\_A\_HI\_RANGE}$ impedance controlled automatically by hardware)		40		100	kΩ
$R_{VUS\_IDLE\_A\_HI\_RANGE}$	A-device V_{BUS} input impedance to ground (for V_{BUS} hi-range)	SRP (V_{BUS} pulsing) capable A-device not driving V_{BUS} For $V_{BUS} > V_{SESS\_VLD}$ (When bit $R_{ABUSIN\_EN=1}$ $_{RVBUS\_IDLE\_A}$ / $R_{VUS\_IDLE\_A\_HI\_RANGE}$ impedance controlled automatically by hardware)		70		100	kΩ
$R_{VBUS\_IDLE\_B}$	B-device V_{BUS} input impedance to ground	When bit R_{ABUSIN_EN} = 0 For V_{BUS} in range [0 V : 20 V] (Not valid for negative values of V_{BUS})		150	220	400	kΩ
$R_{B\_SRP\_DWN}$	B-device V_{BUS} SRP pulldown			5	10	20	kΩ
$R_{B\_SRP\_UP}$	B-device V_{BUS} SRP pullup			0.85	1.3	1.75	kΩ
$t_{RISE\_SRP\_UP\_MAX}$	B-device V_{BUS} SRP rise time maximum for OTG-A communication	0 to 2.1 V with < 13 µF load,	RV_{BUS} = 0 Ω and R1KSERIES = 0			31.4	ms
			RV_{BUS} = 1000 Ω ±10% and R1KSERIES = 1			57.8	
			RV_{BUS} = 1200 Ω ±10% and R1KSERIES = 1			64	
			RV_{BUS} = 1800 Ω ±10% and R1KSERIES = 1			85.4	
$t_{RISE\_SRP\_UP\_MIN}$	B-device V_{BUS} SRP rise time minimum for standard host connection	0.8 to 2.0 V with > 97 µF load,	RV_{BUS} = 0 Ω and R1KSERIES = 0	46.2			ms
			RV_{BUS} = 1000 Ω ±10% and R1KSERIES = 1	96			
			RV_{BUS} = 1200 Ω ±10% and R1KSERIES = 1	100			
			RV_{BUS} = 1800 Ω ±10% and R1KSERIES = 1	100			
	V_{BUS} line maximum voltage			–2		20	V

4.19 LS/FS Single-Ended Receivers

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB SINGLE-ENDED RECEIVERS						
SKWVP_VM	Skew between VP and VM	Driver outputs unloaded	–2	0	2	ns
VSE_HYS	Single-ended hysteresis		50			mV
V_{IH}	High (driven)		2			V
V_{IL}	Low				0.8	V

4.20 LS/FS Differential Receiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDI	Differential Input Sensitivity	Ref. USB2.0	200			mV
VCM	Differential Common Mode Range	Ref. USB2.0	0.8		2.5	V

4.21 LS Transmitter

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low	Ref. USB2.0	0		300	mV
V_{OH}	High (driven)	Ref. USB2.0	2.8		3.6	V
VCRS	Output signal crossover voltage	Ref. USB2.0	1.3		2	V
TFR	Rise time	Ref. USB2.0, covered by eye diagram	75		300	ns
TFF	Fall time	Ref. USB2.0, covered by eye diagram	75		300	ns
TFRFM	Differential rise and fall time matching		80%		125%	
TFDRATE	Low-speed data rate		1.4775		1.5225	Mb/s
	Total source jitter (including frequency tolerance):	Ref. USB2.0, covered by eye diagram				ns
TDJ1	To next transition		–25		25	
TDJ2	For paired transitions		–10		10	
TFEOPT	Source SE0 interval of EOP	Ref. USB2.0, covered by eye diagram	1.25		1.5	µs
	Downstream eye diagram	Ref. USB2.0, covered by eye diagram				
VCM	Differential common mode range	Ref. USB2.0	0.8		2.5	V

4.22 FS Transmitter

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low	Ref. USB2.0	0		300	mV
V_{OH}	High (driven)	Ref. USB2.0	2.8		3.6	V
VCRS	Output signal crossover voltage	Ref. USB2.0	1.3		2	V
TFR	Rise time	Ref. USB2.0, covered by eye diagram	4		20	ns
TFF	Fall time	Ref. USB2.0	4		20	ns
TFRFM	Differential rise and fall time matching	Ref. USB2.0, covered by eye diagram	90%		111.11%	
ZDRV	Driver output resistance	Ref. USB2.0	28		44	Ω
TFDRATE	Full-speed data rate	Ref. USB2.0, covered by eye diagram	11.97		12.03	Mb/s

FS Transmitter *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TDJ1	Total source jitter (including frequency tolerance): To next transition	Ref. USB2.0, covered by eye diagram	–2		2	ns
TDJ2	For paired transitions		–1		1	
TFEOPT	Source SE0 interval of EOP	Ref. USB2.0, covered by eye diagram	160		175	ns
	Downstream eye diagram	Ref. USB2.0, covered by eye diagram				
	Upstream eye diagram					

4.23 HS Transmitter

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VHSOI	High-speed idle level	Ref. USB2.0	–10		10	mV
VHSOH	High-speed data signaling high	Ref. USB2.0	360		440	mV
VHSOL	High-speed data signaling low	Ref. USB2.0	–10		10	mV
VCHIRPJ	Chirp J level (differential voltage)	Ref. USB2.0	700		1100	mV
VCHIRPK	Chirp K level (differential voltage)	Ref. USB2.0	–825		–500	mV
THSR	Rise time (10% to 90%)	Ref. USB2.0, covered by eye diagram	500			ps
	Fall time (10% to 90%)		500			
ZHSDRV	Driver output resistance (which also serves as high-speed termination)	Ref. USB2.0	40.5		49.5	Ω
THSDRAT	High-speed data range	Ref. USB2.0, covered by eye diagram	479.76		480.24	Mb/s
	Data source jitter	Ref. USB2.0, covered by eye diagram				
	Downstream eye diagram	Ref. USB2.0, covered by eye diagram				
	Upstream eye diagram	Ref. USB2.0, covered by eye diagram				

4.24 Pullup and Pulldown Resistors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULLUP RESISTORS						
RPUI	Bus pullup resistor on upstream port (idle bus)	Bus idle	0.9	1.1	1.575	kΩ
RPUA	Bus pullup resistor on upstream port (receiving)	Bus driven, outputs of the driver unloaded	1.425	2.2	3.09	
VIHZ	High (floating)	Pullups and pulldowns on both DP and DM lines	2.7		3.6	V
VPH_DP_UP	DP pullup voltage	Outputs of the driver unloaded	3	3.3	3.6	V
PULLDOWN RESISTORS						
RPH_DP_DWN RPH_DM_DWN	DP/DM pulldown	Outputs of the driver unloaded	14.25	18	24.8	kΩ
VIHZ	High (floating)	Pullups and pulldowns on both DP and DM lines	2.7		3.6	V
DP/-DATA LINE						
VOTG_DATA_LKG	On-the-go device leakage				0.342	V
ZINP	Input impedance exclusive of pullup and pulldown	Outputs of the driver unloaded, Measured at VDP or VDM = 0.8 V, and 2.0 V	800			kΩ
CHARGER DETECTION PULLUP RESISTOR						
RDP_WK_PU	DP weak pullup resistor	Measured at VBAT > VBAT_CERT	105	150	195	kΩ

4.25 Autoresume Watchdog Timer

over operating free-air temperature range (unless otherwise noted)

PARAMETER		NB CK32K cycles	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{AUTORESUME}$	Autoresume time-out	918		20.0	28.0	46.7	ms

4.26 UART Transceiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
UART TRANSMITTER AT DM PIN						
f_{UART_DFLT}	UART signaling rate				9600	bps
V_{OH_UART}	UART interface output high	I_{SOURCE} = 4 mA	V_{VDD33} – 0.4	V_{VDD33} – 0.1	3.6	V
V_{OL_UART}	UART interface output low	I_{SINK} = –4 mA	0	0.1	0.4	V
UART RECEIVER AT DP PIN						
V_{IH_UART}	UART interface input high	DP_PULLDOWN asserted	2			V
V_{IL_UART}	UART interface input low	DP_PULLDOWN asserted			0.8	V

4.27 OTG ID Electrical

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ID COMPARATORS — ID EXTERNAL RESISTORS SPECIFICATIONS						
R_{ID_FLOAT}	ID pulldown, when ID pin is floating	Input spec for external ID resistor	220			kΩ
R_{ID_A}	ACA ID pulldown, TUSB1211 is A-Device	Input spec for external ID resistor	119		132	kΩ
R_{ID_B}	ACA ID pulldown, TUSB1211 is B-Device, but can't connect	Input spec for external ID resistor	65		72	kΩ
R_{ID_C}	ACA ID pulldown, TUSB1211 is B-Device, can connect	Input spec for external ID resistor	35		39	kΩ
R_{IDGND}	ID pulldown when ID pin is grounded	Input spec for external ID resistor			1	kΩ
ID DETECTION CIRCUITRY						
R_{ID_UP}	ID pullup resistor	ID_PULLUP = '1, ID_WKPU = '0, Measured for V(ID) = [0.9,2.7]V	40	50	60	kΩ

OTG ID Electrical *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ID\_UP\_WK}$	ID weak pullup resistor	ID_PULLUP = '1, ID_WKPU = '1, Measured for V(ID) = [0.9,2.7]V	300	400	500	kΩ
ID_R_ID_A_TO_FLOAT	ID R_ID_A_TO_FLOAT comparator threshold	Internal ID comparator threshold	132	182	220	kΩ
ID_R_ID_B_TO_A	ID R_ID_B_TO_A comparator threshold	Internal ID comparator threshold	72	103	119	kΩ
ID_R_ID_C_TO_B	ID R_ID_C_TO_B comparator threshold	Internal ID comparator threshold	39	55	65	kΩ
ID_R_ID_GND_TO_C	ID ground-to-RID_C detection comparator threshold	Internal ID comparator threshold ID_PULLUP = '1, ID_WKPU = '1	20	27	30	kΩ
$V_{IDGND\text{-}to\text{-}RID\_C}$	ID ground-to-RID_C voltage detection threshold	ID_PULLUP = '1, ID_WKPU = '1, Valid for VBAT > VBAT_CERT max	0.9	1.05	2.0	V
V_{ID_MAX}	ID line maximum rated voltage				5.25	V
t_{ID_DEB}	ID detection debounce time	Min 48 cycles of CK32K clock Max 64 cycles of CK32K clock	1.3	1.5	2.8	ms
t_{ID_MASK}	ID detection mask	ID detection is masked for tID_MASK after IDPULLUP=1 or IDPULLUP_WK_EN=1 bits are enabled. Min 1120 cycles of CK32K clock Max 1152 cycles of CK32K clock During mask time TUSB1211 will indicate ID is grounded (ULPI RX CMD Bit6 = ID = 0).	29.5	35.2	50.0	ms

4.28 Electrical Specs – Charger Detection Currents

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SUSP} (USB BC Ver1.1 spec)	V_{BUS} maximum current in dead battery. Maximum current the device is allowed to draw from V_{BUS} in dead battery condition if V_{DP_SRC} is not asserted	Averaged over 1 s			1	mA
I_{VBAT_DET}	V_{BAT} maximum current during battery charger detection			450	550	µA
I_{DP_SRC}	Data contact detect current source		7		13	µA
I_{DM_SINK}	DM sink current		50		150	µA
$I_{DEV\_HCHG\_CHRP}$	Portable device current from charging downstream port during chirp	Refer to USB Battery Charging spec V1.1 Ch6.3.2 and values of VHSCM, and VCHIRPK			710	mA
$I_{VDP\_SRC\_ILIM}$	DP voltage source current limitation	VDP = 0 V			800	µA

4.29 Electrical Specs – Resistance

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DP_DWN}	DP pulldown resistance		14.25		24.8	kΩ
R_{DM_DWN}	DP pulldown resistance		14.25		24.8	kΩ
R_{DCHG_DAT}	Dedicated charging port resistance across DP/DM (input spec to TUSB1211)				200	Ω
R_{DCHRGR_PWR}	Dedicated charging port resistance from DP/DM to VBUS/GND (input spec to TUSB1211)		2			MΩ

4.30 Electrical Specs – Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{DCHG_PWR}	Dedicated charging port capacitance from DP or DP to VBUS or GND (input spec to TUSB1211)				1	nF

4.31 Charger Detection Debounce and Wait Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		NB CK32K CYCLES	TEST CONDITIONS	BC1.1 SPEC	MIN	TYP	MAX	UNIT
DEBVBUS_TIME	VBUS debounce time	459		> 10	12.1	14.0	20.0	ms
TIDP_SRC_ON	DP Current source on-time	8		> 200	210.5	244.1	347.8	µA
TVDP_SRC_ON	DP Voltage source on-time	1792		> 40	47.2	54.7	77.9	ms
TVDP_SRC_HICRNT	DP Voltage source off to high current on charger delay	1792		> 40	47.2	54.7	77.9	ms
TDCD_TIMEOUT	Data contact detect timeout	89400		> 2	2.4	2.7	3.9	s
TSVLD_CON_WKB	Session valid to connect for peripheral with dead or weak battery	53084160	Used to generate SVLDCONWKB_CNTR in FSM	< 45	27.0	23.3	38.5	min
TVDPSRC_CON	DP voltage source off to connect delay	N/A	Input spec	> 40	N/A	N/A	N/A	ms
TVDPSRC_DEB	VDP_SRC comparator debounce time	760	Used to generate CHGD_VDM_DEB in FSM	N/A	20.0	23.2	33.0	ms
TCHGD_SERX_DEB	Charger detect SERX debounce time	1520	Used to generate CHGD_SERX_DP_DEB and CHGD_SERX_DM_DEB in FSM	N/A	40.0	46.4	66.1	ms
TACA_SETUP	ACA setup time	2300		N/A	60.5	70.2	100.0	ms
TID_RARBRC_DEB	ACA ID RA, RB, RC comparators debounce	1520	Used to generate ID_RARBRC_DEB in FSM	N/A	40.0	46.4	66.1	ms

4.32 ULPI Interface

4.32.1 ULPI Interface Timing

Table 4-1. ULPI Interface Timing

PARAMETER	SYMBOL	MIN	MAX	UNIT
OUTPUT CLOCK				
Setup time (control in, 8-bit data in)	TSC, TSD		6	ns
Hold time (control in, 8-bit data in)	TSC, THD	0		ns
Output Delay (control out, 8-bit data out)	TDC, TDD		6.5	ns
INPUT CLOCK				
Setup time (control in, 8-bit data in)	TSC, TSD		3	ns
Hold time (control in, 8-bit data in)	TSC, THD	1.5		ns
Output Delay (control out, 8-bit data out)	TDC, TDD		6	ns

4.33 Power-On Timing Diagrams

4.33.1 Standard Power-up Timing

This scenario corresponds to standard power-up of TUSB1211 device in presence of valid V_{BAT}, V_{IO}, and chip selected (CS = 1 and CS_N = 0).

A timing diagram for standard power up is shown in Figure 4-1. In this plot USB ULPI clock is configured in output mode. A suggested application diagram for this configuration is shown in Section 6.

NOTE

The ULPI clock can also be configured in input mode, see Figure 4-1 for details.

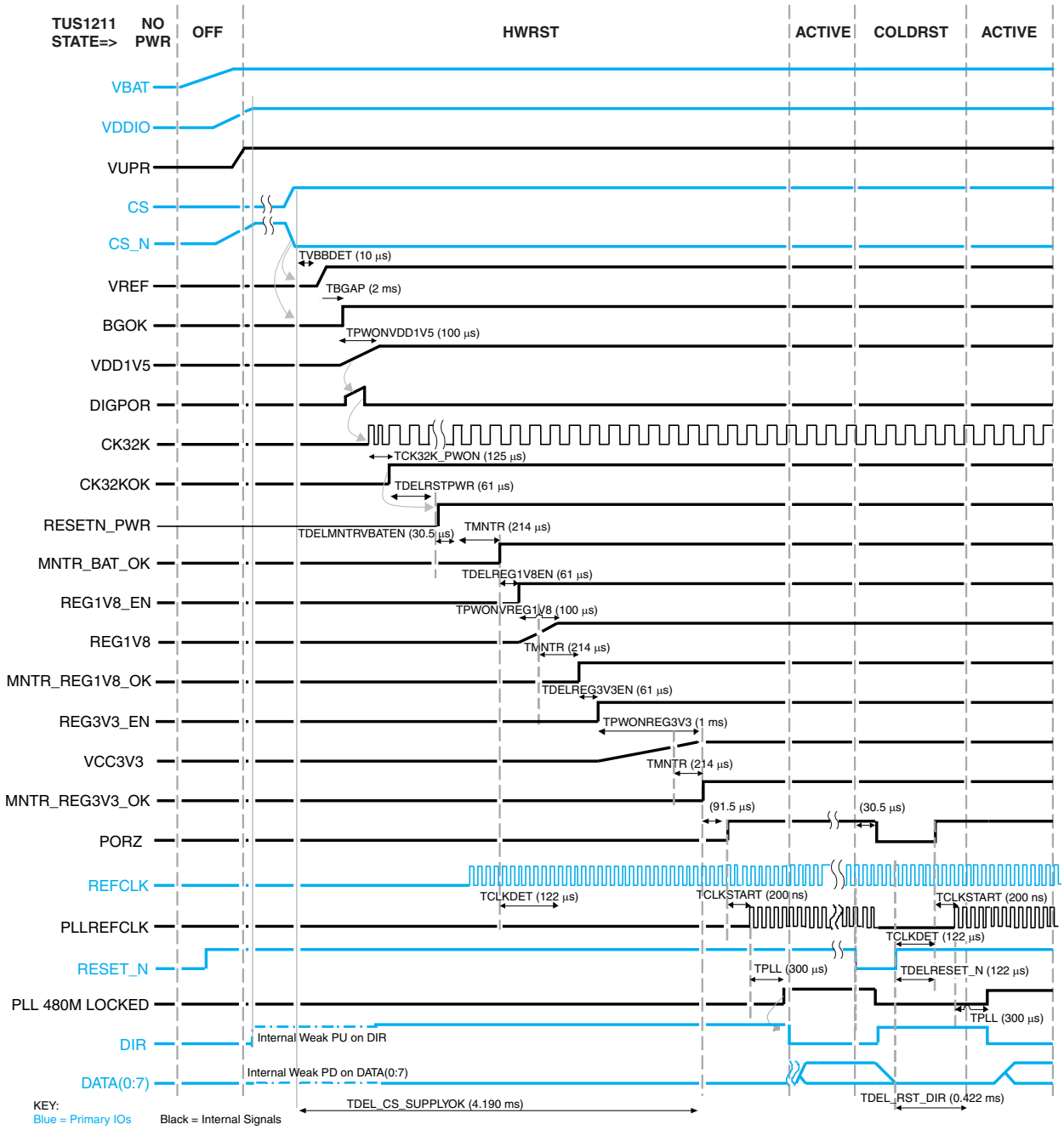


Figure 4-1. Power-Up Timing: (ULPI Clock Output Mode), Normal Battery

4.33.2 Hardware Charger Detection Power-Up Timing

This scenario corresponds to “dead battery” scenario in *USB Battery Charging Specification V1.1*.

Here VBUS is plugged while chip is not enabled (CS = 0 or CS_N = 1 or both), with VBAT > VBAT_DET. This causes the device to power up to and initiate Charger Detection through hardware. See Section 5.3.12 for details.

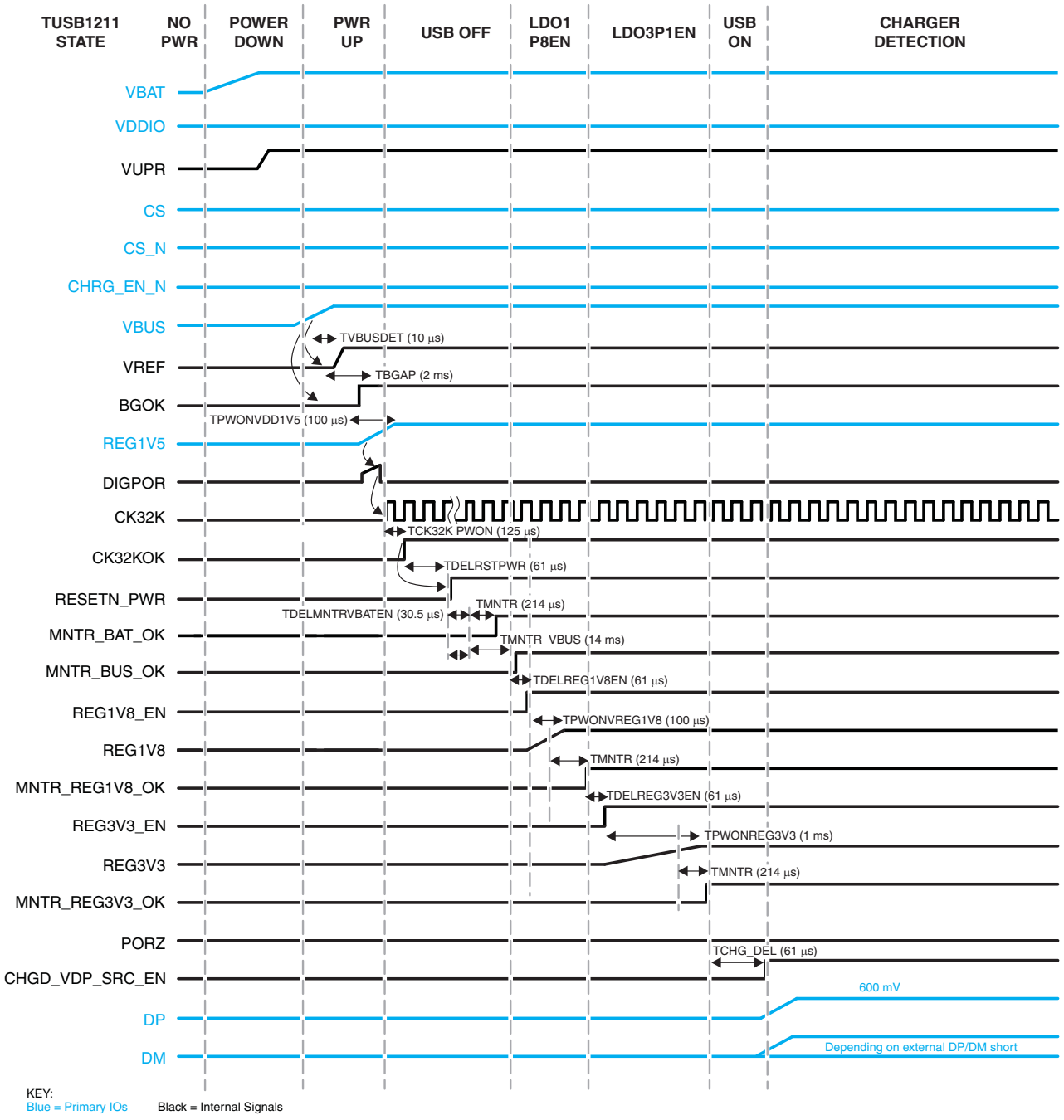


Figure 4-2. Power-Up Timing (ULPI Clock Output Mode), "Dead" Battery

4.34 Clock System

4.34.1 USB PLL Reference Clock

The USB PLL block generates the clocks used to synchronize:

- the ULPI interface (60 MHz clock)
- the USB interface (depending on the USB data rate, 480 Mbps, 12 Mbps or 1.5 Mbps)

TUSB1211 requires an external reference clock which is used as an input to the 480MHz USB PLL block. Depending on the clock configuration, this reference clock can be provided either at REFCLK pin or at CLOCK pin.

By default CLOCK pin is configured as an input.

Two clock configurations are possible:

- Input clock configuration (see Section 4.34.1.1)
- Output clock configuration (see Section 4.34.1.2)

4.34.1.1 ULPI Input Clock Configuration

In this mode REFCLK must be externally tied to GND.

CLOCK remains configured as an input.

When the ULPI interface is used in “input clock configuration”, that is, the 60 MHz ULPI clock is provided to TUSB1211 on CLOCK pin, then this is used as the reference clock for the 480 MHz USB PLL block.

4.34.1.2 ULPI Output Clock Configuration

In this mode a reference clock must be externally provided on REFCLK pin.

When an input clock is detected on REFCLK pin then CLOCK will automatically change to an output, that is, 60 MHz ULPI clock is output by TUSB1211 on CLOCK pin.

Two reference clock input frequencies are supported. REFCLK input frequency is communicated to TUSB1211 through a configuration pin, CFG, see F_{REFCLK} in Section 4.11 for frequency correspondence.

TUSB1211 supports square-wave reference clock input only.

4.35 Clock System

4.35.1 Internal Clock Generator (32 kHz)

An internal clock generator running at 32 kHz has been implemented to provide a low speed low power clock to the system. This is referred to as CK32K elsewhere in this specification.

4.36 Power Management

This chapter describes the electrical characteristics of the voltage regulators and timing characteristics of the supplies digitally controlled within the TUSB1211 device.

4.36.1 Power Provider

Table 4-2. Summary of Internal Power Providers(1)

SUPPLY NAME	PIN NAME	TYPE	TYPICAL VOLTAGE (V)
REG1V5	REG1V5	LDO	1.5
REG1V8	—	LDO	1.8
REG3V3	REG3V3	LDO	3.1

(1) REG3V3 may be supplied externally, or by shorting the REG3V3 pin to VBAT pin provided VBAT min is in range [3.2 V : 3.6 V]. Note that the REG3V3 LDO will always power-on when the chip is enabled, irrespective of whether VDD33 is supplied externally or not.

4.37 Power Provider

Table 4-3. Summary of the Power Provider

LDO NAME	PIN NAME	USAGE	TYPE	TYPICAL VOLTAGE (V)	MAXIMUM CURRENT
REG1V5	REG1V5	Internal	LDO	1.5	50 mA
REG1V8	—	Internal (capless)	LDO	1.8	30 mA
REG3V3	REG3V3	Internal	LDO	3.1	15 mA

4.37.1 REG3V3 Regulator

The REG3V3 internal LDO regulator powers the USB PHY, Charger detection, and OTG functions of the USB subchip inside TUSB1211.

It takes its power from the VBAT pin. It is connected to an external filtering capacitor at the REG3V3 pin (E3).

The USB standard requires data lines to be biased with pullups powered from a >3.0 V supply. Hence TUSB1211 cannot be guaranteed USB2.0 compliant for VBAT voltage lower than VBAT_CERT. TUSB1211 will however keep operating below this voltage.

4.37.2 REG1V8 Regulator

The REG1V8 internal LDO regulator powers the USB PHY, and USB PLL.

It takes its power from the V_{BAT} pin. This LDO is capless, that is, its output is not connected to any external pin.

Section 4.15 describes its characteristics.

4.37.3 REG1V5 Regulator

The REG1V5 internal LDO regulator powers the USB PHY and internal digital circuitry of TUSB1211. Section 4.16 describes the regulator characteristics.

It takes its power from the VBAT pin. It is connected to an external filtering capacitor at the REG1V5 pin (E6).

4.38 Power Control

TUSB1211 can be powered up in two different modes:

- Standard power-up condition

  For this, V_{BAT} and V_{IO} must be present and chip must be selected (CS=1 and CS_N=0). See Section 4.33.1. Standard Power-up Timing Power resources will be configured sequentially until the device reaches the power state.

  USBON . At this time internal power-on-reset signal PORZ will be released and USB PLL will start up. Once PLL is locked, the DIR output pin will be deasserted allowing TUSB1211 to be configured by the USB Link Controller through the ULPI interface.

  Note that by default TUSB1211 will be configured as a Host not providing VBUS as required by register map in ULPI specification Rev1.1.

  This is the case because OTG_CONTROL register bits DRVVBUS and DRVVBUSEXTERNAL bits are 0 by default, and DPPULLDOWN, DMPULLDOWN bits are 1 by default such that the 15 kΩ pulldown resistors at DP/DM pins are enabled by default.

  It is the responsibility of the link to enable external VBUS supply if required in Host mode, or to reconfigure the PHY if required in Device mode.

- Hardware charger detection power-up

  When the chip is not selected (CS=0 or CS_N=1), but VBUS is present and CHRG_EN_N pin is at GND, and VBAT > VBAT_MNTR then TUSB1211 will power-up in Hardware Charger Detection Mode.

  Power resources will be configured sequentially until the device reaches the power state USBON. However, because the chip is not selected, the internal power-on-reset signal PORZ will be not be released and USB PLL will not start up. Instead the device will enter the USB battery charger finite state machine (FSM) .

5 Detailed Description

5.1 Overview

The TUSB1211 device is optimized to be interfaced through a 12-pin SDR UTMI Low Pin Interface (ULPI), supporting both input clock and output clock modes, with 1.8 V interface supply voltage. The TUSB1211 device integrates a 3.3-V LDO, which makes it flexible to work with either battery operated systems or pure 3.3-V supplied systems. Both the main supply and the 3.3-V power domain can be supplied through an external switched-mode converter for optimized power efficiency.

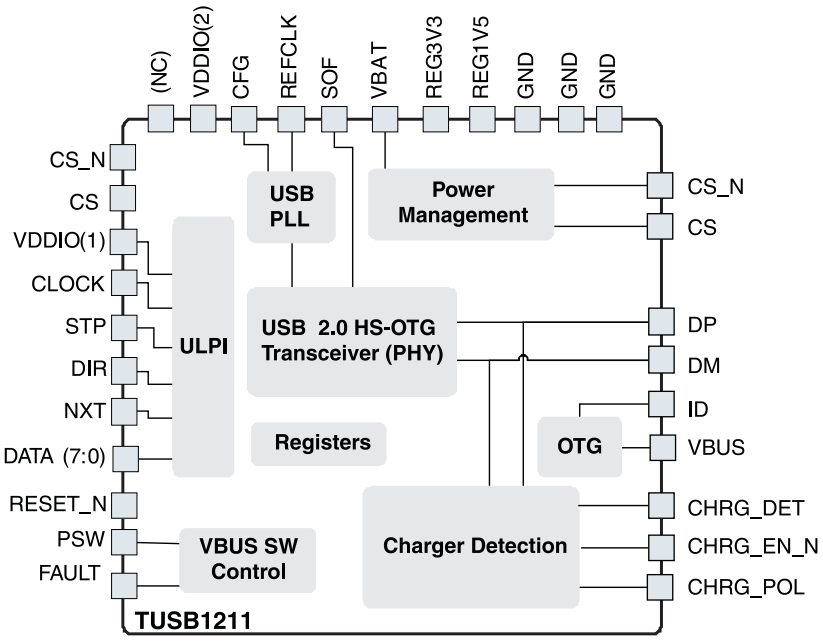
The TUSB1211 device includes a POR circuit to detect supply presence on V_{BAT} and V_{DDIO} pins. The TUSB1211 device can be disabled or configured in low power mode for energy saving.

The TUSB1211 device is protected against accidental shorts to 5 V or ground on its exposed interface (DP/DM/ID). It is also protected against up to 20-V surges on V_{BUS}.

The TUSB1211 device also supports the OTG (Ver1.3) optional addendum to the USB2.0 specification, including host negotiation protocol (HNP) and session request protocol (SRP).

The TUSB1211 device integrates a high-performance low-jitter 480-MHz PLL and supports two clock configurations. Depending on the required link configuration, the TUSB1211 device supports both ULPI input and output clock mode: input clock mode, in which case a square-wave 60-MHz clock is provided to TUSB1211 at the ULPI interface CLOCK pin; and output clock mode in which case the TUSB1211 device can accept a square-wave reference clock at REFCLK of either 19.2 MHz or 26 MHz. Frequency is indicated to the TUSB1211 device through the configuration pin CFG, which can be useful if a reference clock is already available in the system.

5.2 Functional Block Diagram



5.3 Feature Description

5.3.1 USB On-The-Go (OTG) Feature

The on-the-go (OTG) block integrates two main functions:

- ID resistor detection including Accessory Charger Adapter (ACA) detection
- V_{BUS} level detection and SRP pullup/pulldown resistors

5.3.2 V_{BUS} Detection Status Bits vs V_{BUS} Comparators

Four V_{BUS} comparators permit detection of four V_{BUS} levels as described in Table 5-1.

Table 5-1. V_{BUS} Detection Status Bits vs V_{BUS} Comparators

V_{BUS} COMPARATOR	DETECTION STATUS BIT	DETECTION BIT LOGIC
$V_{A\_VBUS\_VLD}$	VBUSVALID	VBUSVALID = 1 if $V_{BUS} > V_{A\_VBUS\_VLD}$ else 0
V_{SESS_VLD}	SESSVALID	SESSVALID = 1 if $V_{BUS} > V_{SESS\_VLD}$ else 0
$V_{B\_SESS\_VLD}$	BVALID_STS	BVALID_STS = 1 if $V_{BUS} > V_{B\_SESS\_VLD}$ else 0
$V_{B\_SESS\_END}$	SESSEND	SESSEND = 0 if $V_{BUS} > V_{B\_SESS\_END}$ else 1

5.3.3 USB Transceiver (PHY)

The TUSB1211 device includes a universal serial bus (USB) on-the-go (OTG) transceiver that supports USB 480-Mb/s high-speed (HS), 1-Mb/s full-speed (FS), and USB 1.5-Mb/s low-speed (LS) through a 12-pin UTMI+ low pin interface (ULPI).

NOTE

LS device mode is not allowed by a USB2.0 HS capable PHY, therefore it is not supported by the TUSB1211 device. This is clearly stated in USB2.0 standard Chapter 7, page 119, second paragraph: "*A high-speed capable upstream facing transceiver must not support low-speed signaling mode.*." There is also some related commentary in Chapter 7.1.2.3.

Table 5-2. Interface Target Frequencies

IO INTERFACE	INTERFACE DESIGNATION		TARGET FREQUENCY
USB	Universal serial bus	High speed	480 Mbits/s
		Full speed	12 Mbits/s
		Low speed	1.5 Mbits/s

5.3.3.1 PHY Overview

The PHY is the physical signaling layer of the USB 2.0. It essentially contains all the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through a standard 12-pin digital interface called UTMI+ low pin interface (ULPI).

The transmitters and receivers inside the PHY are classified into two main classes.

- The full-speed (FS) and low-speed (LS) transceivers. These are the legacy USB1.x transceivers.
- The HS (HS) transceivers

To bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A PLL which does a frequency multiplication to achieve the 480-MHz low-jitter clock necessary for USB and also the clock required for the switched capacitor resistance block.
- Internal biasing circuitry

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry which protects it from accidental short on the DP and DM lines to 5 V or GND.

5.3.4 LS/FS Single-Ended Receivers

In addition to the differential receiver, there is a single-ended receiver (SE–, SE+) for each of the two data lines DP/–. The main purpose of the single-ended receivers is to qualify the DP and DM signals in the full-speed/low-speed modes of operation.

5.3.5 LS/FS Differential Receiver

A differential input receiver (Rx) retrieves the LS/FS differential data signaling. The differential voltage on the line is converted into digital data by a differential comparator on DP/DM. This data is then sent to a clock and data recovery circuit that recovers the clock from the data. An additional serial mode exists in which the differential data is directly output on the RXRCV pin.

5.3.6 LS/FS Transmitter

The USB transceiver (Tx) uses a differential output driver to drive the USB data signal DP/– onto the USB cable. The driver's outputs support 3-state operation to achieve bidirectional half-duplex transactions.

5.3.7 HS Differential Receiver

The HS receiver consists of the following blocks:

- A differential input comparator to receive the serial data
- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a NRZI decoder, bit unstuffing, and serial-to-parallel converter to generate the ULPI DATAOUT

Table 5-3. HS Differential Receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	Ref. USB2.0	100		150	mV
VHSDSC	High-speed disconnect detection threshold (differential signal amplitude)	Ref. USB2.0	525		625	mV
	High-speed differential input signaling levels	Ref. USB2.0, specified by eye pattern templates				mV
VHSCM	High-speed data signaling common mode voltage range (guidelines for receiver)	Ref. USB2.0	–50		500 (1)	mV
	Receiver jitter tolerance	Ref. USB2.0, specified by eye pattern templates			150	ps

(1) For low-frequency Chirp signaling, the max common mode voltage range value is 600 mV

5.3.8 HS Differential Transmitter

The HS transmitter is always operated through the ULPI parallel interface. The parallel data on the interface is serialized, bit stuffed, NRZI encoded, and transmitted as a dc output current on DP or DM depending on the data. Each line has an effective 22.5-Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double thereby doubling the differential amplitude seen on the DP/DM lines.

5.3.9 Autoresume

Asserting AUTORESUME bit enables the PHY to automatically transmit resume signaling.

Refer to USB2.0 specification Section 7.1.7.7 and Section 7.9 for more details. When autoresume is enabled, if the PHY detects a resume-K it takes automatically over-driving of the resume-K within 1 ms.

If AUTORESUME_WDOG_EN bit is set (default is 1), then an internal autoresume watchdog timer, based on the internal 32K oscillator, CK32K, will be initialized and will start counting when the PHY detects a resume-K.

If AUTORESUME_WDOG_EN bit is set then if the PHY does not receive a TXCMD of the NOPID type within TAUTORESUME it will stop driving the resume-K and the USB bus will go back to IDLE-J state Otherwise the PHY will continue to drive the resume-K until it receives a TXCMD of the NOPID type from the LINK.

5.3.10 UART Transceiver

By setting CARKITMODE bit in IFC_CTRL register, the TUSB1211 device will enter UART mode. In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter at DM pin and receiver at DP pin. See Figure 5-1 for the USB UART data flow.

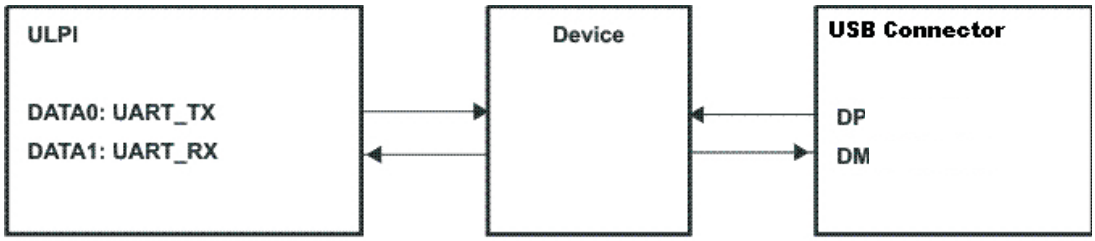


Figure 5-1. USB UART Data Flow

5.3.11 USB On-The-Go (OTG)

5.3.11.1 ID Detection Status Bits vs ID Comparators

Four ID comparators permit detection of five external ID resistances as described in Table 5-4.

Table 5-4. OTG ID Detection Status Bits vs ID Comparators

EXTERNAL RID DETECTED	DETECTION STATUS BIT	DETECTION BIT LOGIC (DETECTION IF COMP1 < R_{ID} < Comp2)	COMP1	COMP2
R_{ID_FLOAT}	ID_FLOAT_STS	ID_FLOAT_STS = 1 if (ID_R_ID_A_TO_FLOAT < RID) else 0	ID_R_ID_A_TO_FLOAT	—
R_{ID_A}	ID_RARBRC_STS<1:0>	ID_RARBRC_STS<1:0> = "11" if (ID_R_ID_B_TO_A < RID < ID_R_ID_A_TO_FLOAT) else 0	ID_R_ID_B_TO_A	ID_R_ID_A_TO_FLOAT
R_{ID_B}	ID_RARBRC_STS<1:0>	ID_RARBRC_STS<1:0> = "10" if (ID_R_ID_C_TO_B < RID < ID_R_ID_B_TO_A) else 0	ID_R_ID_C_TO_B	ID_R_ID_B_TO_A
R_{ID_C}	ID_RARBRC_STS<1:0>	ID_RARBRC_STS<1:0> = "01" if (ID_R_ID_GND_TO_C < RID < ID_R_ID_C_TO_B) else 0	ID_R_ID_GND_TO_C	ID_R_ID_C_TO_B
R_{IDGND}	IDGND	IDGND = 0 if (RID < ID_R_ID_GND_TO_C) else 1	—	ID_R_ID_GND_TO_C

5.3.12 USB Battery Charger Detection and ACA

In order to support Battery Charging Specification v1.1 April 2009 [BCS v1.1], a charger detection module is included inside the TUSB1211 module.

This feature includes:

- Battery charger detection sensing and control on DP/DM lines
- ACA (Accessory Charger Adapter) detection and control on ID line

The detection mechanism aims at distinguishing several types of power sources that can be connected on VBUS line:

- Dedicated Charging Port
- Standard Downstream Port
- Charging Downstream Port

Hardware includes:

- a dedicated voltage referenced pullup on DP line
- a dedicated current controlled pulldown on DM line
- a detection comparator on DM line—a control/detection finite state machine (FSM) including timers
- a charger detection output pin (CHRG_DET) for external charger control
- detection comparators on ID line

ID pin status detection (as defined per OTG v1.3 standard as well as ACA resistor types as described in BCS v1.1) and DP/DM Single-Ended receivers (as defined per USB v2.0 standard) are also used to determine the type of device plugged on USB connector.

USB charger detection is an independent feature, on V_{BAT} supply domain, using CK32K clock.

5.3.13 USB Battery Charger Detection Modes

There are 3 modes of operation of battery charger detection module:

1. Hardware Charger Detection Module
2. Software Mode
3. Software FSM Mode

5.3.14 Accessory Charger Adapter (ACA) Detection

Accessory Charger Adapter (ACA) feature is defined in the USB Battery Charging Specification Rev. 1.1 specification. ACA allows simultaneous connection of a USB Charger or Charging Downstream Port and an Accessory to a portable OTG device (TUSB1211).through only a single USB OTG port.

5.4 Register Maps

Table 5-5. USB Register Summary

REGISTER NAME	TYPE	REGISTER WIDTH (BITS)	PHYSICAL ADDRESS
VENDOR_ID_LO	R	8	0x00
VENDOR_ID_HI	R	8	0x01
PRODUCT_ID_LO	R	8	0x02
PRODUCT_ID_HI	R	8	0x03
FUNC_CTRL	RW	8	0x04
FUNC_CTRL_SET	RW	8	0x05
FUNC_CTRL_CLR	RW	8	0x06
IFC_CTRL	RW	8	0x07
IFC_CTRL_SET	RW	8	0x08
IFC_CTRL_CLR	RW	8	0x09
OTG_CTRL	RW	8	0x0A
OTG_CTRL_SET	RW	8	0x0B
OTG_CTRL_CLR	RW	8	0x0C
USB_INT_EN_RISE	RW	8	0x0D
USB_INT_EN_RISE_SET	RW	8	0x0E
USB_INT_EN_RISE_CLR	RW	8	0x0F
USB_INT_EN_FALL	RW	8	0x10
USB_INT_EN_FALL_SET	RW	8	0x11
USB_INT_EN_FALL_CLR	RW	8	0x12
USB_INT_STS	R	8	0x13
USB_INT_LATCH	R	8	0x14
DEBUG	R	8	0x15
SCRATCH_REG	RW	8	0x16
SCRATCH_REG_SET	RW	8	0x17
SCRATCH_REG_CLR	RW	8	0x18
Reserved	R	8	0x19 0x2E
ACCESS_EXT_REG_SET	RW	8	0x2F
Reserved	R	8	0x30 0x3C
POWER_CONTROL	RW	8	0x3D
POWER_CONTROL_SET	RW	8	0x3E
POWER_CONTROL_CLR	RW	8	0x3F
VENDOR_SPECIFIC1	RW	8	0x80
VENDOR_SPECIFIC1_SET	RW	8	0x81
VENDOR_SPECIFIC1_CLR	RW	8	0x82
VENDOR_SPECIFIC2_STS	R	8	0x83
VENDOR_SPECIFIC2_LATCH	R	8	0x84
VENDOR_SPECIFIC3	RW	8	0x85
VENDOR_SPECIFIC3_SET	RW	8	0x86
VENDOR_SPECIFIC3_CLR	RW	8	0x87
VENDOR_SPECIFIC4	RW	8	0x88
VENDOR_SPECIFIC4_SET	RW	8	0x89
VENDOR_SPECIFIC4_CLR	RW	8	0x8A
VENDOR_SPECIFIC5	RW	8	0x8B
VENDOR_SPECIFIC5_SET	RW	8	0x8C
VENDOR_SPECIFIC5_CLR	RW	8	0x8D
VENDOR_SPECIFIC6	RW	8	0x8E
VENDOR_SPECIFIC6_SET	RW	8	0x8F
VENDOR_SPECIFIC6_CLR	RW	8	0x90

5.4.1 VENDOR_ID_LO

ADDRESS OFFSET	0x00		
PHYSICAL ADDRESS	0x00	**INSTANCE**	USB_SCUSB
DESCRIPTION	Lower byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451)		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
VENDOR_ID							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	VENDOR_ID		R	0x51

5.4.2 VENDOR_ID_HI

ADDRESS OFFSET	0x01		
PHYSICAL ADDRESS	0x01	**INSTANCE**	USB_SCUSB
DESCRIPTION	Upper byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451)		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
VENDOR_ID							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	VEN DOR_ID		R	0x04

5.4.3 PRODUCT_ID_LO

ADDRESS OFFSET	0x02		
PHYSICAL ADDRESS	0x02	**INSTANCE**	USB_SCUSB
DESCRIPTION	Lower byte of Product ID supplied by Vendor (SAUSB Product ID is 0x1508).		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
PRODUCT_ID							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	PRODUCT_ID		R	0x08

5.4.4 PRODUCT_ID_HI

ADDRESS OFFSET	0x03		
PHYSICAL ADDRESS	0x03	**INSTANCE**	USB_SCUSB
DESCRIPTION	Upper byte of Product ID supplied by Vendor (SAUSB Product ID is 0x1508).		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
PRODUCT_ID							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	PRODUCT_ID		R	0x15

5.4.5 FUNC_CTRL

ADDRESS OFFSET	0x04		
PHYSICAL ADDRESS	0x04	**INSTANCE**	USB_SCUSB
DESCRIPTION	Controls UTMI function settings of the PHY.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	SUSPENDM	Active low PHY suspend. Put PHY into Low Power Mode. In Low Power Mode the PHY power down all blocks except the full speed receiver, OTG comparators, and the ULPI interface pins. The PHY automatically set this bit to '1' when Low Power Mode is exited.	RW	1
5	RESET	Active high transceiver reset. Does not reset the ULPI interface or ULPI register set. Once set, the PHY asserts the DIR signal and reset the UTMI core. When the reset is completed, the PHY de-asserts DIR and clears this bit. After de-asserting DIR, the PHY re-assert DIR and send an RX command update. Note: This bit is auto-cleared, this explain why it can't be read at '1'.	RW	0
4:03	OPMODE	Select the required bit encoding style during transmit 0x0: Normal operation 0x1: Non-driving 0x2: Disable bit-stuff and NRZI encoding 0x3: Reserved (No SYNC and EOP generation feature not supported)	RW	0x0
2	TERMSELECT	Controls the internal 1.5 kΩ pullup resistor and 45 Ω HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown.	RW	0
1:0	XCVRSELECT	Select the required transceiver speed. 0x0: Enable HS transceiver 0x1: Enable FS transceiver 0x2: Enable LS transceiver 0x3: Enable FS transceiver for LS packets (FS preamble is automatically pre-pended)	RW	0x1

5.4.6 FUNC_CTRL_SET

ADDRESS OFFSET	0x05		
PHYSICAL ADDRESS	0x05	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	SUSPENDM		RW	1
5	RESET		RW	0
4:3	OPMODE		RW	0x0
2	TERMSELECT		RW	0
1:0	XCVRSELECT		RW	0x1

5.4.7 FUNC_CTRL_CLR

ADDRESS OFFSET	0x06		
PHYSICAL ADDRESS	0x06	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	SUSPENDM		RW	1
5	RESET		RW	0
4:3	OPMODE		RW	0x0
2	TERMSELECT		RW	0
1:0	XCVRSELECT		RW	0x1

5.4.8 IFC_CTRL

ADDRESS OFFSET	0x07		
PHYSICAL ADDRESS	0x07	**INSTANCE**	USB_SCUSB
DESCRIPTION	Enables alternative interfaces and PHY features.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	INDICATORPASSTHRU	INDICATORCOMPLEMENT	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states stp and data. 0b: Enables the interface protect circuit 1b: Disables the interface protect circuit	RW	0
6	INDICATORPASSTHRU	Controls whether the complement output is qualified with the internal vbusvalid comparator before being used in the VBUS State in the RXCMD. EXTERNALVBUSINDICATOR input signal is the FAULT input pin of TUSB1211. 0b: Complement output signal is qualified with the internal VBUSVALID comparator. 1b: Complement output signal is not qualified with the internal VBUSVALID comparator.	RW	0
5	INDICATORCOMPLEMENT	Tells the PHY to invert EXTERNALVBUSINDICATOR input signal, generating the complement output. EXTERNALVBUSINDICATOR input signal is the FAULT input pin of TUSB1211. 0b: PHY will not invert signal EXTERNALVBUSINDICATOR (default) 1b: PHY will invert signal EXTERNALVBUSINDICATOR	RW	0
4	AUTORESUME	Enables the PHY to automatically transmit resume signaling. Refer to USB specification 7.1.7.7 and 7.9 for more details. 0 = AutoResume disabled (default) 1 = AutoResume enabled	RW	0
3	CLOCKSUSPENDM	Active low clock suspend. Valid only in Serial Modes. Powers down the internal clock circuitry only. Valid only when SuspendM = 1b. The PHY must ignore ClockSuspend when SuspendM = 0b. By default, the clock will not be powered in Serial and Carkit Modes. 0b : Clock will not be powered in Serial and UART Modes. 1b : Clock will be powered in Serial and UART Modes.	RW	0
2	CARKITMODE	Changes the ULPI interface to UART interface. The PHY automatically clear this field when UART mode is exited. 0b: UART disabled. 1b: Enable serial UART mode.	RW	0
1	FSLSSERIALMODE_3PIN	Changes the ULPI interface to 3-pin Serial. The PHY must automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using parallel interface 1b: FS/LS packets are sent using 3-pin serial interface	RW	0
0	FSLSSERIALMODE_6PIN	Changes the ULPI interface to 6-pin Serial. The PHY must automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using parallel interface 1b: FS/LS packets are sent using 6-pin serial interface	RW	0

5.4.9 IFC_CTRL_SET

ADDRESS OFFSET	0x08		
PHYSICAL ADDRESS	0x08	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the ifc_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	INDICATORPASSTHRU	INDICATORCOMPLEMENT	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	INTERFACE_PROTECT_DISABLE		RW	0
6	INDICATORPASSTHRU		RW	0
5	INDICATORCOMPLEMENT		RW	0
4	AUTORESUME		RW	0
3	CLOCKSUSPENDM		RW	0
2	CARKITMODE		RW	0
1	FSLSSERIALMODE_3PIN		RW	0
0	FSLSSERIALMODE_6PIN		R	0

5.4.10 IFC_CTRL_CLR

ADDRESS OFFSET	0x09		
PHYSICAL ADDRESS	0x09	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the ifc_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	IN DICATORPASSTHRU	INDICATORCOMPLEMENT	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	INTERFACE_PROTECT_DISABLE		RW	0
6	INDICATORPASSTHRU		RW	0
5	INDICATORCOMPLEMENT		RW	0
4	AUTORESUME		RW	0
3	CLOCKSUSPENDM		RW	0
2	CARKITMODE		RW	0
1	FSLSSERIALMODE_3PIN		RW	0
0	FSLSSERIALMODE_6PIN		R	0

5.4.11 OTG_CTRL

ADDRESS OFFSET	0x0A		
PHYSICAL ADDRESS	0x0A	**INSTANCE**	USB_SCUSB
DESCRIPTION	Controls UTMI+ OTG functions of the PHY.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
USEEXTERNALVBUSINDICATOR	DRVVBUSEXTERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	USEEXTERNALVBUSINDICATOR	Tells the PHY to use an external VBUS over-current indicator. EXTERNALVBUSINDICATOR input signal is the FAULT input pin of TUSB1211. 0b: Use the internal OTG comparator (VA_VBUS_VLD) or internal VBUS valid indicator (default) 1b: Use external VBUS valid indicator signal.	RW	0
6	DRVVBUSEXTERNAL	Selects between the internal and the external 5 V VBUS supply. 0b: Drive VBUS using the internal charge pump. This function does nothing as TUSB1211 does not include an internal charge-pump (default) 1b: Drive VBUS using external supply (assert PSW pin).	RW	0
5	DRVVBUS	Signals the internal charge pump to drive 5 V on VBUS. 0b : do not drive VBUS (deassert PSW pin) 1b : drive 5V on VBUS (assert PSW pin)	RW	0
4	CHRGVBUS	Charge VBUS through a resistor. Used for VBUS pulsing SRP. The Link must first check that VBUS has been discharged (see DischrgVbus register bit), and that both DP and DM data lines have been low (SE0) for 2 ms. 0b : do not charge VBUS 1b : charge VBUS	RW	0
3	DISCHRGVBUS	Discharge VBUS through a resistor. If the Link sets this bit to 1, it waits for an RX CMD indicating SessEnd has transitioned from 0 to 1, and then resets this bit to 0 to stop the discharge. 0b : do not discharge VBUS 1b : discharge VBUS	RW	0
2	DMPULLDOWN	Enables the 15 kΩ pulldown resistor on DM. 0b : Pulldown resistor not connected to DM. 1b : Pulldown resistor connected to DM.	RW	1
1	DPPULLDOWN	Enables the 15 kΩ pulldown resistor on DP. 0b : pulldown resistor not connected to DP. 1b : pulldown resistor connected to DP.	RW	1
0	IDPULLUP	Connects a pullup to the ID line and enables sampling of the signal level. 0b Disable sampling of ID line. when IDPULLUP_WK_EN = 0 :	RW	0

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
		Enable sampling of the ID line when IDPULLUP_WK_EN = 1 Note Weak pull-up (RID_UP_WK) on ID is enabled when IDPULLUP = 0 to avoid floating condition, but sampling is not enabled unless IDPULLUP_WK_EN = 1 1b Enable sampling of ID line and strong pullup resistor (RID_UP) on ID : Note: If ACA_DET_EN=1, then ID strong pullup resistor will be enabled automatically during ACA detection states (ACA_DETECTION, ACA_SETUP) of the charger detection state-machine , irrespective of status of IDPULLUP bit. This is to ensure correct functionality of ID ACA RA/RB/RC detection comparators. Otherwise ID pullup is controlled as described above.		

5.4.12 OTG_CTRL_SET

ADDRESS OFFSET	0x0B		
PHYSICAL ADDRESS	0x0B	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the otg_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
USEEXTERNALVBUSINDICATOR	DRVVBUSEXTERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	USEEXTERNALVBUSINDICATOR		RW	0
6	DRVVBUSEXTERNAL		RW	0
5	DRVVBUS		RW	0
4	CHRGVBUS		RW	0
3	DISCHRGVBUS		RW	0
2	DMPULLDOWN		RW	1
1	DPPULLDOWN		RW	1
0	IDPULLUP		RW	0

5.4.13 OTG_CTRL_CLR

ADDRESS OFFSET	0x0C		
PHYSICAL ADDRESS	0x0C	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the otg_ctrl register with read/Clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
USEEXTERNALVBUSINDICATOR	DRVVBUSEXTERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	USEEXTERNALVBUSINDICATOR		RW	0
6	DRVVBUSEXTERNAL		RW	0
5	DRVVBUS		RW	0
4	CHRGVBUS		RW	0
3	DISCHRGVBUS		RW	0
2	DMPULLDOWN		RW	1
1	DPPULLDOWN		RW	1
0	IDPULLUP		RW	0

5.4.14 USB_INT_EN_RISE

ADDRESS OFFSET	0x0D		
PHYSICAL ADDRESS	0x0D	**INSTANCE**	USB_SCUSB
DESCRIPTION	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high.	RW	1
		Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1.		
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high.	RW	1
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high.	RW	1
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).	RW	1

5.4.15 USB_INT_EN_RISE_SET

ADDRESS OFFSET	0x0E		
PHYSICAL ADDRESS	0x0E	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

5.4.16 USB_INT_EN_RISE_CLR

ADDRESS OFFSET	0x0F		
PHYSICAL ADDRESS	0x0F	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEN D_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

5.4.17 USB_INT_EN_FALL

ADDRESS OFFSET	0x10		
PHYSICAL ADDRESS	0x10	**INSTANCE**	USB_SCUSB
DESCRIPTION	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL	Generate an interrupt event notification when IdGnd changes from high to low. Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1.	RW	1
3	SESSEND_FALL	Generate an interrupt event notification when SessEnd changes from high to low.	RW	1
2	SESSVALID_FALL	Generate an interrupt event notification when SessValid changes from high to low. SessValid is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_FALL	Generate an interrupt event notification when VbusValid changes from high to low.	RW	1
0	HOSTDISCONNECT_FALL	Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).	RW	1

5.4.18 USB_INT_EN_FALL_SET

ADDRESS OFFSET	0x11		
PHYSICAL ADDRESS	0x11	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action)		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL		RW	1
3	SESSEND_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

5.4.19 USB_INT_EN_FALL_CLR

ADDRESS OFFSET	0x12		
PHYSICAL ADDRESS	0x12	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL		RW	1
3	SESSEN D_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

5.4.20 USB_INT_STS

ADDRESS OFFSET	0x13		
PHYSICAL ADDRESS	0x13	**INSTANCE**	USB_SCUSB
DESCRIPTION	Indicates the current value of the interrupt source signal.		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND	SESSEND	SESSVALID	VBUSVALID	HOSTDISCONNECT

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND	Current value of UTMI+ IdGnd output. This bit is not updated if IdPullup bit is reset to 0 and for 50 ms after IdPullup is set to 1.	R	0
3	SESSEND	Current value of UTMI+ SessEnd output.	R	0
2	SESSVALID	Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid.	R	0
1	VBUSVALID	Current value of UTMI+ VbusValid output.	R	0
0	HOSTDISCONNECT	Current value of UTMI+ Hostdisconnect output. Applicable only in host mode. Automatically reset to 0 when Low Power Mode is entered. NOTE: Reset value is '0' when host is connected. Reset value is '1' when host is disconnected.	R	0

5.4.21 USB_INT_LATCH

ADDRESS OFFSET	0x14		
PHYSICAL ADDRESS	0x14	**INSTANCE**	USB_SCUSB
DESCRIPTION	These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial Mode or Carkit Mode is entered regardless of the value of ClockSuspendM. The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit. It is important to note that if register read data is returned to the Link in the same cycle that a USB Interrupt Latch bit is to be set, the interrupt condition is given immediately in the register read data and the Latch bit is not set. Note that it is optional for the Link to read the USB Interrupt Latch register in Synchronous Mode because the RX CMD byte already indicates the interrupt source directly		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.	R	0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.	R	0
2	SESSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid.	R	0
1	VBUSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.	R	0
0	HOSTDISCONNECT_LATCH	Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode. NOTE: As this IT is enabled by default, the reset value depends on the host status Reset value is '0' when host is connected. Reset value is '1' when host is disconnected.	R	0

5.4.22 DEBUG

ADDRESS OFFSET	0x15		
PHYSICAL ADDRESS	0x15	**INSTANCE**	USB_SCUSB
DESCRIPTION	Indicates the current value of various signals useful for debugging.		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LINESTATE	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1:0	LINESTATE	These signals reflect the current state of the single ended receivers. They directly reflect the current state of the DP (LineState[0]) and DM (LineState[1]) signals. Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp) Read 0x1: LS: 'K' State, FS: 'J' State, HS: !Squelch, Chirp: !Squelch and HS_Differential_Receiver_Output Read 0x2: LS: 'J' State, FS: 'K' State, HS: Invalid, Chirp: !Squelch and !HS_Differential_Receiver_Output Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp)	R	0x0

5.4.23 SCRATCH_REG

ADDRESS OFFSET	0x16		
PHYSICAL ADDRESS	0x16	**INSTANCE**	USB_SCUSB
DESCRIPTION	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SCRATCH							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	SCRATCH	Scratch data.	RW	0x00

5.4.24 SCRATCH_REG_SET

ADDRESS OFFSET	0x17		
PHYSICAL ADDRESS	0x17	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the scratch_reg register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SCRATCH							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	SCRATCH		RW	0x00

5.4.25 SCRATCH_REG_CLR

ADDRESS OFFSET	0x18		
PHYSICAL ADDRESS	0x18	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the scratch_reg with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SCRATCH							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	SCRATCH		RW	0x00

5.4.26 POWER_CONTROL

ADDRESS OFFSET	0x3D		
PHYSICAL ADDRESS	0x3D	**INSTANCE**	USB_SCUSB
DESCRIPTION	Power Control register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
HWDETECT	DP_VSRC_EN	VDAT_DET	DP_WKPU_EN	BVALID_FALL	BVALID_RISE	DET_COMP	SW_CONTROL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	HWDETECT	When SW_CONTROL= 0, HWDETECT bit is read-only. This bit indicates if the transceiver is connected to a Charging Port (Dedicated Charging Port or Charging Downstream Port). 0b: No charger detected. 1b: Charger detected. Note when SW_CONTROL=0, hardware controls the CHRG_DET pin with the same logic described below for SW_CONTROL=1 case. When SW_CONTROL=1, HWDETECT is writeable. This bit allows manual control over the logic levels on the CHRG_DET pin. 0b: CHRG_DET is externally pulled LOW (CHRG_DET_POL is HIGH) or CHRG_DET is externally pulled HIGH (CHRG_DET_POL is LOW). 1b: CHRG_DET is driven LOW (CHRG_DET_POL is LOW) or CHRG_DET is driven HIGH (CHRG_DET_POL is HIGH)	RW	0
6	DP_VSRC_EN	This bit controls whether DP is allowed to send V_{DAT_SRC}, which is a sensing voltage for charger detection. This bit also enables I_{DAT_SINK} on DM and V_{DAT_REF}. (Used when manual control over the charger detection is needed.) Note when SW_CONTROL=0, this bit is read-only. In this case hardware controls I_{DAT_SINK} and V_{DAT_REF} with the same logic described below for SW_CONTROL=1 case. When SW_CONTROL=1, DP_VSRC_EN is writeable: 0b: No transmission of sensing voltage is performed. IDAT_SINK and VDAT_REF are disabled. 1b: DP transmits sensing voltage; enables IDAT_SINK and VDAT_REF.	RW	0
5	VDAT_DET	This bit indicates the presence of a voltage level higher that VDAT_REF on the DM. (Used when manual control over the charger detection is needed.) 0b: Voltage on DM is lower than VDAT_REF 1b: Voltage on DM is higher than VDAT_REF	RW	0
4	DP_WKPU_EN	Enables the weak pull-up resistor on the DP pin in synchronous mode when VBUS is above the VSESS_VLD threshold. 0b: DP weak pull-up is disabled. 1b: DP weak pull-up is enabled when VBUS > VSESS_VLD Detection of DP/DM condition while this bit is set should be done through LINESTATE<1:0>bits in DEBUG register (0x15) or through RX CMD.	RW	0
3	BVALID_FALL	Enables RX CMD's for high to low transitions on BVALID. When BVALID changes from high to low, the USB TRANS will send an RX CMD to the link with the alt_int bit set to 1b. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.	RW	0
2	BVALID_RISE	Enables RX CMD's for low to high transitions on BVALID. When BVALID changes from low to high, the USB Trans will send an RX CMD to the link with the alt_int bit set to 1b. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.	RW	0

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
1	DET_COMP	This bit indicates if a Charging Port has been detected. 0b: A Charging Port has not been detected, or charger detection has not been activated. (Identical to HWDETECT) 1b: A Charging Port has been detected (Identical to HWDETECT) When SW_CONTROL = 1 this bit is reset to 0.	RW	0
0	SW_CONTROL	This bit controls whether CHRG_DET pin is controlled automatically or manually. When manual control is required, the software must set the SW_CONTROL bit to logic 1 in the first register access, followed by issuing a second register access to set or clear the HWDETECT bit. Software must never set the SW_CONTROL bit and change the HWDETECT bit in the same register access. 0b: The CHRG_DET pin will be asserted or deasserted depending on the automatic USB charger detection result. 1b: At rising-edge of SW_CONTROL bit save current hardware charger detection context and hand-off control to software: a. DP_VSRC_EN register bit is loaded with current status of VDP_SRC b. HWDETECT register bit is loaded with current status of charger detection result. Therefore battery charger indication signal to external charger remains unchanged. c. Charger detection circuitry is maintained enabled if it was enabled in dead-battery condition d. Charger Detection FSM is exited (to state USB_DET_OFF) e. Control of POWER_CONTROL register bits is handed over to software Therefore if charger detection has been initiated in dead-battery condition (while the chip is disabled (CS=0)), VDP_SRC will remain enabled and CHRG_DET pin status will not change when SW takes control, and SW can read register status before deciding to perform further charger/device/accessory detection or USB attach The CHRG_DET pin will be asserted or deasserted depending on the HWDETECT bit setting.	RW	0

5.4.27 POWER_CONTROL_SET

ADDRESS OFFSET	0x3E		
PHYSICAL ADDRESS	0x3E	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the POWER_CONTROL register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
HWDETECT	DP_VSRC_EN	VDAT_DET	DP_WKPU_EN	BVALID_FALL	BVALID_RISE	DET_COMP	SW_CONTROL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	HWDETECT		RW	0
6	DP_VSRC_EN		RW	0
5	VDAT_DET		R	0
4	DP_WKPU_EN		RW	0
3	BVALID_FALL		RW	0
2	BVALID_RISE		RW	0
1	DET_COMP		R	0
0	SW_CONTROL		RW	0

5.4.28 POWER_CONTROL_CLR

ADDRESS OFFSET	0x3F		
PHYSICAL ADDRESS	0x3F	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the POWER_CONTROL register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
HWDETECT	DP_VSRC_EN	VDAT_DET	DP_WKPU_EN	BVALID_FALL	BVALID_RISE	DET_COMP	SW_CONTROL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	HWDETECT		RW	0
6	DP_VSRC_EN		RW	0
5	VDAT_DET		R	0
4	DP_WKPU_EN		RW	0
3	BVALID_FALL		RW	0
2	BVALID_RISE		RW	0
1	DET_COMP		R	0
0	SW_CONTROL		RW	0

5.4.29 VENDOR_SPECIFIC1

ADDRESS OFFSET	0x80		
PHYSICAL ADDRESS	0x80	**INSTANCE**	USB_SCUSB
DESCRIPTION	Eye diagram programmability and DP/DM swap control		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	DATAPOLARITY	ZHSDRV		IHSTX			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	DATAPOLARITY	Control data polarity on DP/DM DATAPOLARITY bit will control both DP/DM polarity in USB PHY and Charger Detection polarity in active mode but not charger detection in polarity in dead battery condition. 0b: DP & DM polarity is swapped DP is mapped to C1 pin, DM mapped to D1 pin 1b: DP & DM polarity is not swapped DP is mapped to D1 pin, DM mapped to C1 pin as described in Terminal description chapter	RW	1
5:4	ZHSDRV	High speed output impedance configuration for eye diagram tuning : 00 45.455 Ω 01 43.779 Ω 10 42.793 Ω 11 42.411 Ω	RW	0x0
3:0	IHSTX	High speed output drive strength configuration for eye diagram tuning : 0000 17.928 mA 0001 18.117 mA 0010 18.306 mA 0011 18.495 mA 0100 18.683 mA 0101 18.872 mA 0110 19.061 mA 0111 19.249 mA 1000 19.438 mA 1001 19.627 mA 1010 19.816 mA 1011 20.004 mA 1100 20.193 mA 1101 20.382 mA 1110 20.570 mA 1111 20.759 mA IHSTX[0] is also the AC BOOST enable IHSTX[0] = 0 → AC BOOST is disabled IHSTX[0] = 1 → AC BOOST is enabled	RW	0x1

5.4.30 VENDOR_SPECIFIC1_SET

ADDRESS OFFSET	0x81		
PHYSICAL ADDRESS	0x81	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as VENDOR_SPECIFIC1 register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATEN CY			

7	6	5	4	3	2	1	0
Reserved	DATAPOLARITY	ZHSDRV		IHSTX			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	DATAPOLARITY		RW	1
5:4	ZHSDRV		RW	0x0
3:0	IHSTX		RW	0x1

5.4.31 VENDOR_SPECIFIC1_CLR

ADDRESS OFFSET	0x82		
PHYSICAL ADDRESS	0x82	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the VENDOR_SPECIFIC1 register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	DATAPOLARITY	ZHSDRV		IHSTX			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	DATAPOLARITY		RW	1
5:4	ZHSDRV		RW	0x0
3:0	IHSTX		RW	0x1

5.4.32 VENDOR_SPECIFIC2_STS

ADDRESS OFFSET	0x83		
PHYSICAL ADDRESS	0x83	**INSTANCE**	USB_SCUSB
DESCRIPTION	Indicates the current value of the interrupt source signal.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
VBUS_MNTR_STS	REG3V3IN_MNTR_STS	SVLDCONWKB_WDOG_STS	ID_FLOAT_STS	ID_RARBRC_STS<1:0>		Reserved	BVALID_STS

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	VBUS_MNTR_STS	Current value of VBUS_MNTR comparator	R	0
6	REG3V3IN_MNTR_STS	Current value of REG3V3IN_MNTR comparator 0: VBAT REG3V3IN_MNTR threshold 1: VBAT REG3V3IN_MNTR threshold	R	0
5	SVLDCONWKB_WDOG_STS	Current value of SVLDCONWKB_WDOG status. 0: Watchdog timer has not expired 1: Watchdog timer has expired	R	0
4	ID_FLOAT_STS	Current value of ID_FLOAT detection on ID pin 0: If RID_FLOAT not detected 1: If RID_FLOAT detected	R	0
3:2	ID_RARBRC_STS<1:0>	ACA Detection status output 00: ACA not detected 01: R_ID_A resistance on ID detected 10: R_ID_B resistance on ID detected 11: R_ID_C resistance on ID detected	R	0x0
1	Reserved		R	0
0	BVALID_STS	Current value of VB_SESS_VLD output	R	0

5.4.33 VENDOR_SPECIFIC2_LATCH

ADDRESS OFFSET	0x84		
PHYSICAL ADDRESS	0x84	**INSTANCE**	USB_SCUSB
DESCRIPTION	These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial mode is entered regardless of the value of ClockSuspendM. The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit.		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
VBUS_MNTR_LATCH	REG3V3IN_MNTR_LATCH	SVLDCONWKB_WDOG _LATCH	ID_FLOAT_LATCH	ID_RARBRC_LATCH<1:0>		Reserved	BVALID_LATCH

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	VBUS_MNTR_LATCH	Set to '1' when an unmasked event occurs on VBUS_MNTR comparator Clear on read register.	R	0
6	REG3V3IN_MNTR_LATCH	Set to '1' when an unmasked event occurs on REG3V3IN_MNTR. comparator Clear on read register.	R	0
5	SVLDCONWKB_WDOG _LATCH	Set to '1' when an unmasked event occurs on SVLDCONWKB_WDOG,that is,, when watchdog counter has expired. Clear on read register.	R	0
4	ID_FLOAT_LATCH	Set to '1' when an unmasked event occurs on ID_FLOAT detection. Clear on read register.	R	0
3:2	ID_RARBRC_LATCH<1:0>	Set according to table below when an unmasked event occurs on ACA Detection status output 00: No ACA event detected 01: ACA event. Detected 10: ACA event. Detected 11: ACA event. Detected	R	0x0
1	Reserved		R	0
0	BVALID_LATCH	Set to '1' when an unmasked event occurs on VB_SESS_VLD comparator. Clear on read register.	R	0

5.4.34 VENDOR_SPECIFIC3

ADDRESS OFFSET	0x85		
PHYSICAL ADDRESS	0x85	**INSTANCE**	USB_SCUSB
DESCRIPTION			
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	CHGD_IDP_SRC_EN _EN	IDPULLUP_WK_EN	SW_USB_DET	DATA_CONTACT_DET_EN	REG3V3_VSEL<2:0>		

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved	Software must not set this bit	RW	0
6	CHGD_IDP_SRC_EN	Enable IDP_SRC on DP and RDM_DWN on DM.Can be used to perform data contact detect (Used when manual control over the charger detection is needed.) When SW_CONTROL=0 this bit is Read-only and gives the status of IDP_SRC control signal in charger detection FSM. When SW_CONTROL=1, this bit is Read/Write: 0b: IDP_SRC on DP and RDM_DWN on DM are disabled. 1b: IDP_SRC on DP and RDM_DWN on DM are enabled Note: Conflict resolution case: If DP_VSRC_EN = 1 at the same time as this bit is set, then IDP_SRC on DP and RDM_DWN on DM are disabled, (and VDPSRC will remain enabled).	RW	0
5	IDPULLUP_WK_EN	Enable of sampling of ID line with RID_WK_PU. This bit is ignored when IDPULLUP = 1 Refer to IDPULLUP bit description 0b: Disable sampling of ID line 1b: Enable sampling of the ID line with custom RID_UP_WK	RW	0
4	SW_USB_DET	Battery Charger Detection state-machine enable bit 0b: Disable Battery Charger Detection State machine 1b: Enable Battery Charger Detection State-machine if SW_CONTROL = 0 Note: This bit is automatically set to 1 by hardware during Dead Battery Detection. When the chip is powered up and enters ACTIVE mode this bit can be read to check if Charger Detection FSM is active. Setting this bit to 0 will stop Battery Charger Detection that was initiated during Dead Battery Condition. This bit is reset automatically when SW_CONTROL bit is 1. This bit is reset to 0 by RESETN pin This bit will also be reset to 0 if SVLDCONWKB_CNTR timeout occurs. Software must then write this bit to 1 to reenable Battery Charger Detection state-machine if required.	RW	0
3	DATA_CONTACT_DET_EN	If state-machine is enabled in active mode (through SW_USB_DET bit above) and this bit is set to 1, then Data Contact Detection will be enabled in the charger detection state-machine. This optional feature is disabled by default.	RW	0
2:0	REG3V3_VSEL<2:0>	When 000 REG3V3 = 2.5 V When 001 REG3V3 = 2.75 V When 010 REG3V3 = 3.0 V When 011 REG3V3 = 3.10 V (default) When 100 REG3V3 = 3.20 V When 101 REG3V3 = 3.30 V When 110 REG3V3 = 3.40 V When 111 REG3V3 = 3.50 V	RW	0x3

5.4.35 VENDOR_SPECIFIC3_SET

ADDRESS OFFSET	0x86		
PHYSICAL ADDRESS	0x86	**INSTANCE**	USB_SCUSB
DESCRIPTION			
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	CHGD_IDP_SRC_EN	IDPULLUP_WK_EN	SW_USB_DET	DATA_CONTACT_DET_EN	REG3V3_VSEL<2:0>		

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	CHGD_IDP_SRC_EN		RW	0
5	IDPULLUP_WK_EN		RW	0
4	SW_USB_DET		RW	0
3	DATA_CONTACT_DET_EN		RW	0
2:0	REG3V3_VSEL<2:0>		RW	0x3

5.4.36 VENDOR_SPECIFIC3_CLR

ADDRESS OFFSET	0x87		
PHYSICAL ADDRESS	0x87	**INSTANCE**	USB_SCUSB
DESCRIPTION			
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	CHGD_IDP_SRC_EN	IDPULLUP_WK_EN	SW_USB_DET	DATA_CONTACT_DET_EN	REG3V3_VSEL<2:0>		

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	CHGD_IDP_SRC_EN		RW	0
5	IDPULLUP_WK_EN		RW	0
4	SW_USB_DET		RW	0
3	DATA_CONTACT_DET_EN		RW	0
2:0	REG3V3_VSEL<2:0>		RW	0x3

5.4.37 VENDOR_SPECIFIC4

ADDRESS OFFSET	0x88		
PHYSICAL ADDRESS	0x88	**INSTANCE**	USB_SCUSB
DESCRIPTION	Charger Detection SERX Status and PSW,VBUS ext resistor configuration register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	ACA_DET_EN	RABUSIN_EN	R1KSERIES	PSW_OSOD	PSW_CMOS	CHGD_SERX_DP	CHGD_SERX_DM

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	ACA_DET_EN	This bit is used to enable Accessory Charger Adapter (ACA) detection in Battery Charger State-Machine in active-mode	RW	1
5	RABUSIN_EN	This bit is used modify VBUS resistance to ground. 0: A-Device VBUS resistor RVBUS_IDLE_A is disabled. VBUS resistance to ground becomes RVBUS_IDLE_B (see **Section 4.18**) 1: A-Device VBUS resistor RVBUS_IDLE_A is enabled (see **Section 4.18**)	RW	1
4	R1KSERIES	This bit is used to indicate to TUSB1211 whether an external series 1kohm resistor is connected on VBUS. When this bit is set internal VBUS comparator thresholds are adjusted so they remain in spec. 0: No external series resistor on VBUS 1: An external 1=kΩ series resistor is connected on VBUS	RW	1
3	PSW_OSOD	This bit controls PSW pin configuration. It can be overridden by PSW_CMOS bit below ‘0’: PSW pad is in OS mode (active high) ‘1’: PSW pad is in OD mode (active low)	RW	0
2	PSW_CMOS	This bit controls PSW pin configuration. It overrides PSW_OSOD bit above. ‘0’ : PSW pad is in OD or OS mode (controlled by PSW_OD bit) ‘1’: PSW pad is in CMOS mode	RW	0x0

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
1	CHGD_SERX_DP	Read-only status bit showing status of debounced charger detection single-ended receiver comparator on DP 0: VDP < [0.8V : 2.0V] SERX threshold 1: VDP > [0.8V : 2.0V] SERX threshold Note: This comparator and status bit is enabled automatically in the following scenarios: • When charger detection FSM is enabled and VDP_SRC or IDP_SRC are enabled by FSM • When SW_CONTROL=1 and DP_VSRC_EN =1 • When SW_CONTROL=1 and CHGD_IDP_SRC_EN=1 • When DP_WKPU_EN bit is enabled In all other cases (including when DP 1.5K pullup is enabled by SW for CDP/DCP/SDP differentiation after SW charger detection step) this status bit should be ignored and LINESTATE<1:0> bits in DEBUG register, or RXCMD should be used for DP/DM detection	R	0x0
0	CHGD_SERX_DM	Read-only status bit showing status of debounced charger detection single-ended receiver comparator on DM 0: VDM < [0.8V : 2.0V] SERX threshold 1: VDM > [0.8V : 2.0V] SERX threshold Note: This comparator and status bit is enabled automatically in the following scenarios: • When charger detection FSM is enabled and VDP_SRC or IDP_SRC are enabled by FSM • When SW_CONTROL=1 and DP_VSRC_EN =1 • When SW_CONTROL=1 and CHGD_IDP_SRC_EN=1 • When DP_WKPU_EN bit is enabled In all other cases (including when DP 1.5K pullup is enabled by SW for CDP/DCP/SDP differentiation after SW charger detection step) this status bit should be ignored and LINESTATE<1:0> bits in DEBUG register, or RXCMD should be used for DP/DM detection	R	0x0

5.4.38 VENDOR_SPECIFIC4_SET

ADDRESS OFFSET	0x89		
PHYSICAL ADDRESS	0x89	**INSTANCE**	USB_SCUSB
DESCRIPTION	Charger Detection SERX Status and PSW,VBUS ext resistor configuration register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	ACA_DET_EN	RABUSIN_EN	R1KSERIES	PSW_OSOD	PSW_CMOS	CHGD_SERX_DP	CHGD_SERX_DM

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	ACA_DET_EN		RW	1
5	RABUSIN_EN		RW	1
4	R1KSERIES		RW	1
3	PSW_OSOD		RW	0
2	PSW_CMOS		RW	0x0
1	CHGD_SERX_DP		R	0x0
0	CHGD_SERX_DM		R	0x0

5.4.39 VENDOR_SPECIFIC4_CLR

ADDRESS OFFSET	0x8A		
PHYSICAL ADDRESS	0x8A	**INSTANCE**	USB_SCUSB
DESCRIPTION	Charger Detection SERX Status and PSW,VBUS ext resistor configuration register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	ACA_DET_EN	RABUSIN_EN	R1KSERIES	PSW_OSOD	PSW_CMOS	CHGD_SERX_DP	CHGD_SERX_DM

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	ACA_DET_EN		RW	1
5	RABUSIN_EN		RW	1
4	R1KSERIES		RW	1
3	PSW_OSOD		RW	0
2	PSW_CMOS		RW	0x0
1	CHGD_SERX_DP		R	0x0
0	CHGD_SERX_DM		R	0x0

5.4.40 VENDOR_SPECIFIC5

ADDRESS OFFSET	0x8B		
PHYSICAL ADDRESS	0x8B	**INSTANCE**	USB_SCUSB
DESCRIPTION	Vendor-specific interrupt enable register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	AUTORESUME_WDOG_EN	ID_FLOAT_EN	ID_RES_EN	SVLDCONWKB_WDOG _EN	VBUS_MNTR_RISE_EN	VBUS_MNTR_FALL_EN	REG3V3IN_MNTR_EN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	AUTORESUME_WDOG_EN	Autoresume watchdog timer enable bit 0b: Disable the Autoresume watchdog timer 1b: Enable the Autoresume watchdog timer Timer is be initialized and starts counting when the PHY detects a resume-K.	RW	1
5	ID_FLOAT_EN	When set to '1', it enables RX CMD's for high to low or low to high transitions on ID_FLOAT.	RW	0
4	ID_RES_EN	When set to '1', this bit enables RX CMD's for high to low or low to high transitions on detection of ACA resistors RID_A , RID_B or RID_C . When this bit is set to '1' and any of the above ACA resistors are detected, TUSB1211 will send an RX CMD to the link with the alt_int bit set to 1b. The status of ACA detection can then be read back through status bits ID_RARBRC_STS <1:0> Setting this bit also forces ID pull-up (RID_UP) to be enabled irrespective of IDPULLUP bit setting	RW	0
3	SVLDCONWKB_WDOG _EN	Generate an interrupt event notification when SVLDCONWKB_WDOG watchdog timer times out Note SVLDCONWKB_WDOG watchdog timer is enabled and disabled separately, see Section 5.3.12 for more details.	RW	0
2	VBUS_MNTR_RISE_EN	Generate an interrupt event notification when VBUS_MNTR changes from low to high.	RW	0
1	VBUS_MNTR_FALL_EN	Generate an interrupt event notification when VBUS_MNTR changes from high to low.	R	0
0	REG3V3IN_MNTR_EN	Optional feature which can be used to indicate to Link if VBAT level is high enough to guarantee USB functionality 0b: Disable this monitoring featue 1b: Enable monitoring of REG3V3IN (=VBAT) level through RXCMD on detection of high to low or low to high transitions on comparator REG3V3IN_MNTR after debounce.	R	0

5.4.41 VENDOR_SPECIFIC5_SET

ADDRESS OFFSET	0x8C		
PHYSICAL ADDRESS	0x8C	**INSTANCE**	USB_SCUSB
DESCRIPTION	Vendor-specific interrupt set register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	AUTORESUME_WDOG_EN	ID_FLOAT_EN	ID_RES_EN	SVLDCONWKB_WDOG _EN	VBUS_MNTR_RISE_EN	VBUS_MNTR_FALL_EN	REG3V3IN_MNTR_EN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	AUTORESUME_WDOG_EN		RW	1
5	ID_FLOAT_EN		RW	0
4	ID_RES_EN		RW	0
3	SVLDCONWKB_WDOG _EN		RW	0
2	VBUS_MNTR_RISE_EN		RW	0
1	VBUS_MNTR_FALL_EN		RW	0
0	REG3V3IN_MNTR_EN		RW	0

5.4.42 VENDOR_SPECIFIC5_CLR

ADDRESS OFFSET	0x8D		
PHYSICAL ADDRESS	0x8D	**INSTANCE**	USB_SCUSB
DESCRIPTION	Vendor-specific interrupt clear register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	AUTORESUME_WDOG_EN	ID_FLOAT_EN	ID_RES_EN	SVLDCONWKB_WDOG _EN	VBUS_MNTR_RISE_EN	VBUS_MNTR_FALL_EN	REG3V3IN_MNTR_EN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	AUTORESUME_WDOG_EN		RW	1
5	ID_FLOAT_EN		RW	0
4	ID_RES_EN		RW	0
3	SVLDCONWKB_WDOG _EN		RW	0
2	VBUS_MNTR_RISE_EN		RW	0
1	VBUS_MNTR_FALL_EN		RW	0
0	REG3V3IN_MNTR_EN		RW	0

5.4.43 VENDOR_SPECIFIC6

ADDRESS OFFSET	0x8E		
PHYSICAL ADDRESS	0x8E	**INSTANCE**	USB_SCUSB
DESCRIPTION	SOF and ACA CFG Register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
ACA_RID_B_CFG	ACA_RID_A_CFG	SOF_EN	Reserved				

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	ACA_RID_B_CFG	This bit is used to enable correct configuration of TUSB1211 as a B-device with ACA connected and nothing (or A-device OFF) at ACA Accessory port and charger present on ACA Charger Port, if ACA RID_B is detected on ID pin. It impacts: a) VA_VBUS_VLD in RX CMD b) VSESS_VLD in RX CMD c) VBUS SRP When this bit is‘1’ and RID_B is detected on ID pin , then mask VBUS plug detection information from being sent to the link, and mask OTG VBUS SRP commands (CHRGVBUS, DISCHRGVBUS bits) from the link. Set VA_VBUS_VLD =0 and VSESS_VLD =0 in RX CMD, and disable RB_SRP_UP, RB_SRP_DWN Note: CHRGVBUS, DISCHRGVBUS register bit settings themselves are unchanged but VBUS SRP pullup and pulldown are disabled. When this bit is ‘0’ RID_B detection has no impact on VA_VBUS_VLD detection and VA_SESS_VLD detection in RX CMD	RW	0
6	ACA_RID_A_CFG	This bit is used to enable correct configuration of TUSB1211 as an A-device with ACA connected and B-device at ACA Accessory port and charger connected to Charger Port , if ACA RID_A is detected on ID pin. It impacts: a) IDGND detection in RXCMD and b) Enabling of external VBUS on PSW pin When this bit is ‘1’ and RID_A is detected on ID pin then TUSB1211 will be configured as an A-device by set ID=0 in RXCMD (equivalent to IDGND detected). In addition PSW pin is deasserted to avoid contention on VBUS pin since the charger at ACA port already provides VBUS. When this bit is ‘0’ RID_A detection has no impact on RXCMD nor PSW pin	RW	0
5	SOF_EN	USB HS Start-of-Frame clock output feature enable 0: Disable HS SOF clock 1: Enable HS SOF clock output on SOF pin HS USB SOF packet rate is 8kHz	RW	0
4:0	Reserved		RW	0

5.4.44 VENDOR_SPECIFIC6_SET

ADDRESS OFFSET	0x8F		
PHYSICAL ADDRESS	0x8F	**INSTANCE**	USB_SCUSB
DESCRIPTION	SOF and ACA CFG Register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
ACA_RID_B_CFG	ACA_RID_A_CFG	SOF_EN	Reserved				

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	ACA_RID_B_CFG		RW	0
6	ACA_RID_A_CFG		RW	0
5	SOF_EN		RW	0
4:0	Reserved		RW	0

5.4.45 VENDOR_SPECIFIC6_CLR

ADDRESS OFFSET	0x90		
PHYSICAL ADDRESS	0x90	**INSTANCE**	USB_SCUSB
DESCRIPTION	SOF and ACA CFG Register		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
ACA_RID_B_CFG	ACA_RID_A_CFG	SOF_EN	Reserved				

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	ACA_RID_B_CFG		RW	0
6	ACA_RID_A_CFG		RW	0
5	SOF_EN		RW	0
4:0	Reserved		RW	0

6 Application, Implementation, and Layout

NOTE

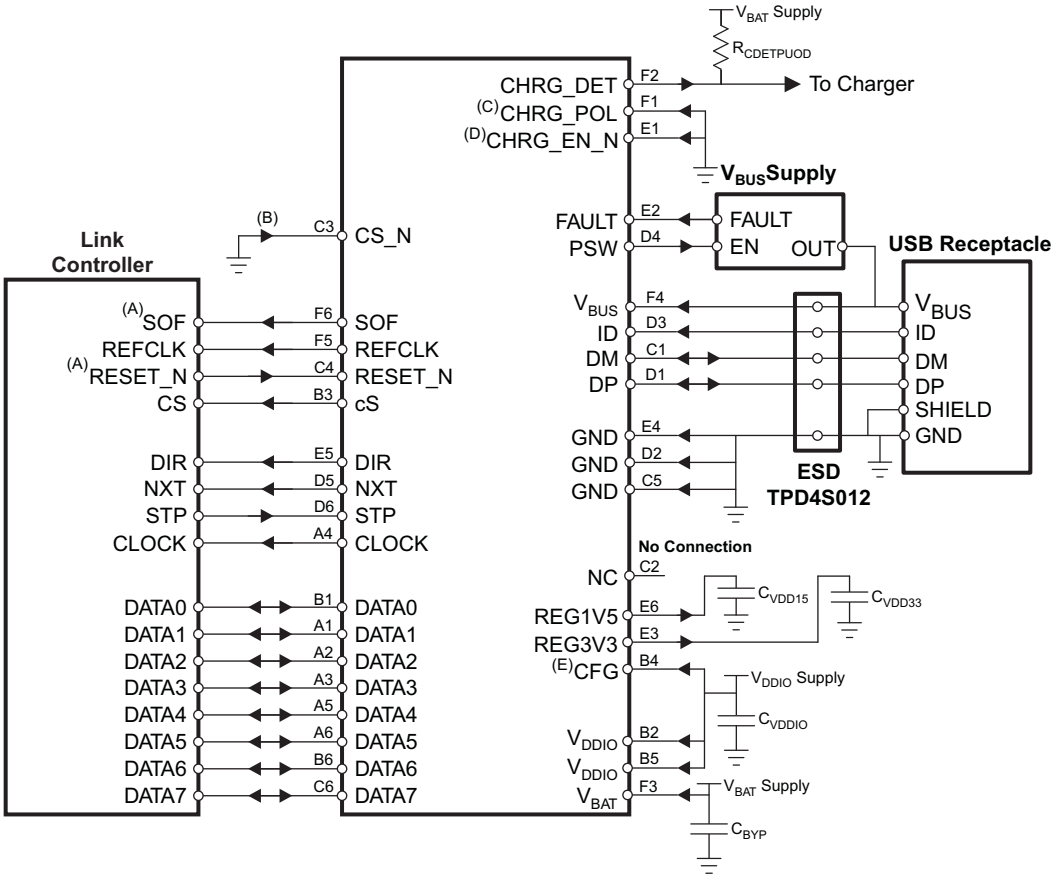
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

Figure 6-1 shows the suggested application diagram (host or OTG, ULPI output-clock mode).

The TUSB1211 is a USB2.0 transceiver chip, designed to interface with a USB controller through a ULPI interface. The device supports all USB2.0 data rates (high-speed, full-speed, and low-speed) and it is compliant to both host and peripheral (OTG) modes. Use Section 6.2.1 and Section 6.2.2 to select the wished operation mode. This section presents a simplified discussion of the design process.

6.2 Typical Application



A. Optional: SOF (open if unused); RESET_N (tie to V_{DDIO} if unused)
B. Link controls chip select through CS pin with CS_N at GND. Alternatively, Link may control CS_N pin with CS pin tied to V_{DDIO}.
C. CHRG_DET is active-low (tie CHRG_POL to V_{BAT} for CHRG_DET active high).
D. Dead battery charger detection is enabled (tie CHRG_EN_N to V_{BAT} to disable).
E. CFG tied to V_{DDIO} for 26 MHz input at REFCLK (tie to GND for 19.2 MHz).

Figure 6-1. USB-OTG With ULPI Output Clock

6.2.1 Design Requirements

Table 6-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VBAT	3.3 V
VDDIO	1.8 V
VBUS	5 V
USB Support	HS, FS, LS
USB Battery Charger Detection	Yes
USB On the Go (OTG)	Yes
Clock sources	26 MHz or 19.2 MHz oscillator

6.2.2 Detailed Design Procedure

Connect the TUSB12111 device as is shown in the suggested application diagram, Figure 6-1. Follow the Board Guidelines of the Application Report, *TUSB121x USB2.0 Board Guidelines* (SWCA124)

Table 6-2. External Components

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE
VDDIO	Capacitor	CVDDIO.IN	100 nF	Suggested value, application dependent
REG3V3	Capacitor	CREG3V3	2.2 µF (recommended)	Range: [0.45 µF : 6.5 µF] ESR = [0 : 600 mΩ] for f > 10 kHz
REG1V5	Capacitor	CREG1V5	2.2 µF (recommended)	Range: [0.45 µF : 6.5 µF] ESR = [0 : 600 mΩ] for f > 10 kHz
VBAT	Capacitor	CBYP	2.2 µF (recommended)	Range: [0.45 µF : 6.5 µF] ESR = [0 : 600 mΩ] for f > 10 kHz
VBUS	Capacitor	CVBUS	4.7 µF (recommended)	Place close to USB connector

Table 6-3. V_{BUS} Capacitors

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE
VBUS – HOST	Capacitor	CV_{BUS}	> 120 µF	
VBUS – DEVICE	Capacitor	CV_{BUS}	4.7 µF	Range: 1.0 µF to 10.0 µF
VBUS – OTG	Capacitor	CV_{BUS}	4.7 µF	Range: 1.0 µF to 6.5 µF

6.2.2.1 Unused Pins Connection

- CHRG_DET Output. Leave floating if unused.
- CHRG_POL Input. Tie to GND to make CHRG_DET pin active low if unused.
- CHRG_EN_N Input. Tie to VBAT to disable dead-battery charger detection if unused.
- SOF Output. Leave floating if unused.
- REFCLK Input. If REFCLK is unused, and 60-MHz clock is provided by MODEM (60 MHz should be connected to CLOCK pin in this case) then tie REFCLK to GND.
- CFG tie to GND if REFCLK is 19.2 MHz, or tie to VDDIO if REFCLK is 26 MHz. Tie to either GND or VDDIO (do not care which) if REFCLK not used (that is, ULPI input clock configuration).

6.2.3 Application Curves

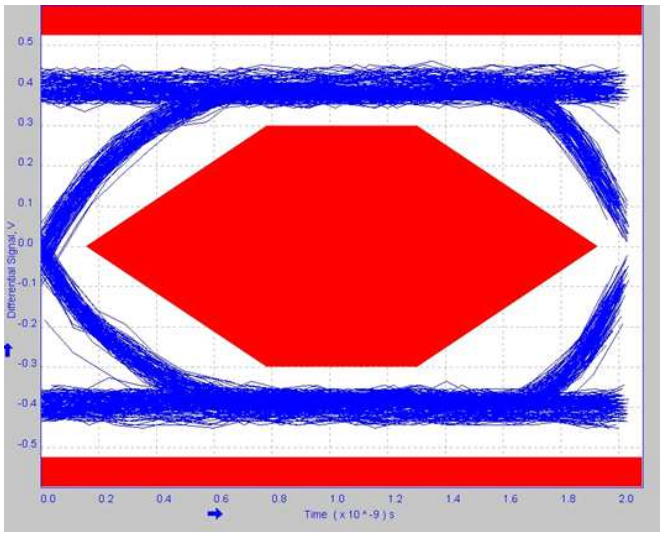


Figure 6-2. High-Speed Eye Diagram

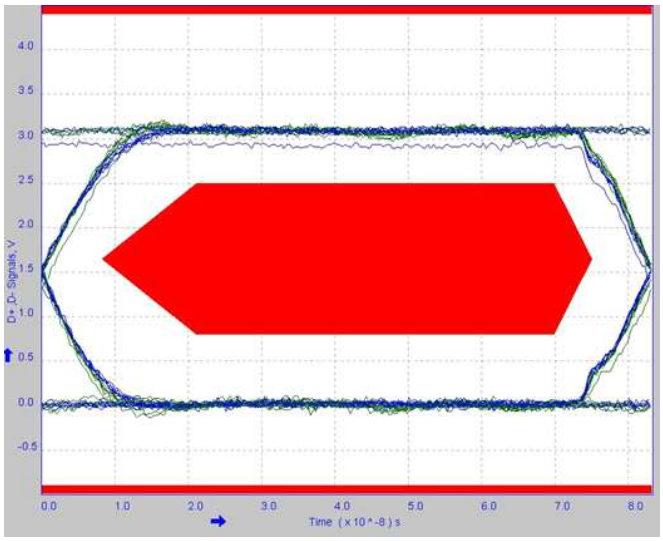


Figure 6-3. Full-Speed Eye Diagram

6.3 Layout

6.3.1 Layout Guidelines

- The VDDIO pins of the TUSB1211 supply 1.8 V (nominal) power to the core of the TUSB1211 device. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The VBAT pin of the TUSB1211 supply 3.3 V (nominal) power rail to the TUSB1211 device. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The VBUS pin of the TUSB1211 supply 5 V (nominal) power rail to the TUSB1211 device. This pin is normally connected to the VBUS pin of the USB connector.
- All power rails require 0.1-µF decoupling capacitors for stability and noise immunity. The smaller decoupling capacitors should be placed as close to the TUSB1211 device power pins as possible with an optimal grouping of two of differing values per pin.

6.3.1.1 Ground

TI recommends using almost one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

6.3.2 Layout Example

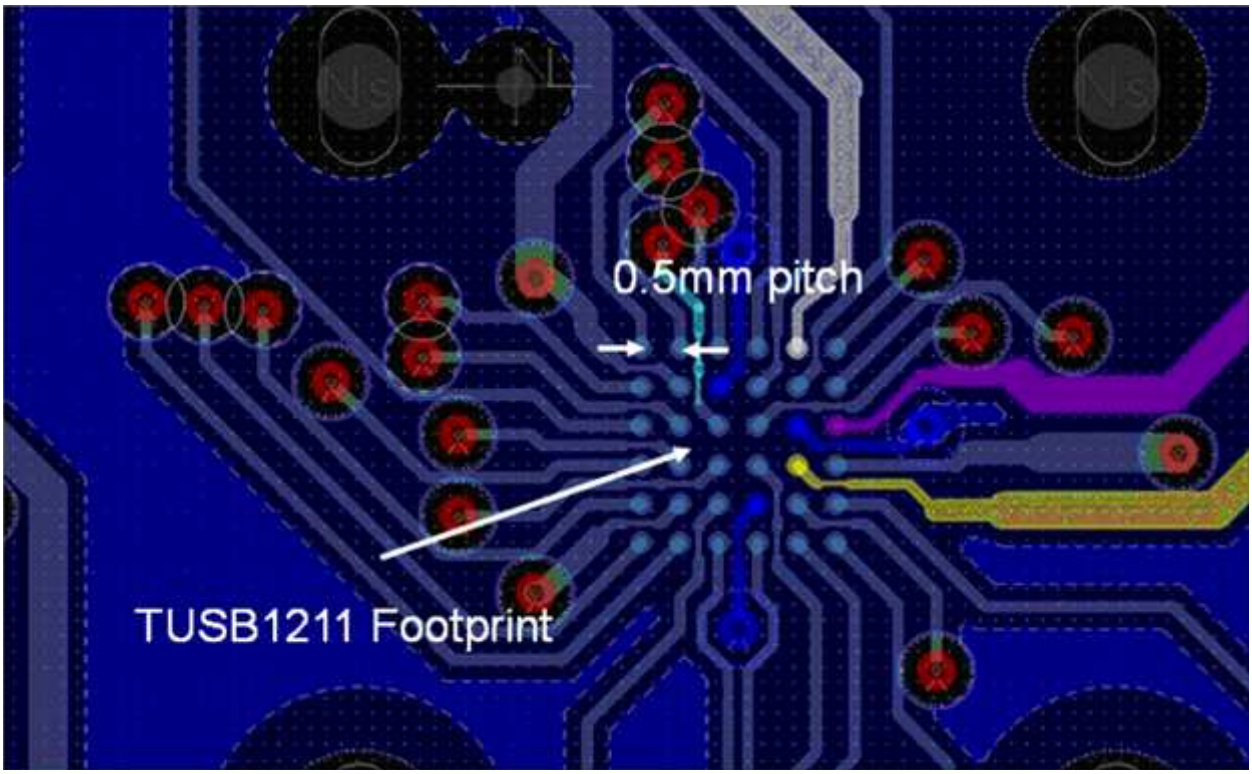


Figure 6-4. TUSB1211 Layout

6.4 Power Supply Recommendations

VBUS, VBAT, and VDDIO are needed for power the TUSB1211 device.

The recommended operation is for VBAT to be present before VDDIO. Applying VDDIO before VBAT to the TUSB1211 device is not recommended because a diode from VDDIO to VBAT will be forward-biased when VDDIO is present but VBAT is not present. TUSB121x does not strictly require VBUS to function.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

See *TUSB121x USB2.0 Board Guidelines* (SWCA124) for a description of the TUSB1211 board guidelines.

7.1.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB1211A1ZRQ	ACTIVE	BGA MICROSTAR JUNIOR	ZRQ	36	490	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	1211A1	Samples
TUSB1211A1ZRQR	ACTIVE	BGA MICROSTAR JUNIOR	ZRQ	36	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	1211A1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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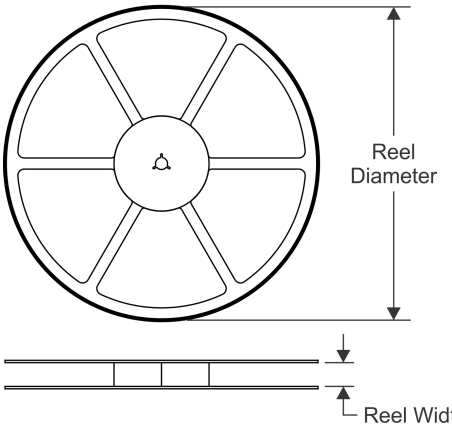
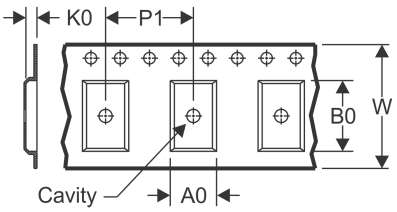
TAPE AND REEL INFORMATION

REEL DIMENSIONS

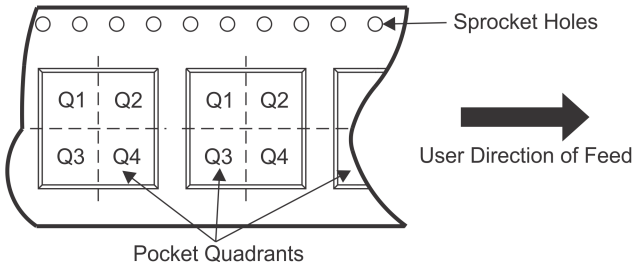


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

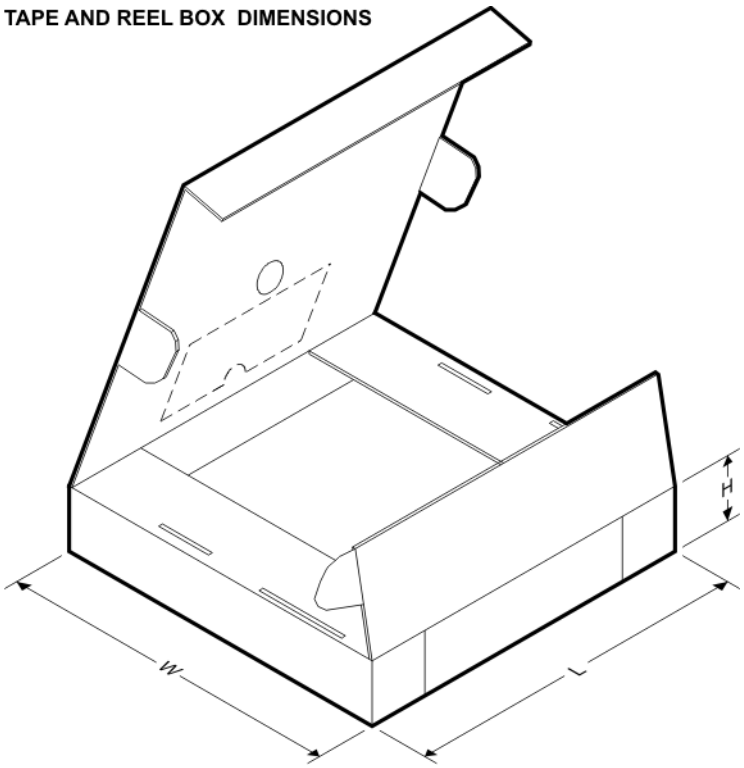
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1211A1ZRQR	BGA MICROSTAR JUNIOR	ZRQ	36	1500	330.0	12.4	3.7	3.7	1.4	8.0	12.0	Q1

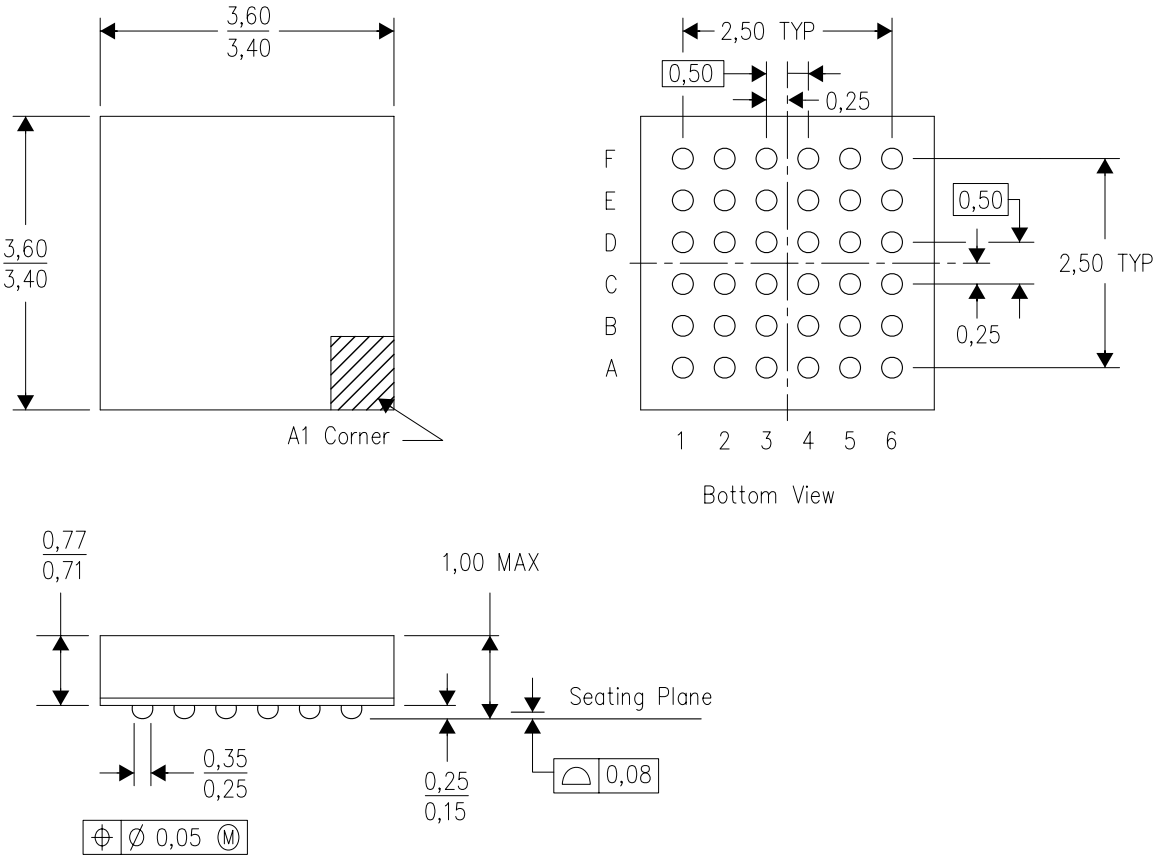
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1211A1ZRQR	BGA MICROSTAR JUNIOR	ZRQ	36	1500	336.6	336.6	31.8

ZRQ (S–PBGA–N36) PLASTIC BALL GRID ARRAY



4210358/A 07/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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