4/3/2/1-Phase PWM Controller for High-Density Power Supply

General Description

The RT8841 is a 4/3/2/1-phase synchronous buck controller with 2 integrated MOSFET drivers for VR11 CPU power application. RT8841 uses differential inductor DCR current sense to achieve phase current balance and active voltage positioning. Other features include adjustable operating frequency, adjustable soft start, power good indication, external error-amp compensation, over voltage protection, over current protection and enable/shutdown for various applications. RT8841 comes to a small footprint with WQFN-40L 6x6 package

Applications

- Desktop CPU Core Power
- Low Voltage, High Current DC/ DC Converter

Ordering Information

RT8841 □ □

Package Type
QW : WQFN-40L 6x6 (W-Type)

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

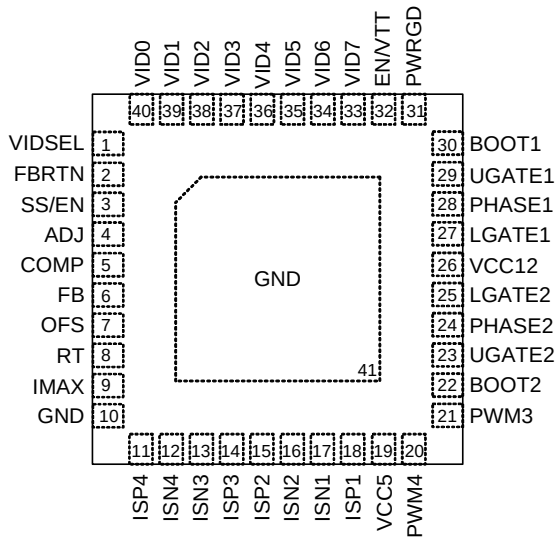
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **12V Power Supply Voltage**
- **4/3/2/1-Phase Power Conversion**
- **2 Embedded MOSFET Drivers**
- **Internal Regulated 5V Output**
- **VID Tables for Intel VRD11/VRD10.x and AMD K8, K8_M2 CPUs**
- **Continuous Differential Inductor DCR Current Sense**
- **Adjustable Soft Start**
- **Adjustable Frequency**
- **Power Good Indication**
- **Adjustable Over Current Protection**
- **Over Voltage Protection**
- **Small 40-Lead WQFN Package**
- **RoHS Compliant and 100% Lead(Pb)-Free**

Pin Configurations

(TOP VIEW)



WQFN-40L 6x6

Typical Application Circuit

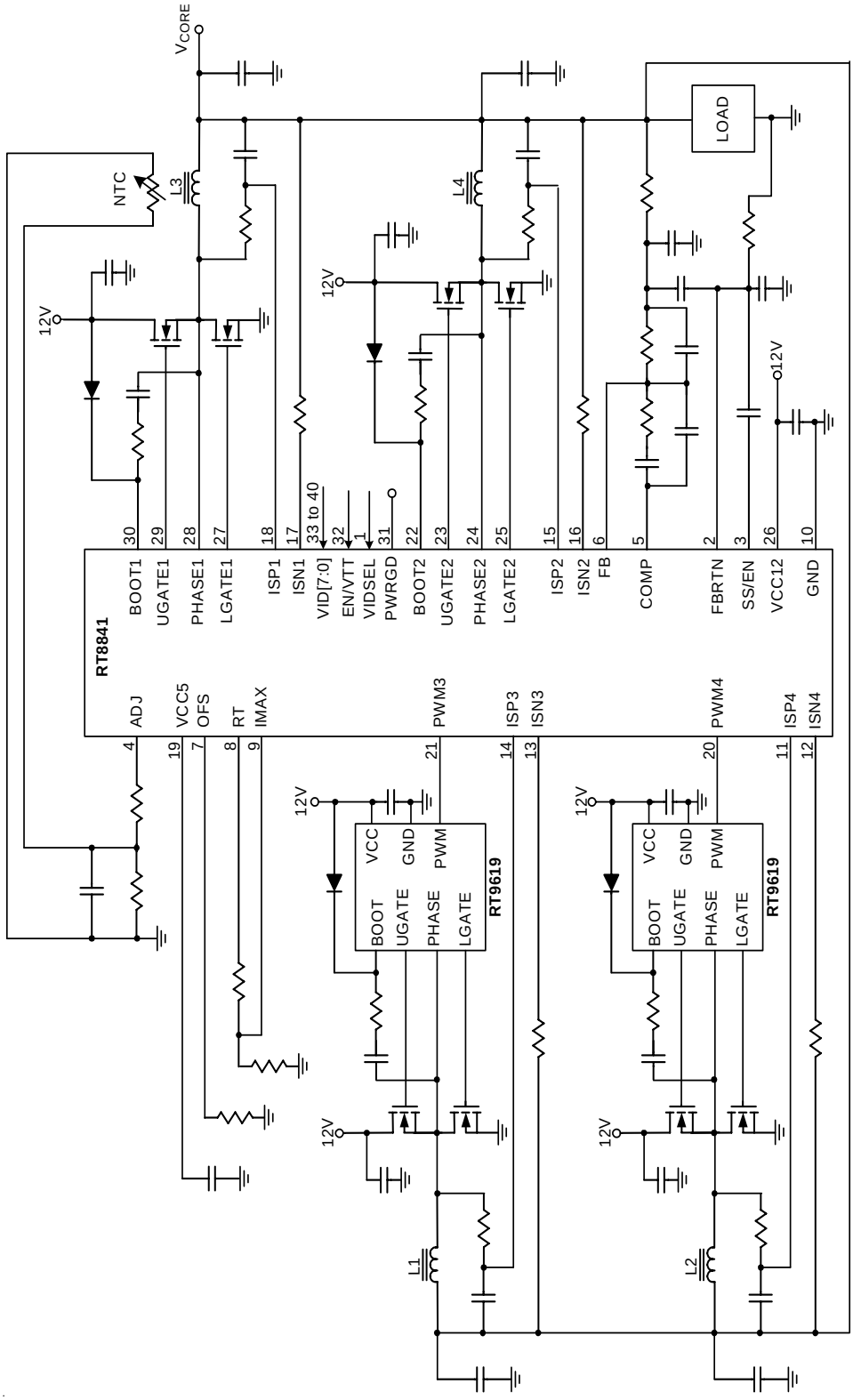


Table 1. Output Voltage Program (VRD10.x + VID6)

Pin Name							Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID5	VID6	
0	1	0	1	0	1	1	1.60000V
0	1	0	1	0	1	0	1.59375V
0	1	0	1	1	0	1	1.58750V
0	1	0	1	1	0	0	1.58125V
0	1	0	1	1	1	1	1.57500V
0	1	0	1	1	1	0	1.56875V
0	1	1	0	0	0	1	1.56250V
0	1	1	0	0	0	0	1.55625V
0	1	1	0	0	1	1	1.55000V
0	1	1	0	0	1	0	1.54375V
0	1	1	0	1	0	1	1.53750V
0	1	1	0	1	0	0	1.53125V
0	1	1	0	1	1	1	1.52500V
0	1	1	0	1	1	0	1.51875V
0	1	1	1	0	0	1	1.51250V
0	1	1	1	0	0	0	1.50625V
0	1	1	1	0	1	1	1.50000V
0	1	1	1	0	1	0	1.49375V
0	1	1	1	1	0	1	1.48750V
0	1	1	1	1	0	0	1.48125V
0	1	1	1	1	1	1	1.47500V
0	1	1	1	1	1	0	1.46875V
1	0	0	0	0	0	1	1.46250V
1	0	0	0	0	0	0	1.45625V
1	0	0	0	0	1	1	1.45000V
1	0	0	0	0	1	0	1.44375V
1	0	0	0	1	0	1	1.43750V
1	0	0	0	1	0	0	1.43125V
1	0	0	0	1	1	1	1.42500V
1	0	0	0	1	1	0	1.41875V
1	0	0	1	0	0	1	1.41250V
1	0	0	1	0	0	0	1.40625V
1	0	0	1	0	1	1	1.40000V
1	0	0	1	0	1	0	1.39375V
1	0	0	1	1	0	1	1.38750V
1	0	0	1	1	0	0	1.38125V
1	0	0	1	1	1	1	1.37500V
1	0	0	1	1	1	0	1.36875V
1	0	1	0	0	0	1	1.36250V

To be continued

Table 1. Output Voltage Program (VRD10.x + VID6)

Pin Name							Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID5	VID6	
1	0	1	0	0	0	0	1.35625V
1	0	1	0	0	1	1	1.35000V
1	0	1	0	0	1	0	1.34375V
1	0	1	0	1	0	1	1.33750V
1	0	1	0	1	0	0	1.33125V
1	0	1	0	1	1	1	1.32500V
1	0	1	0	1	1	0	1.31875V
1	0	1	1	0	0	1	1.31250V
1	0	1	1	0	0	0	1.30625V
1	0	1	1	0	1	1	1.30000V
1	0	1	1	0	1	0	1.29375V
1	0	1	1	1	0	1	1.28750V
1	0	1	1	1	0	0	1.28125V
1	0	1	1	1	1	1	1.27500V
1	0	1	1	1	1	0	1.26875V
1	1	0	0	0	0	1	1.26250V
1	1	0	0	0	0	0	1.25625V
1	1	0	0	0	1	1	1.25000V
1	1	0	0	0	1	0	1.24375V
1	1	0	0	1	0	1	1.23750V
1	1	0	0	1	0	0	1.23125V
1	1	0	0	1	1	1	1.22500V
1	1	0	0	1	1	0	1.21875V
1	1	0	1	0	0	1	1.21250V
1	1	0	1	0	0	0	1.20625V
1	1	0	1	0	1	1	1.20000V
1	1	0	1	0	1	0	1.19375V
1	1	0	1	1	0	1	1.18750V
1	1	0	1	1	0	0	1.18125V
1	1	0	1	1	1	1	1.17500V
1	1	0	1	1	1	0	1.16875V
1	1	1	0	0	0	1	1.16250V
1	1	1	0	0	0	0	1,15625V
1	1	1	0	0	1	1	1.15000V
1	1	1	0	0	1	0	1.14375V
1	1	1	0	1	0	1	1.13750V
1	1	1	0	1	0	0	1.13125V
1	1	1	0	1	1	1	1.12500V
1	1	1	0	1	1	0	1.11875V

To be continued

Table 1. Output Voltage Program (VRD10.x + VID6)

Pin Name							Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID5	VID6	
1	1	1	1	0	0	1	1.11250V
1	1	1	1	0	0	0	1.10625V
1	1	1	1	0	1	1	1.10000V
1	1	1	1	0	1	0	1.09375V
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750V
0	0	0	0	0	0	0	1.08125V
0	0	0	0	0	1	1	1.07500V
0	0	0	0	0	1	0	1.06875V
0	0	0	0	1	0	1	1.06250V
0	0	0	0	1	0	0	1.05625V
0	0	0	0	1	1	1	1.05000V
0	0	0	0	1	1	0	1.04375V
0	0	0	1	0	0	1	1.03750V
0	0	0	1	0	0	0	1.03125V
0	0	0	1	0	1	1	1.02500V
0	0	0	1	0	1	0	1.01875V
0	0	0	1	1	0	1	1.01250V
0	0	0	1	1	0	0	1.00625V
0	0	0	1	1	1	1	1.00000V
0	0	0	1	1	1	0	0.99375V
0	0	1	0	0	0	1	0.98750V
0	0	1	0	0	0	0	0.98125V
0	0	1	0	0	1	1	0.97500V
0	0	1	0	0	1	0	0.96875V
0	0	1	0	1	0	1	0.96250V
0	0	1	0	1	0	0	0.95625V
0	0	1	0	1	1	1	0.95000V
0	0	1	0	1	1	0	0.94375V
0	0	1	1	0	0	1	0.93750V
0	0	1	1	0	0	0	0.93125V
0	0	1	1	0	1	1	0.92500V
0	0	1	1	0	1	0	0.91875V
0	0	1	1	1	0	1	0.91250V
0	0	1	1	1	0	0	0.90625V
0	0	1	1	1	1	1	0.90000V

To be continued

Table 1. Output Voltage Program (VRD10.x + VID6)

Pin Name							Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID5	VID6	
0	0	1	1	1	1	0	0.89375V
0	1	0	0	0	0	1	0.88750V
0	1	0	0	0	0	0	0.88125V
0	1	0	0	0	1	1	0.87500V
0	1	0	0	0	1	0	0.86875V
0	1	0	0	1	0	1	0.86250V
0	1	0	0	1	0	0	0.85625V
0	1	0	0	1	1	1	0.85000V
0	1	0	0	1	1	0	0.84375V
0	1	0	1	0	0	1	0.83750V
0	1	0	1	0	0	0	0.83125V

Note: (1) 0 : Connected to GND
(2) 1 : Open

Table 2. Output Voltage Program (VRD11)

Pin Name								Nominal Output Voltage
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	DACOUT
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000V
0	0	0	0	0	0	1	1	1.59375V
0	0	0	0	0	1	0	0	1.58750V
0	0	0	0	0	1	0	1	1.58125V
0	0	0	0	0	1	1	0	1.57500V
0	0	0	0	0	1	1	1	1.56875V
0	0	0	0	1	0	0	0	1.56250V
0	0	0	0	1	0	0	1	1.55625V
0	0	0	0	1	0	1	0	1.55000V
0	0	0	0	1	0	1	1	1.54375V
0	0	0	0	1	1	0	0	1.53750V
0	0	0	0	1	1	0	1	1.53125V
0	0	0	0	1	1	1	0	1.52500V
0	0	0	0	1	1	1	1	1.51875V
0	0	0	1	0	0	0	0	1.51250V
0	0	0	1	0	0	0	1	1.50625V
0	0	0	1	0	0	1	0	1.50000V
0	0	0	1	0	0	1	1	1.49375V
0	0	0	1	0	1	0	0	1.48750V
0	0	0	1	0	1	0	1	1.48125V
0	0	0	1	0	1	1	0	1.47500V
0	0	0	1	0	1	1	1	1.46875V
0	0	0	1	1	0	0	0	1.46250V
0	0	0	1	1	0	0	1	1.45625V
0	0	0	1	1	0	1	0	1.45000V
0	0	0	1	1	0	1	1	1.44375V
0	0	0	1	1	1	0	0	1.43750V
0	0	0	1	1	1	0	1	1.43125V
0	0	0	1	1	1	1	0	1.42500V
0	0	0	1	1	1	1	1	1.41875V
0	0	1	0	0	0	0	0	1.41250V
0	0	1	0	0	0	0	1	1.40625V
0	0	1	0	0	0	1	0	1.40000V
0	0	1	0	0	0	1	1	1.39375V
0	0	1	0	0	1	0	0	1.38750V
0	0	1	0	0	1	0	1	1.38125V
0	0	1	0	0	1	1	0	1.37500V
0	0	1	0	0	1	1	1	1.36875V

To be continued

Table 2. Output Voltage Program (VRD11)

Pin Name								Nominal Output Voltage
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	DACOUT
0	0	1	0	1	0	0	0	1.36250V
0	0	1	0	1	0	0	1	1.35625V
0	0	1	0	1	0	1	0	1.35000V
0	0	1	0	1	0	1	1	1.34375V
0	0	1	0	1	1	0	0	1.33750V
0	0	1	0	1	1	0	1	1.33125V
0	0	1	0	1	1	1	0	1.32500V
0	0	1	0	1	1	1	1	1.31875V
0	0	1	1	0	0	0	0	1.31250V
0	0	1	1	0	0	0	1	1.30625V
0	0	1	1	0	0	1	0	1.30000V
0	0	1	1	0	0	1	1	1.29375V
0	0	1	1	0	1	0	0	1.28750V
0	0	1	1	0	1	0	1	1.28125V
0	0	1	1	0	1	1	0	1.27500V
0	0	1	1	0	1	1	1	1.26875V
0	0	1	1	1	0	0	0	1.26250V
0	0	1	1	1	0	0	1	1.25625V
0	0	1	1	1	0	1	0	1.25000V
0	0	1	1	1	0	1	1	1.24375V
0	0	1	1	1	1	0	0	1.23750V
0	0	1	1	1	1	0	1	1.23125V
0	0	1	1	1	1	1	0	1.22500V
0	0	1	1	1	1	1	1	1.21875V
0	1	0	0	0	0	0	0	1.21250V
0	1	0	0	0	0	0	1	1.20625V
0	1	0	0	0	0	1	0	1.20000V
0	1	0	0	0	0	1	1	1.19375V
0	1	0	0	0	1	0	0	1.18750V
0	1	0	0	0	1	0	1	1.18125V
0	1	0	0	0	1	1	0	1.17500V
0	1	0	0	0	1	1	1	1.16875V
0	1	0	0	1	0	0	0	1.16250V
0	1	0	0	1	0	0	1	1.15625V
0	1	0	0	1	0	1	0	1.15000V
0	1	0	0	1	0	1	1	1.14375V
0	1	0	0	1	1	0	0	1.13750V
0	1	0	0	1	1	0	1	1.13125V
0	1	0	0	1	1	1	0	1.12500V
0	1	0	0	1	1	1	1	1.11875V

To be continued

Table 2. Output Voltage Program (VRD11)

Pin Name								Nominal Output Voltage
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	DACOUT
0	1	0	1	0	0	0	0	1.11250V
0	1	0	1	0	0	0	1	1.10625V
0	1	0	1	0	0	1	0	1.10000V
0	1	0	1	0	0	1	1	1.09375V
0	1	0	1	0	1	0	0	1.08750V
0	1	0	1	0	1	0	1	1.08125V
0	1	0	1	0	1	1	0	1.07500V
0	1	0	1	0	1	1	1	1.06875V
0	1	0	1	1	0	0	0	1.06250V
0	1	0	1	1	0	0	1	1.05625V
0	1	0	1	1	0	1	0	1.05000V
0	1	0	1	1	0	1	1	1.04375V
0	1	0	1	1	1	0	0	1.03750V
0	1	0	1	1	1	0	1	1.03125V
0	1	0	1	1	1	1	0	1.02500V
0	1	0	1	1	1	1	1	1.01875V
0	1	1	0	0	0	0	0	1.01250V
0	1	1	0	0	0	0	1	1.00625V
0	1	1	0	0	0	1	0	1.00000V
0	1	1	0	0	0	1	1	0.99375V
0	1	1	0	0	1	0	0	0.98750V
0	1	1	0	0	1	0	1	0.98125V
0	1	1	0	0	1	1	0	0.97500V
0	1	1	0	0	1	1	1	0.96875V
0	1	1	0	1	0	0	0	0.96250V
0	1	1	0	1	0	0	1	0.95625V
0	1	1	0	1	0	1	0	0.95000V
0	1	1	0	1	0	1	1	0.94375V
0	1	1	0	1	1	0	0	0.93750V
0	1	1	0	1	1	0	1	0.93125V
0	1	1	0	1	1	1	0	0.92500V
0	1	1	0	1	1	1	1	0.91875V
0	1	1	1	0	0	0	0	0.91250V
0	1	1	1	0	0	0	1	0.90625V
0	1	1	1	0	0	1	0	0.90000V
0	1	1	1	0	0	1	1	0.89375V
0	1	1	1	0	1	0	0	0.88750V
0	1	1	1	0	1	0	1	0.88125V
0	1	1	1	0	1	1	0	0.87500V
0	1	1	1	0	1	1	1	0.86875V

To be continued

Table 2. Output Voltage Program (VRD11)

Pin Name								Nominal Output Voltage
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	DACOUT
0	1	1	1	1	0	0	0	0.86250V
0	1	1	1	1	0	0	1	0.85625V
0	1	1	1	1	0	1	0	0.85000V
0	1	1	1	1	0	1	1	0.84375V
0	1	1	1	1	1	0	0	0.83750V
0	1	1	1	1	1	0	1	0.83125V
0	1	1	1	1	1	1	0	0.82500V
0	1	1	1	1	1	1	1	0.81875V
1	0	0	0	0	0	0	0	0.81250V
1	0	0	0	0	0	0	1	0.80625V
1	0	0	0	0	0	1	0	0.80000V
1	0	0	0	0	0	1	1	0.79375V
1	0	0	0	0	1	0	0	0.78750V
1	0	0	0	0	1	0	1	0.78125V
1	0	0	0	0	1	1	0	0.77500V
1	0	0	0	0	1	1	1	0.76875V
1	0	0	0	1	0	0	0	0.76250V
1	0	0	0	1	0	0	1	0.75625V
1	0	0	0	1	0	1	0	0.75000V
1	0	0	0	1	0	1	1	0.74375V
1	0	0	0	1	1	0	0	0.73750V
1	0	0	0	1	1	0	1	0.73125V
1	0	0	0	1	1	1	0	0.72500V
1	0	0	0	1	1	1	1	0.71875V
1	0	0	1	0	0	0	0	0.71250V
1	0	0	1	0	0	0	1	0.70625V
1	0	0	1	0	0	1	0	0.70000V
1	0	0	1	0	0	1	1	0.69375V
1	0	0	1	0	1	0	0	0.68750V
1	0	0	1	0	1	0	1	0.68125V
1	0	0	1	0	1	1	0	0.67500V
1	0	0	1	0	1	1	1	0.66875V
1	0	0	1	1	0	0	0	0.66250V
1	0	0	1	1	0	0	1	0.65625V
1	0	0	1	1	0	1	0	0.65000V
1	0	0	1	1	0	1	1	0.64375V
1	0	0	1	1	1	0	0	0.63750V
1	0	0	1	1	1	0	1	0.63125V
1	0	0	1	1	1	1	0	0.62500V
1	0	0	1	1	1	1	1	0.61875V

To be continued

Table 2. Output Voltage Program (VRD11)

Pin Name								Nominal Output Voltage
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	DACOUT
1	0	1	0	0	0	0	0	0.61250V
1	0	1	0	0	0	0	1	0.60625V
1	0	1	0	0	0	1	0	0.60000V
1	0	1	0	0	0	1	1	0.59375V
1	0	1	0	0	1	0	0	0.58750V
1	0	1	0	0	1	0	1	0.58125V
1	0	1	0	0	1	1	0	0.57500V
1	0	1	0	0	1	1	1	0.56875V
1	0	1	0	1	0	0	0	0.56250V
1	0	1	0	1	0	0	1	0.55625V
1	0	1	0	1	0	1	0	0.55000V
1	0	1	0	1	0	1	1	0.54375V
1	0	1	0	1	1	0	0	0.53750V
1	0	1	0	1	1	0	1	0.53125V
1	0	1	0	1	1	1	0	0.52500V
1	0	1	0	1	1	1	1	0.51875V
1	0	1	1	0	0	0	0	0.51250V
1	0	1	1	0	0	0	1	0.50625V
1	0	1	1	0	0	1	0	0.50000V
1	0	1	1	0	0	1	1	X
1	0	1	1	0	1	0	0	X
1	0	1	1	0	1	0	1	X
1	0	1	1	0	1	1	0	X
1	0	1	1	0	1	1	1	X
1	0	1	1	1	0	0	0	X
1	0	1	1	1	0	0	1	X
1	0	1	1	1	0	1	0	X
1	0	1	1	1	0	1	1	X
1	0	1	1	1	1	0	0	X
1	0	1	1	1	1	0	1	X
1	0	1	1	1	1	1	0	X
1	0	1	1	1	1	1	1	X
1	1	0	0	0	0	0	0	X
1	1	0	0	0	0	0	1	X
1	1	0	0	0	0	1	0	X
1	1	0	0	0	0	1	1	X
1	1	0	0	0	1	0	0	X
1	1	0	0	0	1	0	1	X
1	1	0	0	0	1	1	0	X
1	1	0	0	0	1	1	1	X

To be continued

Table 2. Output Voltage Program (VRD11)

Pin Name								Nominal Output Voltage
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	DACOUT
1	1	0	0	1	0	0	0	X
1	1	0	0	1	0	0	1	X
1	1	0	0	1	0	1	0	X
1	1	0	0	1	0	1	1	X
1	1	0	0	1	1	0	0	X
1	1	0	0	1	1	0	1	X
1	1	0	0	1	1	1	0	X
1	1	0	0	1	1	1	1	X
1	1	0	1	0	0	0	0	X
1	1	0	1	0	0	0	1	X
1	1	0	1	0	0	1	0	X
1	1	0	1	0	0	1	1	X
1	1	0	1	0	1	0	0	X
1	1	0	1	0	1	0	1	X
1	1	0	1	0	1	1	0	X
1	1	0	1	0	1	1	1	X
1	1	0	1	1	0	0	0	X
1	1	0	1	1	0	0	1	X
1	1	0	1	1	0	1	0	X
1	1	0	1	1	0	1	1	X
1	1	0	1	1	1	0	0	X
1	1	0	1	1	1	0	1	X
1	1	0	1	1	1	1	0	X
1	1	0	1	1	1	1	1	X
1	1	1	0	0	0	0	0	X
1	1	1	0	0	0	0	1	X
1	1	1	0	0	0	1	0	X
1	1	1	0	0	0	1	1	X
1	1	1	0	0	1	0	0	X
1	1	1	0	0	1	0	1	X
1	1	1	0	0	1	1	0	X
1	1	1	0	0	1	1	1	X
1	1	1	0	1	0	0	0	X
1	1	1	0	1	0	0	1	X
1	1	1	0	1	0	1	0	X
1	1	1	0	1	0	1	1	X
1	1	1	0	1	1	0	0	X
1	1	1	0	1	1	0	1	X
1	1	1	0	1	1	1	0	X
1	1	1	0	1	1	1	1	X

To be continued

Table 2. Output Voltage Program (VRD11)

Pin Name								Nominal Output Voltage
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	DACOUT
1	1	1	1	0	0	0	0	X
1	1	1	1	0	0	0	1	X
1	1	1	1	0	0	1	0	X
1	1	1	1	0	0	1	1	X
1	1	1	1	0	1	0	0	X
1	1	1	1	0	1	0	1	X
1	1	1	1	0	1	1	0	X
1	1	1	1	0	1	1	1	X
1	1	1	1	1	0	0	0	X
1	1	1	1	1	0	0	1	X
1	1	1	1	1	0	1	0	X
1	1	1	1	1	0	1	1	X
1	1	1	1	1	1	0	0	X
1	1	1	1	1	1	0	1	X
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Note: (1) 0 : Connected to GND
(2) 1 : Open
(3) X : Don't Care

Table 3. Output Voltage Program (K8)

VID4	VID3	VID2	VID1	VID0	Nominal Output Voltage DACOUT
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.200
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

Note: (1) 0 : Connected to GND
(2) 1 : Open

Table 4. Output Voltage Program (K8_M2)

Pin Name						Nominal Output Voltage DACOUT
VID5	VID4	VID3	VID2	VID1	VID0	
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500
0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500

To be continued

Table 4. Output Voltage Program (K8_M2)

Pin Name						Nominal Output Voltage DACOUT
VID5	VID4	VID3	VID2	VID1	VID0	
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

Note: (1) 0 : Connected to GND
(2) 1 : Open
(3) The voltage above are load independent for desktop and server platforms. For mobile platforms the voltage above correspond to zero load current.

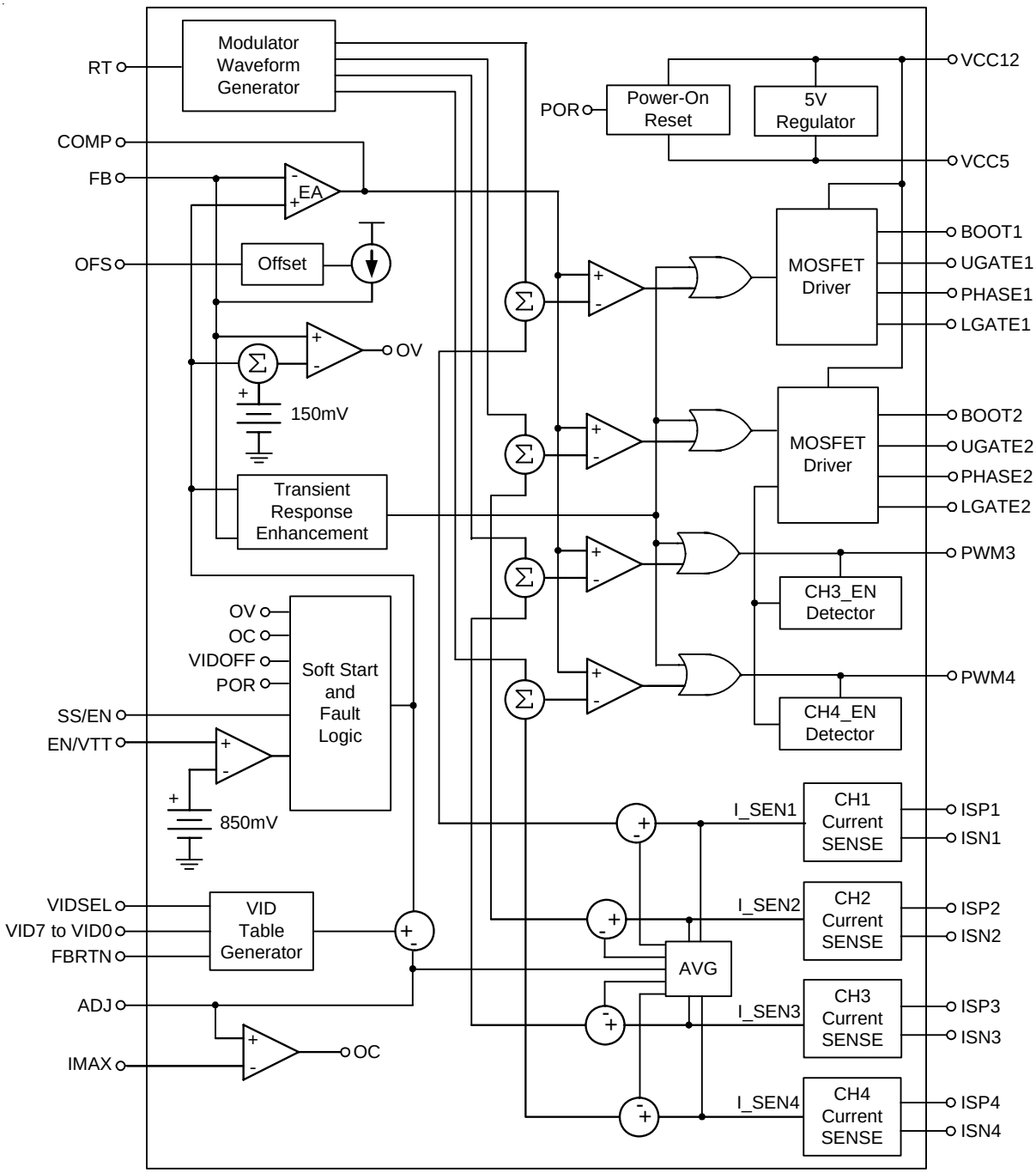
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIDSEL	VID DAC Selection Pin.
2	FBRTN	Negative remote sense pin of output voltage.
3	SS/EN	Connect this pin to GND by a capacitor to adjust soft start time. Pull this pin to GND to disable controller.
4	ADJ	Connect this pin to GND by a resistor to set loadline.
5	COMP	Output of error-amp and input of PWM comparator.
6	FB	Inverting input of error-amp.
7	OFS	Connect this pin to GND by a resistor to set no-load offset voltage.
8	RT	Connect this pin to GND by a resistor to adjust frequency.
9	IMAX	Negative input of OCP comparator. (Positive input of OCP comparator is ADJ).
10	GND	Ground Pin.
11,14,15,18	ISP4, ISP3, ISP2, ISP1	Positive current sense pin of channel 1, 2, 3 and 4.
12,13,16,17	ISN4, ISN3, ISN2, ISN1	Negative current sense pin of channel 1, 2, 3 and 4.
19	VCC5	5V LDO output for system power supply pin.
20,21	PWM4, PWM3	PWM output for channel 4 and channel 3.
22,30	BOOT2, BOOT1	Bootstrap supply for channel 2 and channel 1.
23,29	UGATE2, UGATE1	Upper gate driver for channel 2 and channel 1.
24,28	PHASE2, PHASE1	Switching node of channel 2 and channel 1.
25,27	LGATE2, LGATE1	Lower gate driver for channel 2 and channel 1.
26	VCC12	IC power supply. Connect to 12V.
31	PWRGD	Power good indicator.
32	EN/VTT	VTT voltage detector input.
33 to 40	VID7 to VID0	Voltage identification input for DAC.
41 (Exposed pad)	GND	Exposed pad should be soldered to PCB board and connected to GND.

VID Table Selection

VIDSEL	VID [7]	Table
VTT	X	VR11
GND	X	VR10.x
VCC5	VTT	K8
VCC5	GND	K8_M2

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 15V
- BOOTx to PHASEx ---------- –0.3V to 15V
- BOOTx to GND
  - DC ---------- –0.3V to 30V
  - <200ns ---------- –0.3V to 42V
- PHASEx to GND
  - DC ---------- –2V to 15V
  - <200ns ---------- –5V to 30V
- Input/Output Voltage ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–40L 6x6 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  - WQFN-40L 6x6, θ_{JA} ---------- 36°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC12 ---------- 12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- 0°C to 70°C

Electrical Characteristics

(V_{CC12} = 12V, V_{GND} = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC12 Supply Input						
VCC12 Supply Voltage	V_{VCC12}		10.8	12	13.2	V
VCC12 Supply Current	I_{CC}	No switching	--	6	--	mA
VCC5 power						
VCC5 Supply Voltage	V_{VCC5}	I_{LOAD} = 10mA	4.75	5.0	5.25	V
VCC5 Output Sourcing	I_{VCC5}		10	--	--	mA
Power-On Reset						
VCC12 Rising Threshold	$V_{VCC12TH}$	VCC12 Rising	9.2	9.6	10.0	V
VCC12 Hysteresis	$V_{VCC12HY}$	VCC12 Falling	--	0.9	--	V
EN/VTT						
EN/VTT Rising Threshold	V_{ENVTT}	EN/VTT Rising	0.80	0.85	0.90	V
Enable Hysteresis	$V_{ENVTTHY}$	EN/VTT Falling	--	100	--	mV
Reference Voltage accuracy						
DAC Accuracy		0.8V to 1.6V	–5	--	+5	mV
		0.5V to 0.8V	–8	--	+8	

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier						
DC Gain	A_{DC}	No Load	--	80	--	dB
Gain-Bandwidth	GBW	C_{LOAD} = 10pF	--	10	--	MHz
Slew Rate	SR	C_{LOAD} = 10pF	10	--	--	V/us
Output voltage range	V_{COMP}		0.5		3.6	V
Max Current	I_{EA_SLEW}	Slew	300	--	--	uA
Power Sequence						
PWRGD Low Voltage	V_{PGOOD}	I_{PWRGD} = 4mA	--	--	0.4	V
Soft-Start Delay	T_{D1}		--	2	--	ms
V_{BOOT} Duration	T_{D3}		--	0.8	--	ms
PWRGD Delay	T_{D5}	Measured the time form V_{BOOT} change to PWRGD = 1	--	1.6	--	ms
Current Sense Amplifier						
Max Current	I_{GMMAX}	V_{CSP} = 1.3V Sink Current from CSN	100	--	--	uA
Input Offset Voltage	V_{OSCS}		–1.5	0	1.5	mV
Running Frequency	f_{OSC}	R_{RT} = 40kΩ	270	300	330	kHz
RT Pin Voltage	V_{RT}	R_{RT} = 40kΩ	1.52	1.60	1.68	V
Ramp Amplitude	V_{RAMP}	R_{RT} = 40kΩ	--	1.60	--	V
Soft Start						
Soft Start Current	I_{SS1}	Slew	13	16	19	uA
VID change Current	I_{SS2}	Slew	130	160	190	uA
Gate Driver						
UGATE Drive Source	$R_{UGATEsr}$	BOOT – PHASE = 8V 250mA Source Current	--	1	--	Ω
UGATE Drive Sink	$R_{UGATEsk}$	BOOT – PHASE = 8V 250mA Sink Current	--	1	--	Ω
LGATE Drive Source	$R_{LGATEsr}$	V_{LGATE} = 8V	--	1	--	Ω
LGATE Drive Sink	$R_{LGATEsk}$	250mA Sink Current	--	0.8	--	Ω
Protection						
Over-Voltage Threshold	V_{OVP}	Sweep FB Voltage, $V_{FB,EAP}$	125	150	175	mV
Over-Current Threshold	V_{OCP}	Sweep IMAX Voltage, $V_{IMAX,ADJ}$	–13	0	+13	mV
Dynamic Characteristic						
UGATE Rise Time	t_{rUGATE}	Ciss = 3000p	--	15	--	ns
UGATE Fall Time	t_{fUGATE}		--	10	--	ns
LGATE Rise Time	t_{rLGATE}		--	15	--	ns
LGATE Fall Time	t_{fLGATE}		--	10	--	ns
Input Threshold						
VID7 to VID0, VIDSEL Rising Threshold	$V_{ID7\ to\ 0}$, V_{IDSEL}	VID7 to VID0 Rising, VIDSEL Rising	--	$1/2V_{TT}$ + 12.5mV	--	V
VID7 to VID0, VIDSEL Hysteresis	$V_{ID7\ to\ 0\_Hy}$, V_{IDSEL_Hy}	VID7 to VID0 Falling, VIDSEL Falling	--	25	--	mV

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

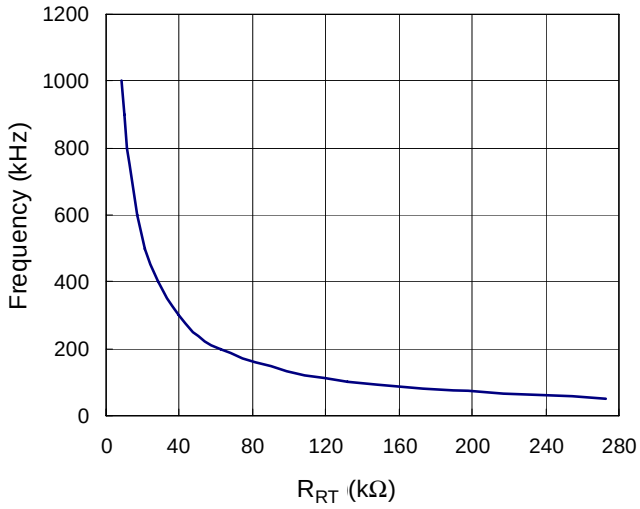
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a effective single layer thermal conductivity test board of JEDEC thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

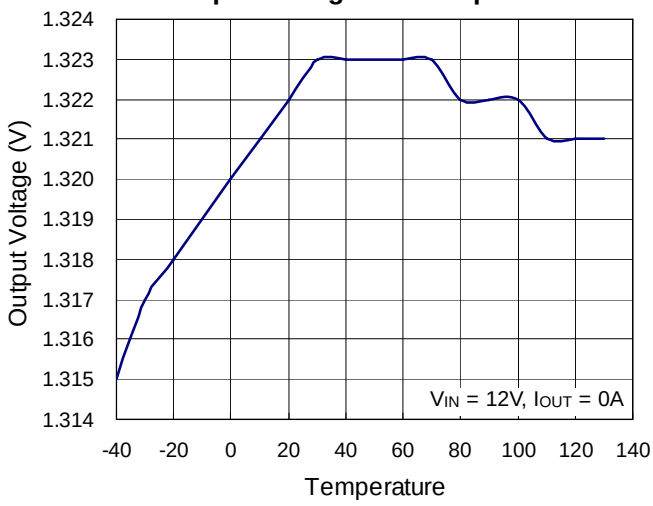
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

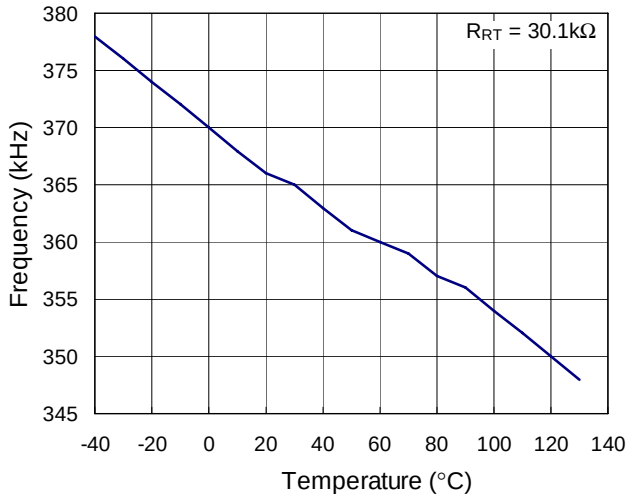
Frequency vs. R_{RT}



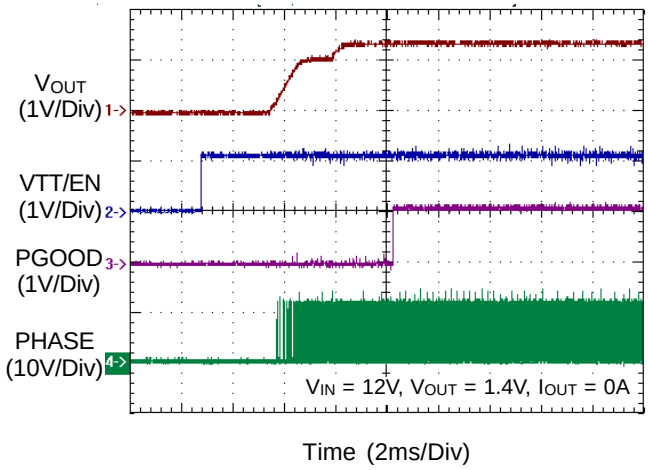
Output Voltage vs. Temperature



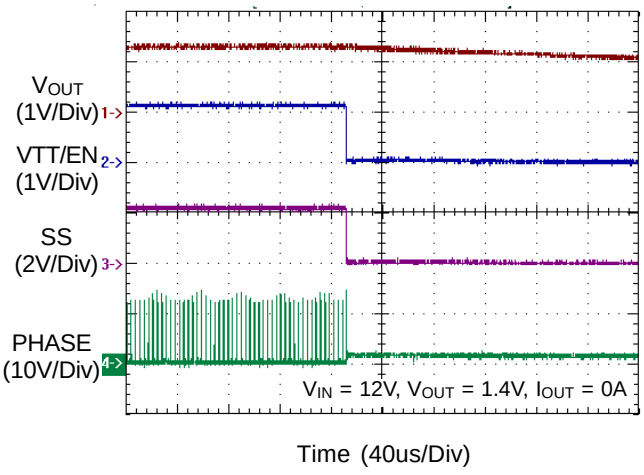
Frequency vs. Temperature



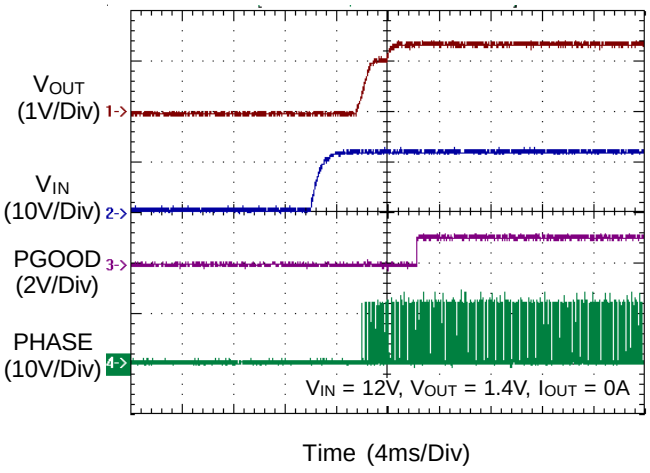
Power On from VTT/EN



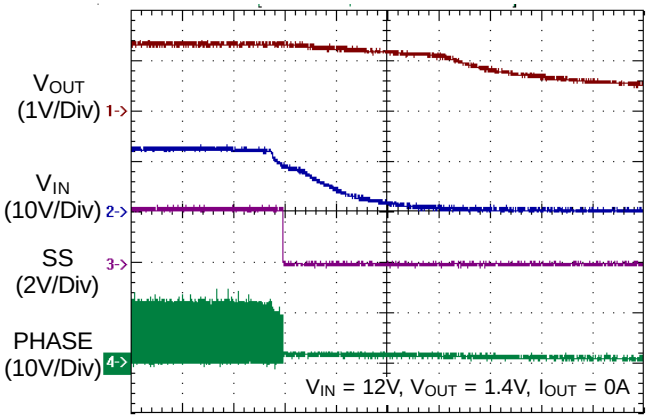
Power Off from VTT/EN



Power On from VIN

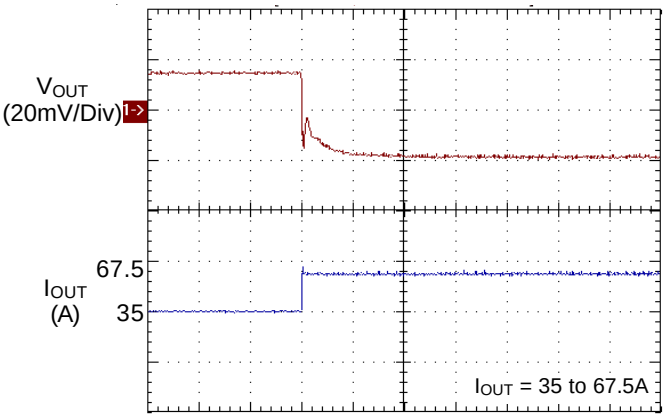


Power Off from VIN



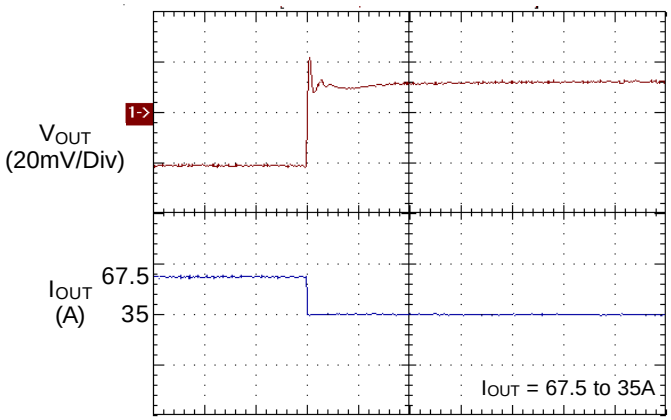
Time (4ms/Div)

ACLL Drop



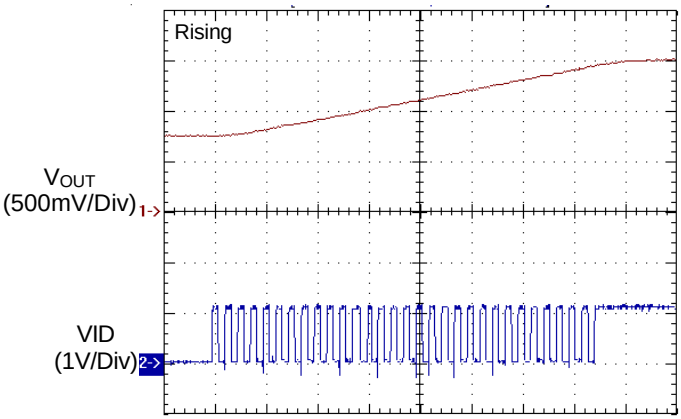
Time (20us/Div)

ACLL Overshoot



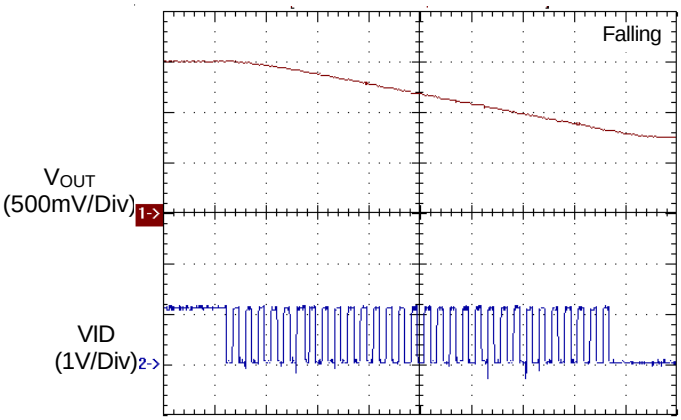
Time (20us/Div)

Dynamic VID



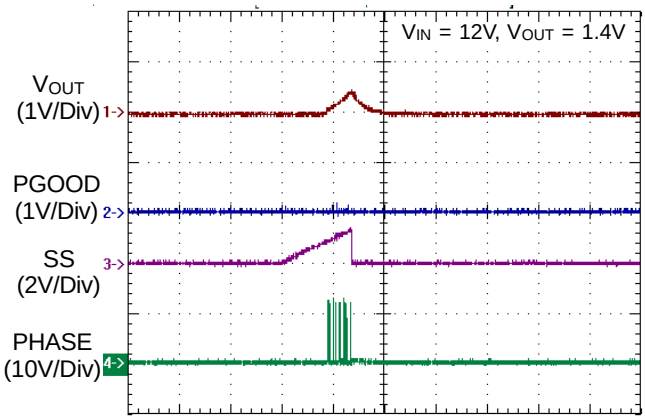
Time (40us/Div)

Dynamic VID



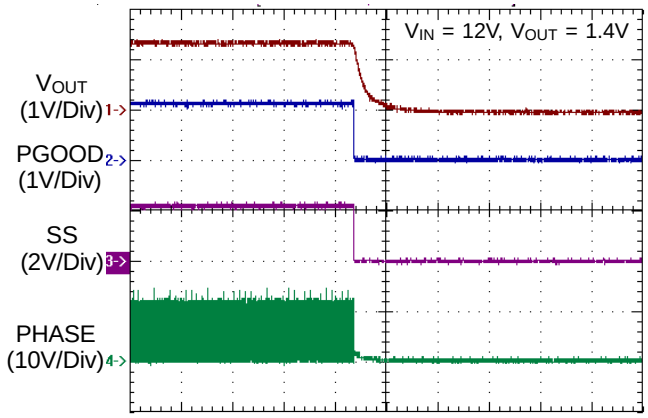
Time (40us/Div)

Output Short then Power On

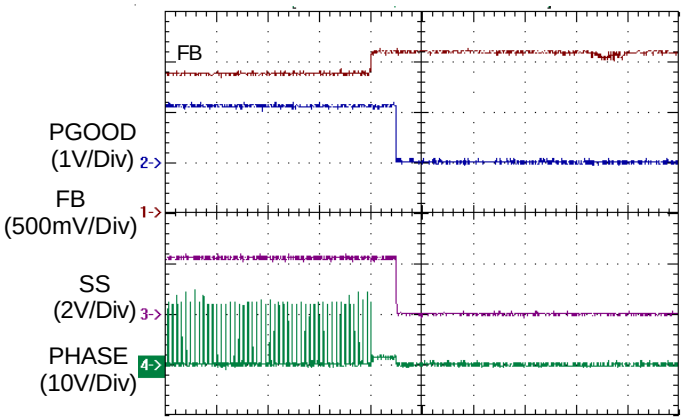


Time (1ms/Div)

Power On then Output Short



OVP



Application Information

RT8841 is a 4/3/2/1-phase synchronous buck DC/DC converter with 2 embedded MOSFET drivers. The internal VID DAC is designed to interface with the Intel 8-bit VR11 compatible CPUs.

Power Ready Detection

During start-up, RT8841 will detect $V_{CC}12$, $V_{CC}5$ and V_{TT}. When $V_{CC}12$ > 9.6V, $V_{CC}5$ > 4.6V and V_{TT} > 0.85V POR will go high. POR (Power On Reset) is the internal signal to indicate all voltage powers are ready to let RT8841 and the companioned MOSFET drivers to work properly. When POR = L, RT8841 will try to turn off both high side and low side MOSFETs.

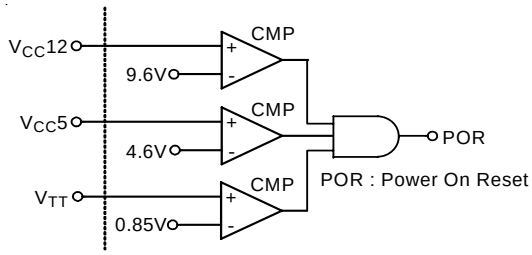


Figure 1. Circuit for Power Ready Detection

Phase Detection

The number of operational phases is determined by the internal circuitry that monitors the ISNx voltages during start up. Normally, the RT8841 operates as a 4-phase PWM controller. Pull ISN4 and ISP4 to $V_{CC}5$ programs 3-phase operation, pull ISN3 and ISP3 to $V_{CC}5$ programs 2-phase operation, and pull ISN2 and ISP2 to $V_{CC}5$ programs 1-phase operation. RT8841 detects the voltage of ISN4, ISN3 and ISN2 at POR rising edge. At the rising edge, RT8841 detects whether the voltage of ISN4, ISN3 and ISN2 are higher than "$V_{CC}5$ – 1V" respectively to decide how many phases should be active. Phase detection is only active during start up. When POR = H, the number of operational phases is determined and latched. The unused PWM pin can be connected to 5V, GND or left open.

Phase Switching Frequency

The phase switching frequency of the RT8841 is set by an external resistor connected from the RT pin to GND. The frequency follows the graph in Figure 2.

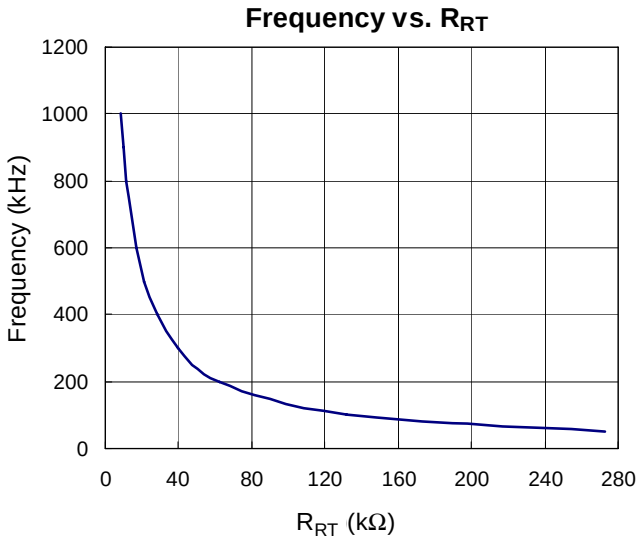


Figure 2. R_{RT} vs Phase Switching Frequency

Soft Start

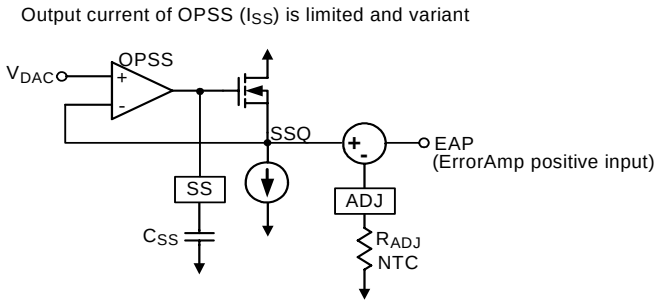


Figure 4. Circuit for Soft Start and Dynamic VID

The V_{OUT} start-up time is set by a capacitor from the SS pin to GND. In power_on_reset state (POR = L), the SS pin is held at GND. After power_on_reset stae (POR = H) and an extra delay 1600us, V_{SS} and V_{SSQ} begin to rise till $V_{SSQ} = V_{BOOT}$. When $V_{SSQ} = V_{BOOT}$, RT8841 stays in this state for 800us waiting for valid VID code sent by CPU. After receiving valid VID code, V_{OUT} continues ramping up or down to the voltage specified by VID code. Before PWRGD = H, output current of OPSS (I_{SS}) is limited to 8uA ($I_{SS}1$). When PWRGD = H, I_{SS} is limited to 80uA ($I_{SS}2$). The soft start waveform is shown in Figure 5.

V_{OUT} will trace V_{EAP} which is equal to "$V_{SSQ} - V_{ADJ}$". V_{ADJ} is a small voltage signal which is proportional to I_{OUT}. This voltage is used to generate loadline and will be described later. T1 is the delay time from power_on_reset state to the beginning of V_{OUT} rising.

$$T1 = 1600\mu s + 0.6V \times C_{SS}/I_{SS}1 \quad (1)$$

T2 is the soft start time from V_{OUT} = 0 to $V_{OUT} = V_{BOOT}$.

$T2 = V_{BOOT} \times C_{SS}/I_{SS}1$ (2)

T3 is the dwelling time for $V_{OUT} = V_{BOOT}$. T3 = 800µs.

T4 is the soft start time from $V_{OUT} = V_{BOOT}$ to $V_{OUT} = V_{DAC}$.

$T4 \sim= |V_{DAC} - V_{BOOT}| \times C_{SS}/I_{SS}1$ (3)

T5 is the power good delay time, T5 ~= 1600µs.

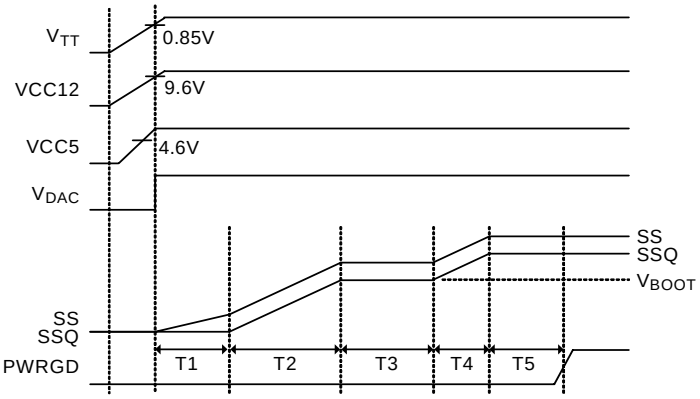


Figure 5. Soft Start Waveforms

Dynamic VID

The RT8841 can accept VID input changing while the controller is running. This allows the output voltage (V_{OUT}) to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under either light or heavy load conditions. The CPU changes the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative. Theoretically, V_{OUT} should follow V_{DAC} which is a staircase waveform. In RT8841, as mentioned in soft start session, V_{DAC} slew rate is limited by $I_{SS}2/C_{SS}$ when PWRGD = H. This slew rate limiter works as a low pass filter of V_{DAC} and makes the bandwidth of V_{DAC} waveform finite. By smoothening V_{DAC} staircase waveform, V_{OUT} will no longer overshoot or undershoot. On the other hand, C_{SS} will increase the settling time of V_{OUT} during VID OTF. In most cases, 1nF to 30nF ceramic capacitor is suitable for C_{SS}.

Output Voltage Differential Sensing

The RT8841 uses differential sensing by a high gain low offset ErrorAmp. The CPU voltage is sensed between the FB and FBRTN pins. A resistor (R_{FB}) connects FB pin and the positive remote sense pin of the CPU (V_{CCP}). FBRTN pin connects to the negative remote sense pin of CPU (V_{CCN}) directly. The ErrorAmp compares EAP (= $V_{DAC} - V_{ADJ}$) with the V_{FB} to regulate the output voltage.

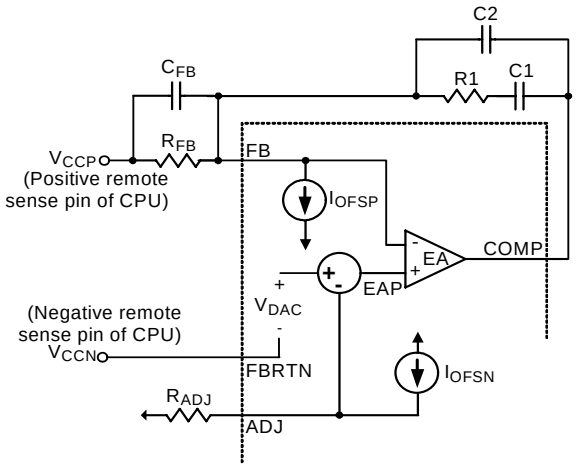


Figure 6. Circuit for V_{OUT} Differential Sensing and No Load Offset

No-Load Offset

In Figure 6, I_{OFSN} or I_{OFSP} are used to generate no-load offset. Either I_{OFSN} or I_{OFSP} is active during normal operation. It should be noted that users can only enable one polarity of no-load offset. Do not connect OFS pin to GND and to V_{CC5} at the same time. Connect a resistor from OFS pin to GND to activate I_{OFSN}. I_{OFSN} flows through R_{ADJ} from ADJ pin to GND. In this case, negative no-load offset voltage (V_{OFSN}) is generated.

$V_{OFSN} = I_{OFSN} \times R_{ADJ} = 0.8 \times R_{ADJ}/R_{OFS}$ (4)

Connect a resistor from OFS pin to $V_{CC}5$ to activate I_{OFSP}. I_{OFSP} flows through R_{FB} from the V_{CCP} to FB pin. In this case, positive no-load offset voltage (V_{OFSP}) is generated.

When positive no-load offset is selected, the RT8841 will generate another internal 8uA current source to eliminate dead zone problem of droop function. This 8uA current will be injected into ADJ resistors, producing a small initial negative no-load offset. Therefore, when OFS pin is connected to VCC5 through a resistor, the positive no-load offset can be calculated as :

$$V_{OFSP} = I_{OFSP} \times R_{FB} - 8uA \times R_{ADJ} = 6.4 \times \frac{R_{FB}}{R_{OFS}} - 8uA \times R_{ADJ} \quad (5)$$

RT8841 provides wide range no-load positive offset for over-clocking applications. The I_{OFSP} capability can supply from 30uA to 640uA, which means in Equation (5), R_{OFS} can range from 240kΩ to 10kΩ. Other resistances of R_{OFS} exceeding this range can also provide no-load positive offset but cannot be guaranteed by Equation (5).

Load Transient Quick Response

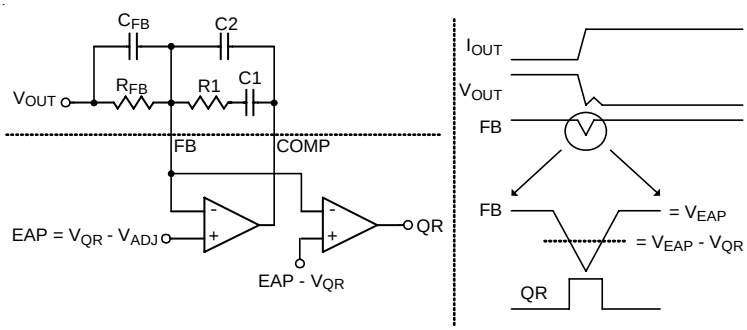


Figure 7. Load Transient Quick Response

In steady state, the voltage of V_{FB} is controlled to be very close to V_{EAP}. While a load step transient from light load to heavy load could cause V_{FB} lower than V_{EAP} by several tens of mV. In prior design, owing to limited control bandwidth, controller is hard to prevent V_{OUT} undershoot during quick load transient from light load to heavy load. RT8841 detects load transient by comparing V_{FB} and V_{EAP}. If V_{FB} suddenly drops below "$V_{EAP} - V_{QR}$", V_{QR} is a predetermined voltage. The quick response indicator QR rises up. When QR = H, RT8841 turns on all high side MOSFETs and turn off all low side MOSFETs. The sensitivity of quick response can be adjusted by the values of C_{FB} and R_{FB}. Smaller R_{FB} and/or larger C_{FB} will make QR easier to be triggered. Figure 7 is the circuit and typical waveforms.

Output Current Sensing

The RT8841 provides low input offset current-sense amplifier (CSA) to monitor the output current of every channel. Output current of CSA (I_X[n]) is used for channel current balance and active voltage position. In this inductor current sensing topology, R_S and C_S must be set according to the equation below :

$L/DCR = R_S \times C_S$

Then the output current of CSA will follow the equation below :

$I_X = [I_L \times DCR - V_{OFS-CSA} + 235n \times (R_{CSP} - R_{CSN})]/R_{CSN}$

235nA is typical value of CSA input offset current. $V_{OFS-CSA}$ is the input offset voltage of CSA. $V_{OFS-CSA}$ of RT8841 is smaller than +/- 1mV. Usually, "$V_{OFS-CSA}$ + 235n x (R_{CSP} – R_{CSN})" is negligible except at very light load and the equation can be simplified as the equation below :

$I_X = I_L \times DCR/R_{CSN}$

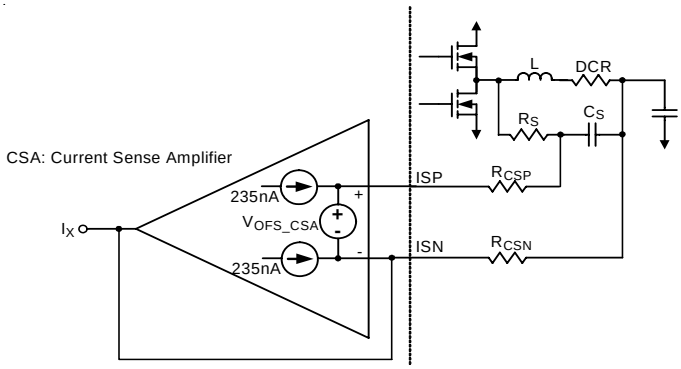


Figure 8. Circuit for Channel Current Sensing

Loadline

Output current of CSA is summed and averaged in RT8841. Then 0.5Σ(I_X[n]) is sent to ADJ pin. Because ΣI_X[n] is a PTC (Positive Temperature Coefficient) current, an NTC (Negative Temperature Coefficient) resistor is needed to connect ADJ pin to GND. If the NTC resistor is properly selected to compensate the temperature coefficient of I_X[n], the voltage on ADJ pin will be proportional to I_{OUT} without temperature effect. In RT8841, the positive input of ErrorAmp is "$V_{DAC} - V_{ADJ}$". V_{OUT} will follow "$V_{DAC} - V_{ADJ}$", too. Thus, the output voltage decreasing linearly with I_{OUT} is obtained. The loadline is defined as

$LL(loadline) = \Delta V_{OUT}/\Delta I_{OUT} = \Delta V_{ADJ}/\Delta I_{OUT}$

$= 0.5 \times DCR \times R_{ADJ}/R_{CSN}$

Briefly, the resistance of R_{ADJ} sets the resistance of loadline. The temperature coefficient of R_{ADJ} compensates the temperature effect of loadline.

Current Balance

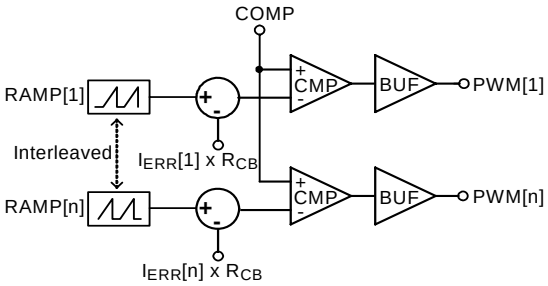


Figure 9. Circuit for Channel Current Balance

In Figure 8, $I_X[n]$ is the current signal which is proportional to current flowing through channel n. In Figure 9, the current error signals $I_{ERR}[n]$ (= $I_X[n]$ – AVG($I_X[n]$)) are used to raise or lower the internal sawtooth waveforms (RAMP[1] to RAMP[n]) which are compared with ErrorAmp output (COMP) to generate PWM signal. The raised sawtooth waveform will decrease the PWM duty of the corresponding channel while the lowered will increase. Eventually, current flowing through each channel will be balanced.

Channel Current Adjust

If channel current is not balanced due to asymmetric PCB layout of power stage, external resistors can be adjusted to correct current imbalance. Figure 10 shows two types of current imbalance, constant ratio type and constant difference type.

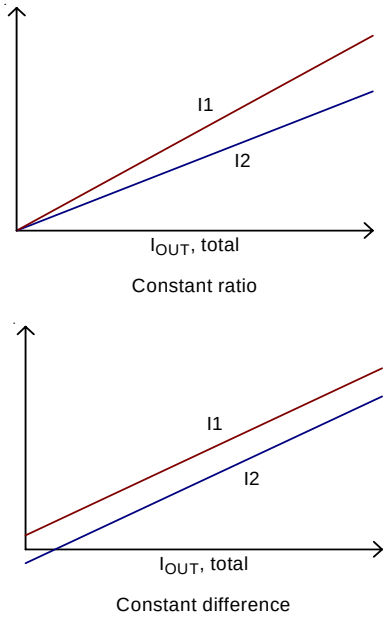


Figure 10. Channel Current vs. Total Current

If the initial current distribution is constant ratio type, according to Equation(8), reduce $R_{CSN}[1]$ can reduce $I_L[1]$ and improve current balance. If the initial current distribution is constant difference type, according to Equation(7), increase $R_{CSP}[1]$ can reduce $I_L[1]$ and improve current balance.

Over Current Protection (OCP)

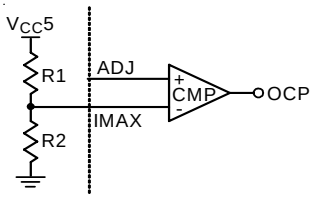


Figure 11. Over Current Protection

In Figure 11, V_{IMAX} is equal to 5V x R2/(R1 + R2). In RT8841, V_{ADJ} is proportional to I_{OUT} and is thermally compensated. Once V_{ADJ} is larger than V_{IMAX}, OCP is triggered and latched. RT8841 will turn off both high side MOSFET and low side MOSFET of all channels. A 20uS delay is used in OCP detection circuit to prevent false trigger.

Over Voltage Protectiom (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds "V_{EAP} + 150mV", OVP is triggered and latched. RT8841 will try to turn on low side MOSFET and turn off high side MOSFET to protect CPU. A 20µs delay is used in OVP detection circuit to prevent false trigger.

Loop Compensation

The RT8841 is a synchronous Buck converter with two control loops : voltage loop and current balance loop. Since the function of the current balance loop is to maintain the current balance between each active channel, its influence to converter stability will be negligible compared with the voltage feedback loop. Therefore, to compensate the voltage loop will be the main task to maintain converter stability.

The converter duty-to-output transfer function G_d is :

$$G_d = \frac{\frac{V_{OUT}}{D}}{1 + \frac{S}{R\sqrt{\frac{L}{C}}} + \frac{S^2}{\left(\frac{1}{\sqrt{LC}}\right)^2}}$$

and the modulator gain of the converter is :

$$F_m = \frac{1}{V_P}$$

Where V_{OUT} is the output voltage of the converter, R is the loading resistance, L and C are the output inductance and capacitance, and V_P is the peak-to-peak voltage of ramp applied at modulator input. The overall loop gain after compensation can be described as :

Loop Gain = T = G_d x F_m x A

Where A denotes as compensation gain. To compensate a typical voltage mode buck converter, there are two ordinary compensation schemes, well known as type-II compensator and type-III compensator. The choice of using type-II or type-III compensator will be up to platform designers, and the main concern will be the position of the capacitor ESR zero and mid-frequency to high-frequency gain boost. Typically, the ESR zero of output capacitor will tend to stabilize the effect of output LC double poles, hence the positon of the output capacitor ESR zero in frequency domain may influence the design of voltage loop compensation. If $F_{ZERO,ESR}$ is <1/2F_{CO} where F_{CO} denotes cross-over frequency, type-II compensation will be sufficient for voltage stability. If $F_{ZERO,ESR}$ is > 1/2F_{CO} (or higher gain and phase margin is required at mid-frequency to high-frequency), then type-III compensation may be a better solution for voltage loop compensation.

A typical type-II compensation network is shown in Figure 13.

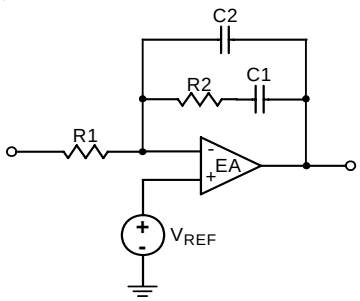


Figure 13. Type-II Compensation

R1 can be determined independently from DC considerations. Normally choose R1 that the current passing by will be around 1mA. Therefore,

$$R1 = \frac{V_{REF}}{1mA}$$

Then determine R2 by the boosted gain of loop gain at crossover :

$$R2 = R1 \times \frac{V_P}{V_{IN(MAX)}} \times \left(\frac{F_{ZERO,\ ESR}}{F_{LC}}\right)^2 \times \frac{F_{CO}}{F_{ZERO,\ ESR}}$$

Where $V_{IN(MAX)}$ is the max input voltage of power stage, V_P is the peak-to-peak voltage of ramp applied at modulator input, $F_{ZERO,ESR}$ is the frequency of output capacitor ESR zero, and F_{LC} is the frequency of output LC :

$$F_{ZERO,\ ESR} = \frac{1}{2\pi \times R_{ESR} \times C}$$

$$F_{LC} = \frac{1}{2\pi \times \sqrt{LC}}$$

After determining the phase margin at crossover frequency, the position of zero and pole produced by type-II compensation network, F_Z and F_P, can then be determined. The bode plot of type-II compensation is shown in Figure14, where

$$F_Z = \frac{1}{2\pi \times R2 \times C1}$$

$$F_P = \frac{1}{2\pi \times R2 \times (C1\ //\ C2)}$$

F_Z can be determined by the following Equation :

$$\tan^{-1}\left(\frac{F_{CO}}{F_Z}\right) - \tan^{-1}\left(\frac{F_Z}{F_{CO}}\right) \geq 90^\circ$$

$$+P.M. - \tan^{-1}\left(\frac{F_{CO}}{F_{ZERO,\ ESR}}\right)$$

By properly choosing F_Z to fit equation (22), C1 can then be determined by :

$$C1 = \frac{1}{2\pi \times R2 \times F_Z}$$

and C2 can be determined by :

$$C2 = \frac{1}{2\pi \times R2 \times \frac{F^2_{CO}}{F_Z} - \frac{1}{C1}}$$

A typical type-III compensation contains two zeros and two poles where the extra one zero and one pole compared with type-II compensation are added for stabilizing the system when ESR zero is relatively far from LC double poles in frequency domain. Figure15. and Figure.16 shows the typical circuit and bode plot of the type-III compensation.

After determining desired phase margin, according to the following Equation :

$$\tan^{-1}\left(\frac{F_{CO}}{F_Z}\right)-\tan^{-1}\left(\frac{F_Z}{F_{CO}}\right)\geq\frac{P.M.}{2}+45^\circ$$

and

$$F_P=\frac{F_{CO}^2}{F_Z}$$

F_Z and F_P can be determined by choosing proper F_{CO} to F_Z ratio to meet Equation (25). Again, R1 can be determined by the Equation (16).

R2 can be determined by the following Equation :

$$R2=R1\times\frac{V_P}{V_{IN(MAX)}}\times\left(\frac{F_{CO}}{F_{LC}}\right)^2\times\frac{F_Z}{F_{CO}}$$

Other component values of the Type-III compensation can then be calculated as :

$$C1=\frac{1}{2\pi\times R2\times F_Z}$$

$$C2=\frac{1}{2\pi\times R2\times F_P-\frac{1}{C1}}$$

$$C3=\frac{1}{2\pi\times R1\times F_Z}$$

$$R3=\frac{1}{2\pi\times C3\times F_P}$$

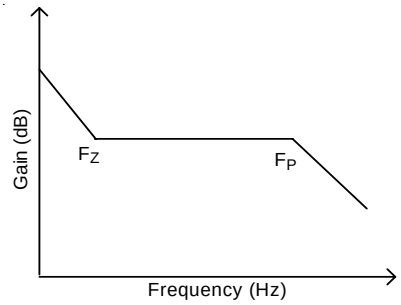


Figure 14. Bode Plot of Type-II Compensation

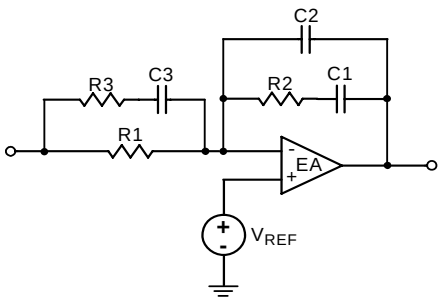


Figure 15. Type-III Compensation

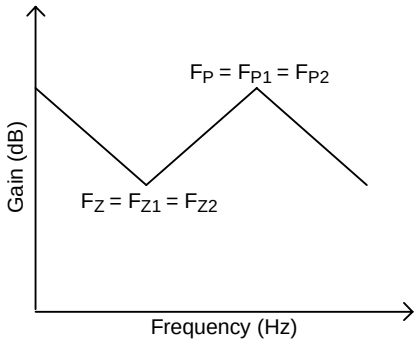


Figure 16. Bode Plot of the Type-III Compensation

Layout Considerations

For best performance of the RT8841, the following guidelines must be strictly followed :

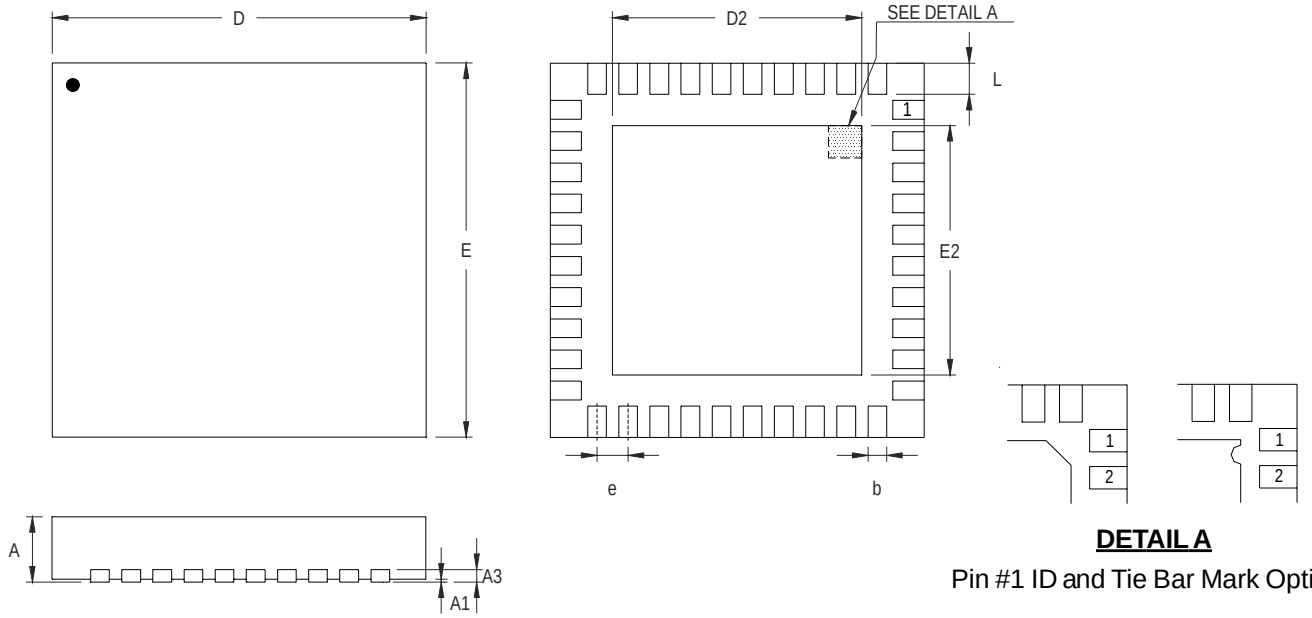
- Input bulk capacitors and MLCCS have to be put near high side MOSFETs. The connection plane of input capacitors and high side MOSFETs then can be kept as square as possible.
- The shape of phase planes (the connection plane between high side MOSFETs, low side MOSFETs and output inductors) have to be as square as possible. Long traces, thin bars or separated islands must be avoided in phase planes.
- Keep snubber circuits or damping elements near its objects. Phase RC snubbers have to be close to low side MOSFETs, UGATE damping resistors have to be close to high side MOSFETs, and boot to phase damping resistors have to be close to high side MOSFETs and phase planes. Also keep the traces of these snubbers circuits as short as possible.
- The area of V_{IN} plane (power stage 12V V_{IN}) and V_{OUT} plane (output bulk capacitors and inductors connection plane) have to be as wide as possible. Long traces or thin bars must be avoided in these planes. The plane trace width must be wide enough to carry large input/ output current (40mil/A).
- The following traces have to be wide and short : UGATE, LGATE, BOOT, PHASE, and VCC12. Make sure the width of these traces are wide enough to carry large driving current(at least 40mil).
- The voltage feedback loop contains two traces, VCC and VSS, which are Kelvin sensed from CPU socket or output capacitors. These two traces are suggested above

10mil width and put away from high (di/dt) switching elements such as high side MOSFETs, low side MOSFETs, phase plane etc. The circuit elements of voltage feedback loop, such as feedback loop short resistors and voltage loop compensation RCs, have to be kept near the RT8841 and also away from switching elements.

- The current sense mechanism of the RT8841 is fully differential Kelvin sense. Therefore, the current sense loops of the RT8841 contain two traces : the positive traces(ISP1 to ISP4) come from the positive node of output inductors(the node connecting phase plane) and the negative traces (ISN1 to ISN4) come from the negative node of output inductors(the node connecting output plane).

  DO NOT connect the current sense traces from phase plane or output plane. Only connect these traces from both sides of output inductors can achieve the goal of precise Kelvin sense. The current sense feedback loops have to be routed away from switching elements, and the current sense RC elements have to be put near their respective ISN or ISP pins of the RT8841 and also away from noise switching elements. At least 10 mil width is suggested for current sense feedback loops.

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	5.950	6.050	0.234	0.238
D2	4.000	4.750	0.157	0.187
E	5.950	6.050	0.234	0.238
E2	4.000	4.750	0.157	0.187
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 6x6 Package

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