

88A, 68V N-CHANNEL MOSFET

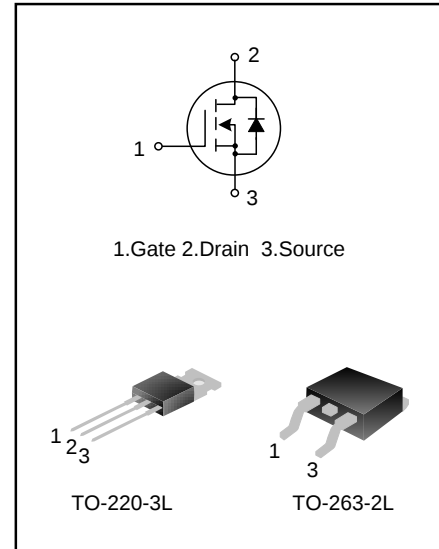
DESCRIPTION

The SVT078R0NT/S is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in the fields of uninterruptible power supplies and power management of inverter systems.

FEATURES

- ◆ 88A, 68V, $R_{DS(on)(typ.)}=6.0m\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVT078R0NT	TO-220-3L	078R0NT	Pb free	Tube
SVT078R0NS	TO-263-2L	078R0NS	Halogen free	Tube
SVT078R0NSTR	TO-263-2L	078R0NS	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_C=25^{\circ}C$)

Characteristics		Symbol	Ratings		Unit
			SVT078R0NT	SVT078R0NS	
Drain-Source Voltage		V _{DS}	68		V
Gate-Source Voltage		V _{GS}	±25		V
Drain Current	T _C =25°C	I _D	88		A
	T _C =100°C		65		
Drain Current Pulsed		I _{DM}	352		A
Power Dissipation (T _C =25°C) -Derate above 25°C		P _D	140	140	W
			0.93	0.93	W/°C
Single Pulsed Avalanche Energy (Note1)		E _{AS}	420		mJ
Operation Junction Temperature Range		T _J	-55~+175		°C
Storage Temperature Range		T _{stg}	-55~+175		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVT078R0NT	SVT078R0NS	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.07	1.07	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_c=25^{\circ}\text{C}$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	68	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=68V, V_{GS}=0V$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 25V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=35A$	--	6.0	8.0	$m\Omega$
Gate Resistance	R_G	$f=1\text{MHz}$		2.0		Ω
Input Capacitance	C_{iss}	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=30V$	--	3962	--	pF
Output Capacitance	C_{oss}		--	262	--	
Reverse Transfer Capacitance	C_{rss}		--	180	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V, R_G=8\Omega, I_D=40A$ (Notes 2,3)	--	24	--	ns
Turn-on Rise Time	t_r		--	46	--	
Turn-off Delay Time	$t_{d(off)}$		--	73	--	
Turn-off Fall Time	t_f		--	29	--	
Total Gate Charge	Q_g	$V_{DD}=54V, V_{GS}=10V, I_D=40A$ (Notes 2,3)	--	74.6	--	nC
Gate-Source Charge	Q_{gs}		--	21.8	--	
Gate-Drain Charge	Q_{gd}		--	20.5	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	88	A
Pulsed Source Current	I_{SM}		--	--	352	
Diode Forward Voltage	V_{SD}	$I_S=20A, V_{GS}=0V$	--	0.8	1.2	V
Reverse Recovery Time	T_{rr}	$I_S=40A, V_{GS}=0V,$ $dI_F/dt=100A/\mu s$	--	23	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.02	--	μC

Notes:

1. $L=1mH, I_{AS}=29A, V_{DD}=50V, R_G=10\Omega$, starting $T_J=25^{\circ}\text{C}$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

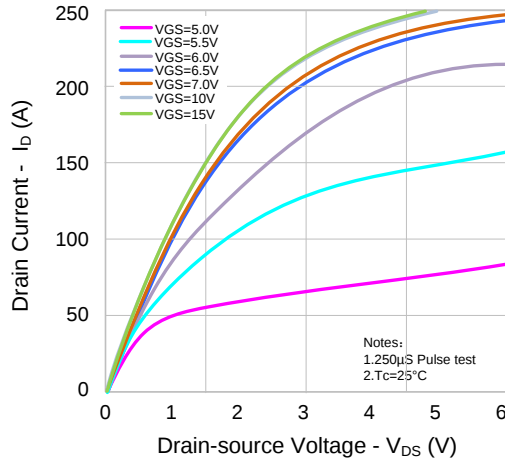


Figure 2. Transfer Characteristics

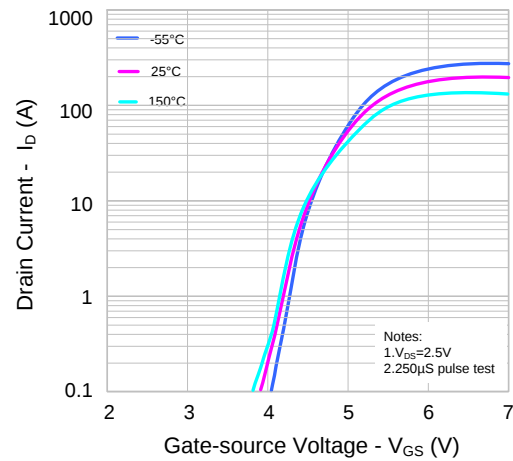


Figure 3. On-resistance vs. Drain Current

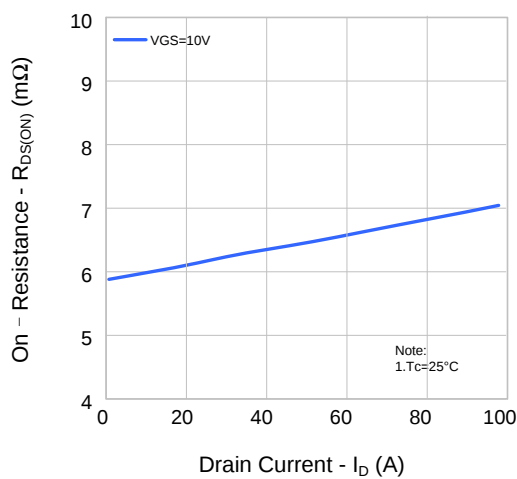


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

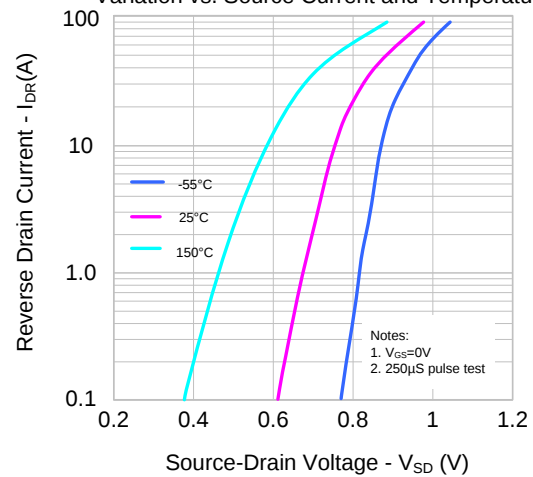


Figure 5. Capacitance Characteristics

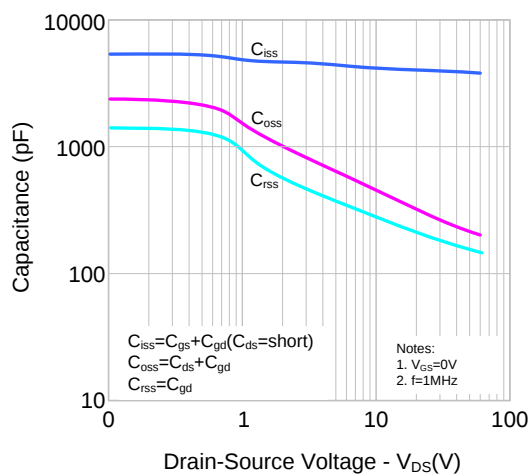
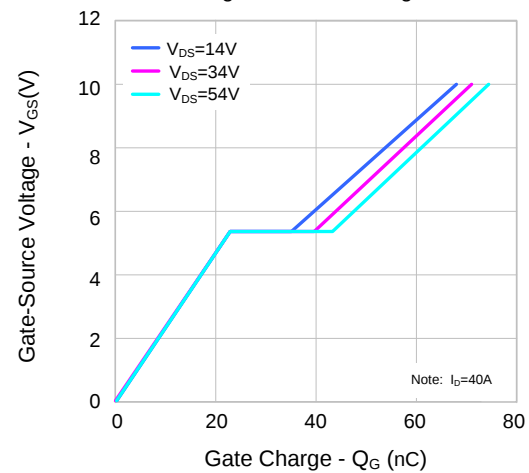
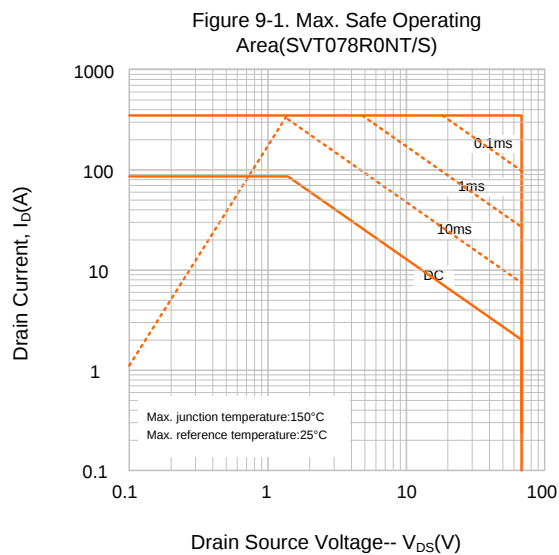
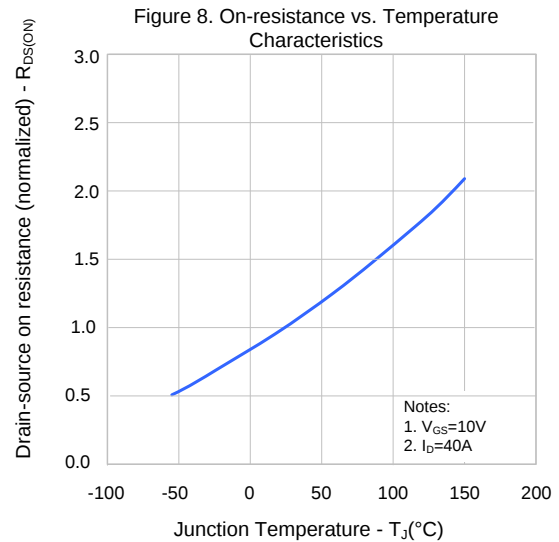
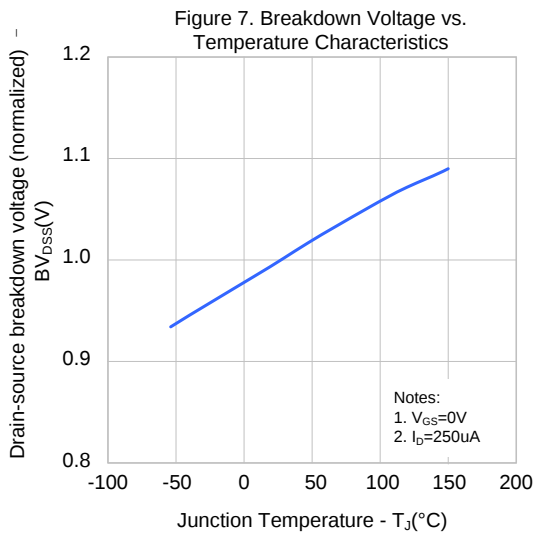


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (continued)



TYPICAL TEST CIRCUIT

Figure 1: Gate Charge Test Circuit & Waveform

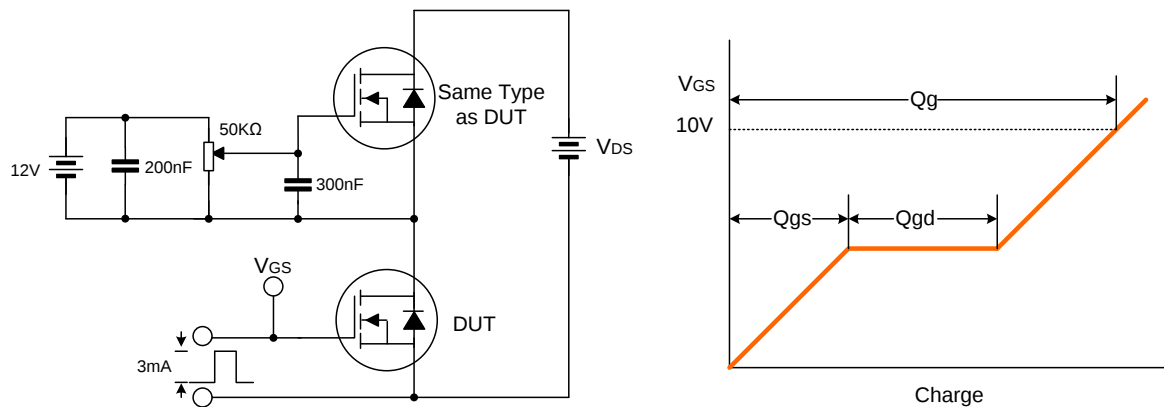


Figure 2: Resistive Switching Test Circuit & Waveform

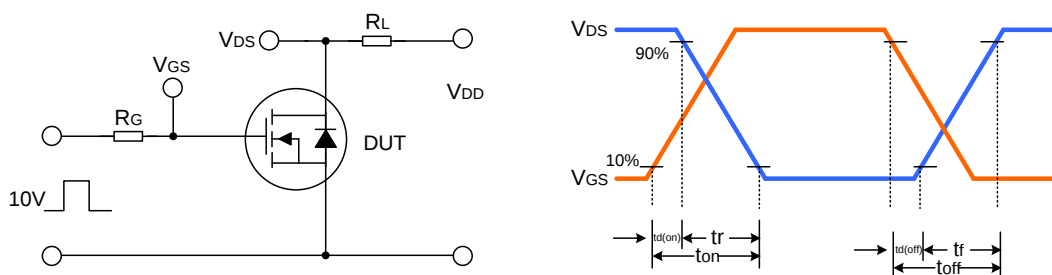
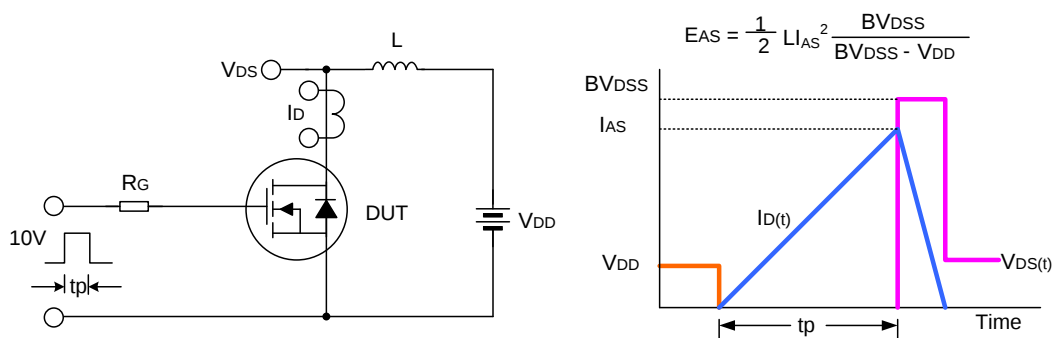


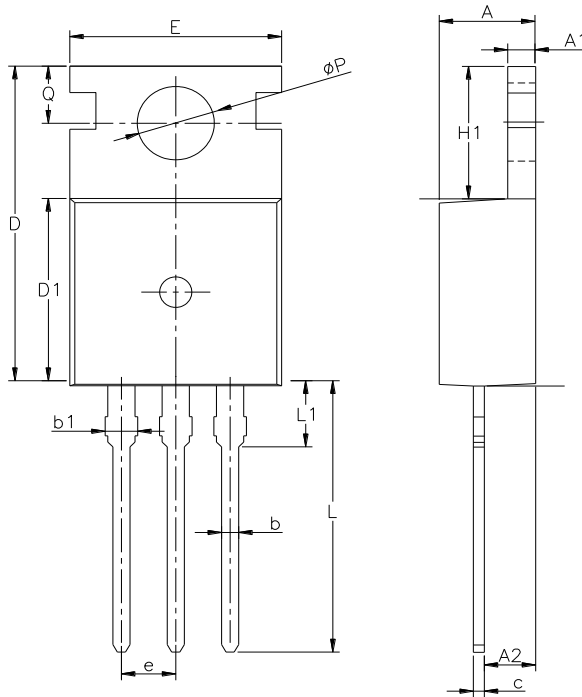
Figure 3: Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220-3L

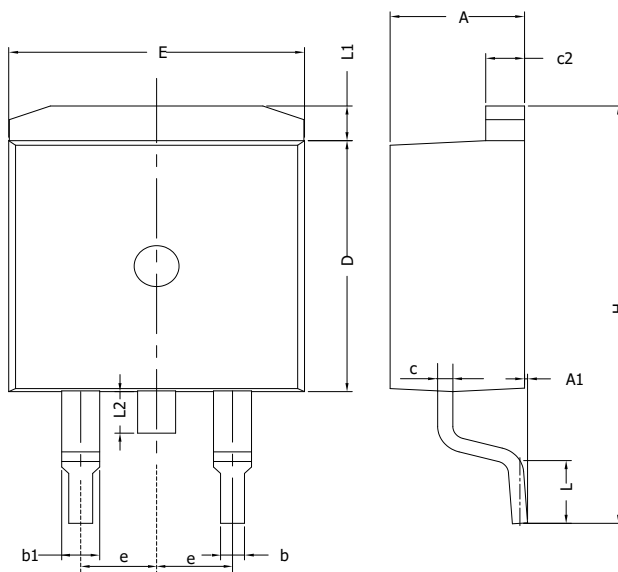
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-263-2L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

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Part No.: **SVT078R0NT/S**Document Type: **Datasheet**Copyright: **HANGZHOU SILAN MICROELECTRONICS CO.,LTD**Website: **<http://www.silan.com.cn>**Rev.: **1.4**

Revision History:

1. Delete the package outline of TO-252-2L

Rev.: **1.3**

Revision History:

1. Update the package outline of TO-220-3L

Rev.: **1.2**

Revision History:

1. Add the package outline of TO-263-2L

Rev.: **1.1**

Revision History:

1. Delete the package outline of TO-263-2L

Rev.: **1.0**

Revision History:

1. First release