Synchronous-Rectified Buck MOSFET Drivers

General Description

The RT9618/A are high frequency, dual MOSFET drivers specifically designed to drive two power N-MOSFETs in a synchronous-rectified buck converter topology. The drivers combined with Richtek' s series of Multi-Phase Buck PWM controller form a complete core-voltage regulator solution for advanced micro-processors.

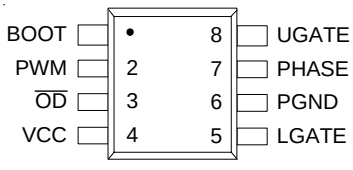
The RT9618/A drive both the lower/upper gate in a synchronous-rectifier bridge with 12V. This drive-voltage flexibility provides the advantage of optimizing applications involving trade-offs between switching losses and conduction losses.

RT9618A has longer UGATE/LGATE deadtime which can drive the MOSFETs with large gate RC value, avoiding the shoot-through phenomenon. RT9618 is targeted to drive low gate RC MOSFETs and performs better efficiency.

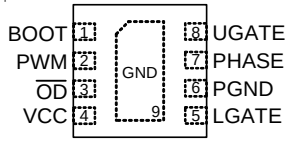
The output drivers in the RT9618/A can efficiently switch power MOSFETs at frequency up to 500kHz. Switching frequency above 500kHz has to take into account the thermal dissipation of the packages. RT9618/A are capable to drive a 3nF load with a 30ns rise time. RT9618/A implements bootstrapping on the upper gate with an external capacitor and an embedded diode. This reduces implementation complexity and allows the use of higher performance, cost effective N-MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

Pin Configurations

(TOP VIEW)



SOP-8



WDFN-8L 3x3

Features

- **Drives Two N-MOSFETs**
- **Adaptive Shoot-Through Protection**
- **Embedded Boot Strapped Diode**
- **Support High Switching Frequency**
- **Fast Output Rise Time**
- **Small SOP-8 and 8-Lead WDFN Package**
- **Tri-State Input for Bridge Shutdown**
- **Supply Under Voltage Protection**
- **Upper MOSFET Direct Shorted Protection**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Core Voltage Supplies for Desktop, Motherboard CPU
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters

Ordering Information

RT9618/A □ □

- Package Type
  - S : SOP-8
  - QW : WDFN-8L 3x3
- Lead Plating System
  - P : Pb Free
  - G : Green (Halogen Free and Pb Free)
- Long Dead Time
- Short Dead Time

Note :

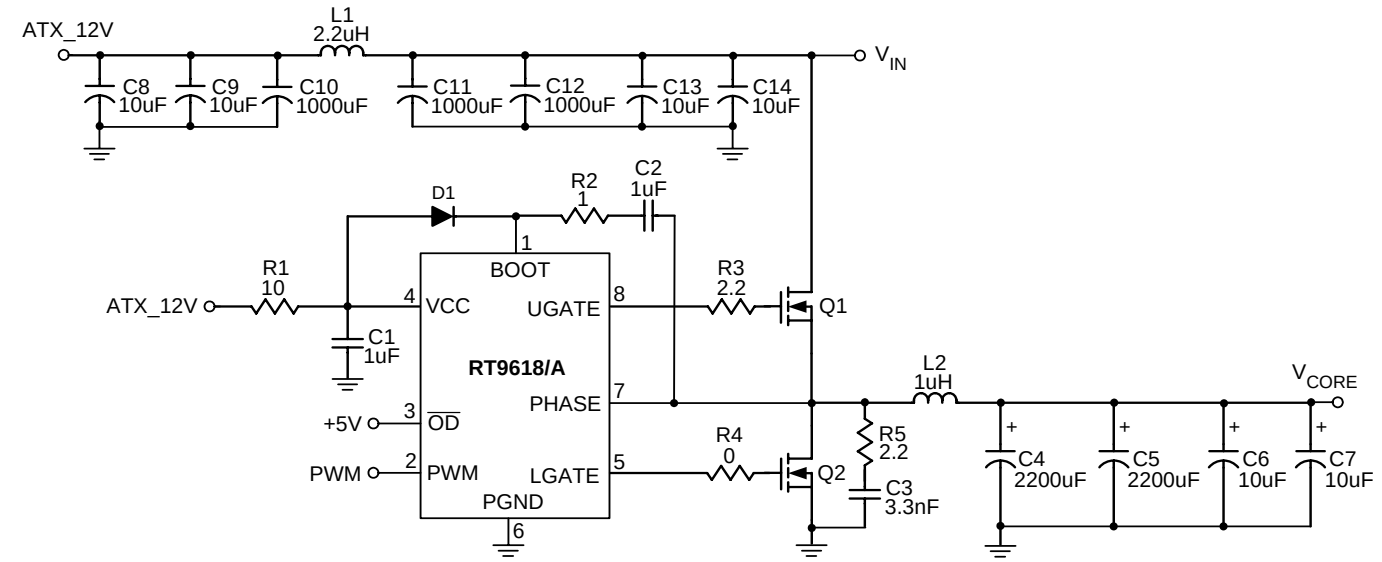
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

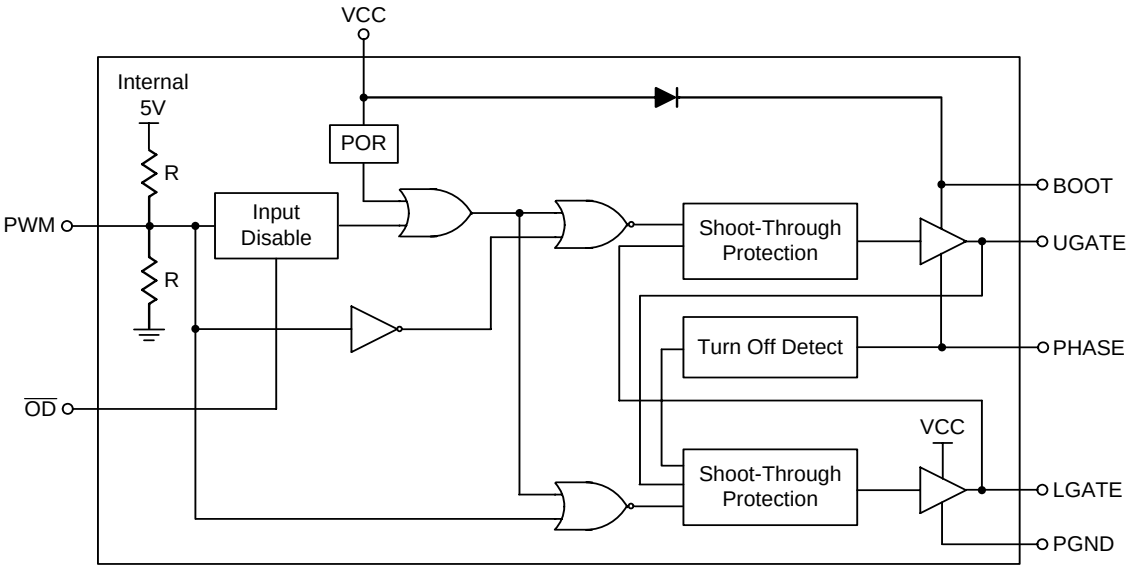
Typical Application Circuit



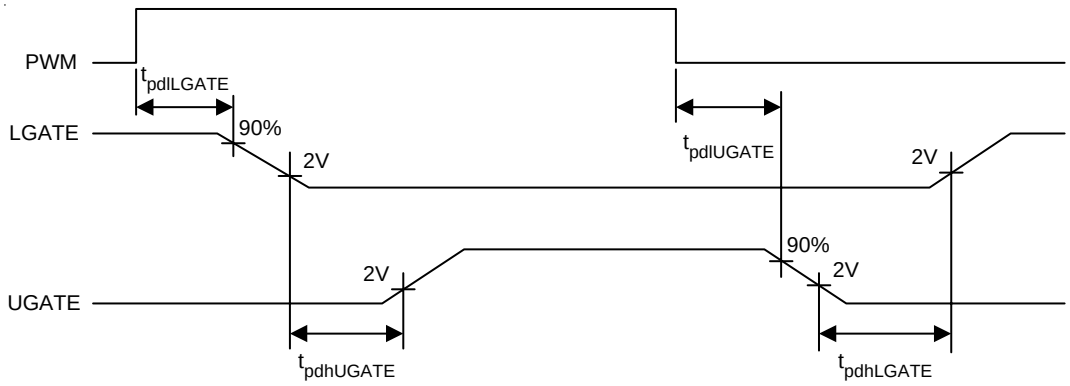
Functional Pin Description

Pin No.		Pin Name	Pin Function
RT9618/A□S	RT9618/A□QW		
1	1	BOOT	Floating bootstrap supply pin for upper gate drive.
2	2	PWM	Input PWM signal for controlling the driver.
3	3	$\overline{OD}$	Output Disable. When low, both UGATE and LGATE are driven low and the normal operation is disabled.
4	4	VCC	+12V Supply Voltage.
5	5	LGATE	Lower Gate Drive Output. Connected to gate of low-side power N-MOSFET.
6	6	PGND	Common Ground.
7	7	PHASE	Connected this pin to the source of the high-side MOSFET and the drain of the low-side MOSFET.
8	8	UGATE	Upper Gate Drive Output. Connected to gate of high-side power N-MOSFET.
--	9 (Exposed Pad)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Timing Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- –0.3V to 15V
- BOOT to PHASE ---------- –0.3V to 15V
- BOOT to GND
  - DC ---------- –0.3V to V_{CC} + 15V
  - < 200ns ---------- –0.3V to 42V
- PHASE to GND
  - DC ---------- –5V to 15V
  - < 200ns ---------- –10V to 30V
- LGATE
  - DC ---------- GND – 0.3V to V_{CC} + 0.3V
  - < 200ns ---------- –2V to V_{CC} + 0.3V
- UGATE ---------- V_{PHASE} – 0.3V to V_{BOOT} + 0.3V
  - < 200ns ---------- V_{PHASE} – 2V to V_{BOOT} + 0.3V
- PWM Input Voltage ---------- GND – 0.3V to 7V
- $\overline{OD}$ ---------- GND – 0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 ---------- 0.625W
  - WDFN-8L 3x3 ---------- 0.909W
- Package Thermal Resistance (Note 2)
  - SOP-8, θ_{JA} ---------- 160°C/W
  - WDFN-8L 3x3, θ_{JA} ---------- 110°C/W
  - WDFN-8L 3x3, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –40°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 12V ±10%
- Junction Temperature Range ---------- 0°C to 125°C
- Ambient Temperature Range ---------- 0°C to 70°C

Electrical Characteristics

(Recommended Operating Conditions, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply Voltage						
Power Supply Voltage	V_{CC}		7.3	--	13.5	V
V_{CC} Supply Current						
Power Supply Current	I_{VCC}	V_{BOOT} = 12V, PWM = 0V	--	1	2.5	mA
Power-On Reset						
POR Threshold	V_{VCCrth}	V_{CC} Rising	5.5	6.4	7.3	V

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Hysteresis		V_{VCChys}		--	2.2	--	V
PWM Input							
Maximum Input Current		I_{PWM}	PWM = 0V or 5V	--	300	--	μA
PWM Floating Voltage		V_{PWMfl}	V_{CC} = 12V	--	2.4	--	V
PWM Rising Threshold		V_{PWMrth}		3.2	3.6	3.9	V
PWM Falling Threshold		V_{PWMfth}		1.1	1.3	1.5	V
Output Disable Input							
$\overline{OD}$ Rising Threshold		$V_{\overline{OD}rth}$		1.5	1.8	2.1	V
$\overline{OD}$ Hysteresis		$V_{\overline{OD}hys}$		--	0.5	--	V
Timing							
UGATE Rise Time		t_{rUGATE}	V_{CC} = 12V, 3nF load	--	27	35	ns
UGATE Fall Time		t_{fUGATE}	V_{CC} = 12V, 3nF load	--	32	45	ns
LGATE Rise Time		t_{rLGATE}	V_{CC} = 12V, 3nF load	--	35	45	ns
LGATE Fall Time		t_{fLGATE}	V_{CC} = 12V, 3nF load	--	27	38	ns
Propagation Delay	RT9618	$t_{pdhUGATE}$	$V_{BOOT} - V_{PHASE}$= 12V See Timing Diagram	--	20	--	ns
	RT9618A			--	90	--	
	RT9618/A	$t_{pdlUGATE}$		--	15	--	
		$t_{pdhLGATE}$	See Timing Diagram	--	20	--	
		$t_{pdlLGATE}$		--	8	--	
Output							
UGATE Drive Source		$R_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$= 12V	--	1.9	3	Ω
UGATE Drive Sink		$R_{UGATEsk}$	$V_{BOOT} - V_{PHASE}$= 12V	--	1.4	3	Ω
LGATE Drive Source		$R_{LGATEsr}$	V_{CC} = 12V	--	1.9	3	Ω
LGATE Drive Sink		$R_{LGATEsk}$	V_{CC} = 12V	--	1.1	2.2	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the package.

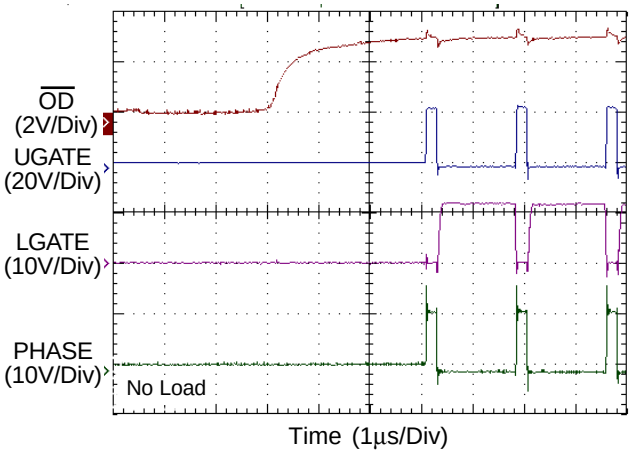
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

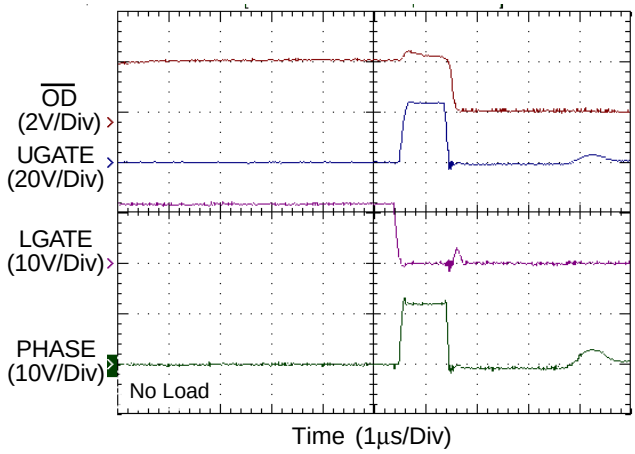
Typical Operating Characteristics

High side MOSFET : FR3707Z x 1, Low side MOSFET : LR8113 x 2

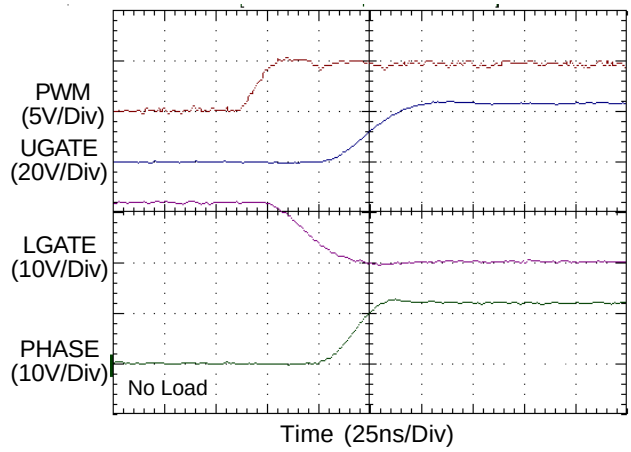
Drive Enable



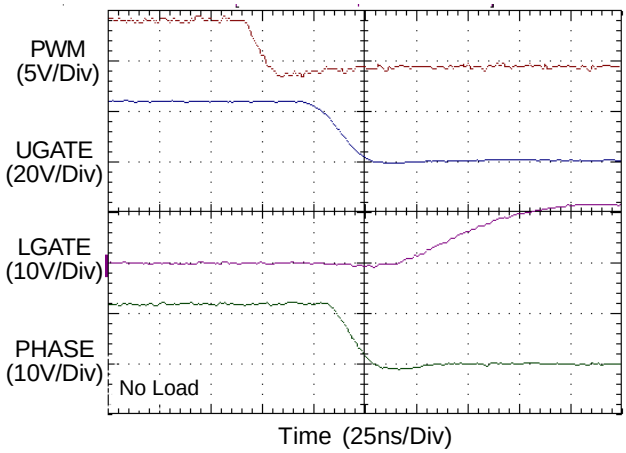
Drive Disable



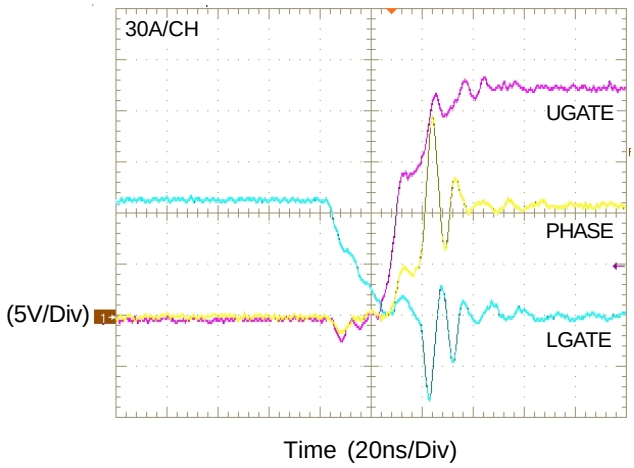
PWM to Drive Waveform



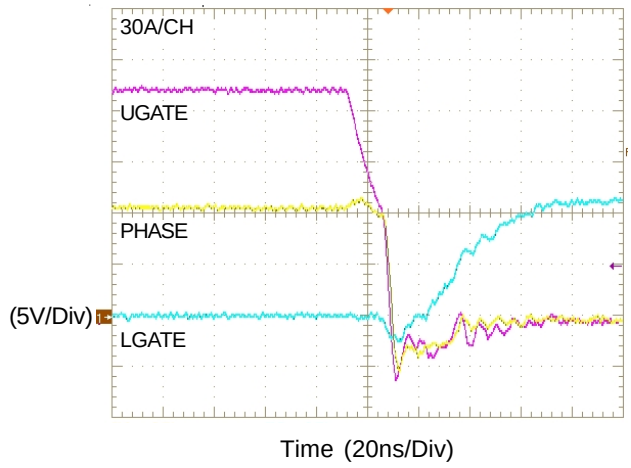
PWM to Drive Waveform



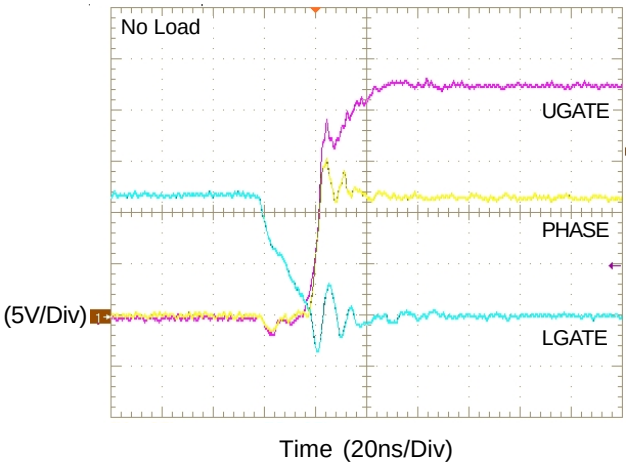
Dead Time



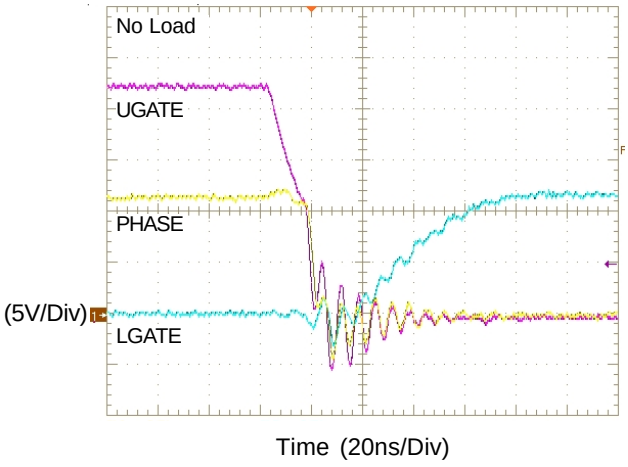
Dead Time



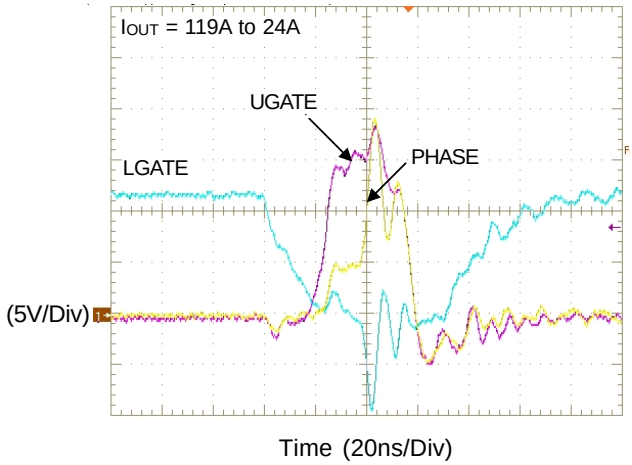
Dead Time



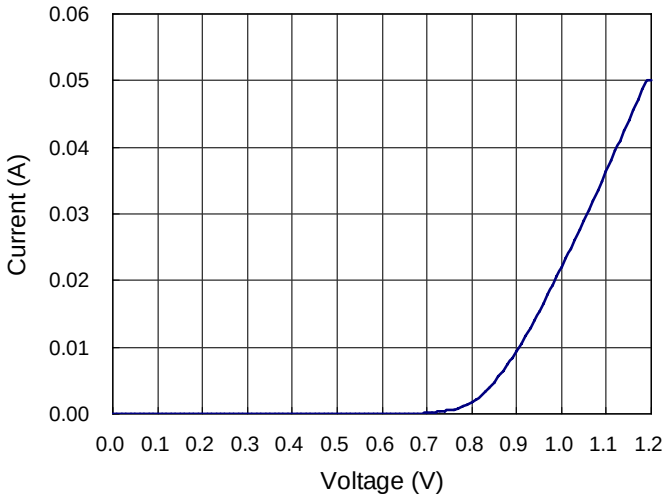
Dead Time



Short Pulse



Internal Diode I-V Curve



Application Information

The RT9618/A are designed to drive both high side and low side N-MOSFET through externally input PWM control signal. It has power-on protection function which held UGATE and LGATE low before VCC up across the rising threshold voltage. After the initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE signal turns low then UGATE signal is allowed to go high just after a non-overlapping time to avoid shoot-through current. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE signal reach a predetermined low level, LGATE signal is allowed to turn high.

The PWM signal is acted as "High" if above the rising threshold and acted as "Low" if below the falling threshold. Any signal level enters and remains within the shutdown window is considered as "tri-state", the output drivers are disabled and both MOSFET gates are pulled and held low. If left the PWM signal floating, the pin will be kept around 2.4V by the internal divider and provide the PWM controller with a recognizable level. $\overline{OD}$ pin will also shutdown the bridge of tied to GND.

The RT9618/A typically operate at frequency of 200kHz to 500kHz. It shall be noted that to place a 1N4148 or schottky diode between the VCC and BOOT pin as shown in the typical application circuit for ligher efficiency.

Non-overlap Control

To prevent the overlap of the gate drives during the UGATE turn low and the LGATE turn high, the non-overlap circuit monitors the voltages at the PHASE node and high side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to turn low (after propagation delay). Before LGATE can turn high, the non-overlap protection circuit ensures that the monitored voltages have gone below 1.2V. Once the monitored voltages fall below 1.2V, LGATE begins to turn high. For short pulse condtion, if the PHASE pin had not gone high after LGATE turns low, the LGATE has to wait for 200ns before turn high. By waiting for the voltages of the PHASE pin and high side gate drive to fall below 1.2V, the non-overlap protection circuit ensures that UGATE is low before LGATE turns high.

Also to prevent the overlap of the gate drives during LGATE turn low and UGATE turn high, the non-overlap circuit monitors the LGATE voltage. When LGATE go below 1.2V, UGATE is allowed to go high.

Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs} at 12V (or 5V), the gate draws the current only few nano-amperes. Thus once the gate has been driven up to "ON" level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

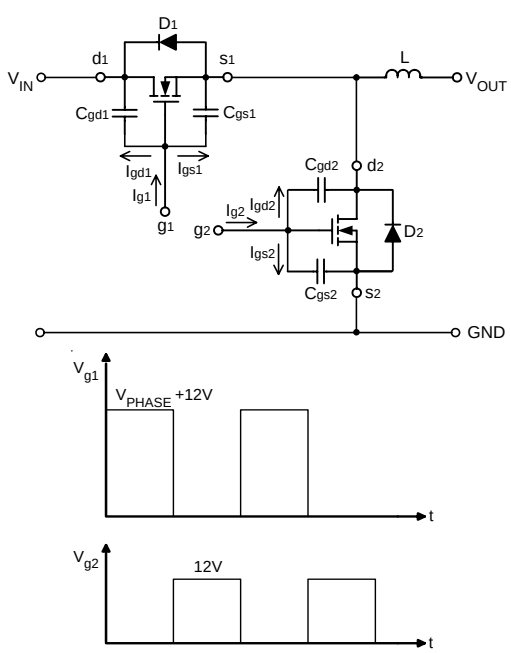


Figure 1. Equivalent Circuit and Associated Waveforms

In Figure 1, the current I_{g1} and I_{g2} are required to move the gate up to 12V. The operation consists of charging C_{gd} and C_{gs}. C_{gs1} and C_{gs2} are the capacitances from gate to source of the high side and the low side power MOSFETs, respectively. In general data sheets, the C_{gs} is referred as "C_{iss}" which is the input capacitance. C_{gd1} and C_{gd2} are the capacitances from gate to drain of the high side and

the low side power MOSFETs, respectively and referred to the data sheets as "C_{rss}" the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high side and the low side power MOSFETs respectively, the required current I_{gs1} and I_{gs2} are showed below :

$$I_{gs1} = C_{gs1}\frac{dVg1}{dt} = \frac{C_{gs1}\times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs1}\frac{dVg2}{dt} = \frac{C_{gs1}\times 12}{t_{r2}} \quad (2)$$

Before driving the gate of the high side MOSFET up to 12V (or 5V), the low side MOSFET has to be off; and the high side MOSFET is turned off before the low side is turned on. From Figure 1, the body diode "D_2" had been turned on before high side MOSFETs turned on.

$$I_{gd1} = C_{gd1}\frac{dV}{dt} = C_{gd1}\frac{12V}{t_{r1}} \quad (3)$$

Before the low side MOSFET is turned on, the C_{gd2} have been charged to V_{IN}. Thus, as C_{gd2} reverses its polarity and g_2 is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{Vi+12V}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified buck converter, input voltage V_{IN} = 12V, $V_{g1} = V_{g2}$ = 12V. The high side MOSFET is PHB83N03LT whose C_{iss} = 1660pF, C_{rss} = 380pF, and t_r = 14ns. The low side MOSFET is PHB95N03LT whose C_{iss} = 2200pF, C_{rss} = 500pF and t_r = 30ns, from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660\times 10^{-12}\times 12}{14\times 10^{-9}} = 1.428 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200\times 10^{-12}\times 12}{30\times 10^{-9}} = 0.88 \quad (A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380\times 10^{-12}\times 12}{14\times 10^{-9}} = 0.326 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500\times 10^{-12}\times (12+12)}{30\times 10^{-9}} = 0.4 \quad (A) \quad (8)$$

the total current required from the gate driving source is

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.754 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28 \quad (A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

Select the Bootstrap Capacitor

Figure 2 shows part of the bootstrap circuit of RT9618/A. The V_{CB} (the voltage difference between BOOT and PHASE on RT9618/A) provides a voltage to the gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance C_B has to be selected properly. It is determined by following constraints.

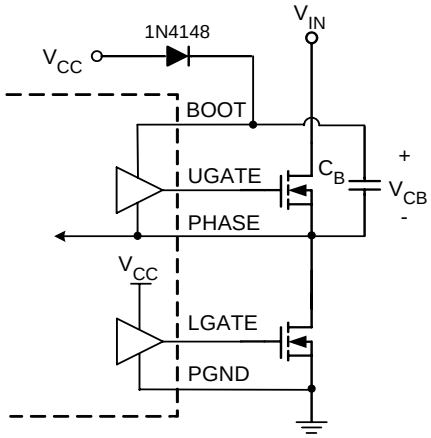


Figure 2. Part of Bootstrap Circuit of RT9618/A

In practice, a low value capacitor C_B will lead the over-charging that could damage the IC. Therefore to minimize the risk of overcharging and reducing the ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1µF, and the larger the better. In general design, using 1uF can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. Here, to adopt either a ceramic or tantalum capacitor is suitable.

Power Dissipation

For not exceeding the maximum allowable power dissipation to drive the IC beyond the maximum recommended operating junction temperature of 125°C, it is necessary to calculate power dissipation appro-priately.

This dissipation is a function of switching frequency and total gate charge of the selected MOSFET. Figure 3 shows the power dissipation test circuit. C_L and C_U are the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is 0.01uF.

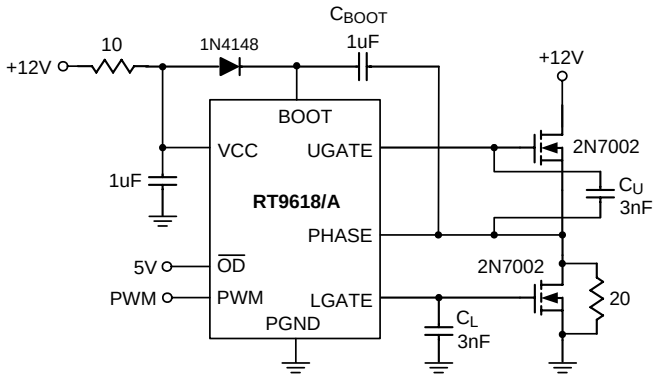


Figure 3. Test Circuit

Figure 4 shows the power dissipation of the RT9618/A as a function of frequency and load capacitance. The value of the C_U and C_L are the same and the frequency is varied from 100kHz to 1MHz.

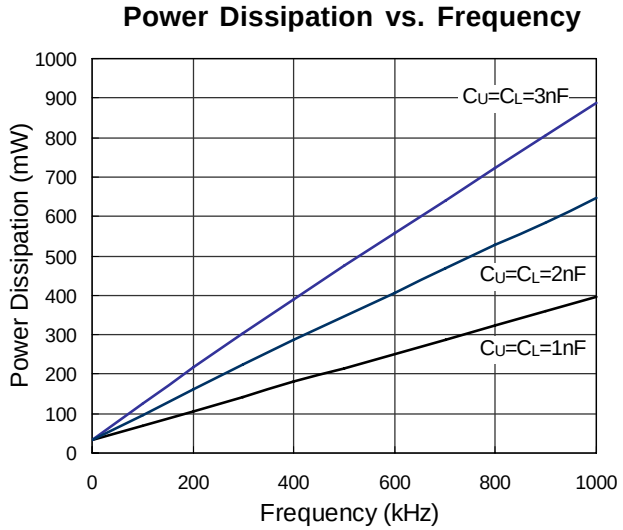


Figure 4. Power Dissipation vs. Frequency

The operating junction temperature can be calculated from the power dissipation curves (Figure 4). Assume V_{CC} =12V, operating frequency is 200kHz and the C_U=C_L=1nF which emulate the input capacitances of the high side and low side power MOSFETs. From Figure 4, the power dissipation is 100mW. For RT9618/A, the SOP-8 package thermal resistance θ_{JA} is 160°C/W, the operating junction temperature is calculated as :

$$T_J = (160°C/W \times 100mW) + 25°C = 41°C \quad (11)$$

where the ambient temperature is 25°C.

The method to improve the thermal transfer is to increase the PCB copper area around the RT9618/A first. Then, adding a ground pad under IC to transfer the heat to the peripheral of the board.

Layout Consideration

Figure 5 shows the schematic circuit of a two-phase synchronous buck converter to implement the RT9618/A. The converter operates from 5V to 12V of V_{IN}.

When layout the PCB, it should be very careful. The power-circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The junction of Q1, Q2, L2 should be very close.

Next, the trace from UGATE, and LGATE should also be short to decrease the noise of the driver output signals. PHASE signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C4 should be connected to PGND directly. Furthermore, the bootstrap capacitors (C_B) should always be placed as close to the pins of the IC as possible.

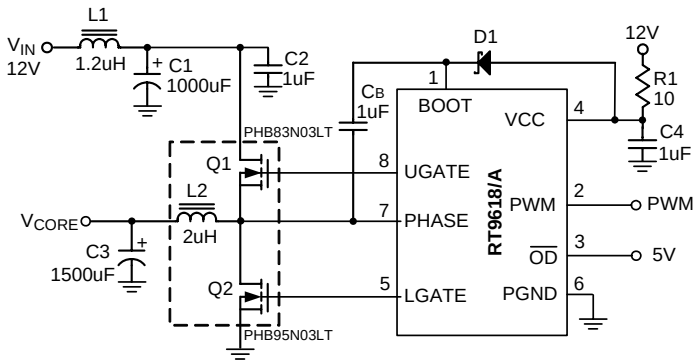
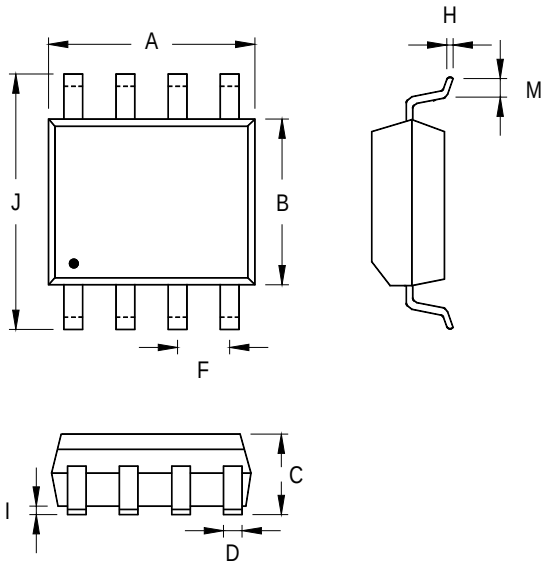


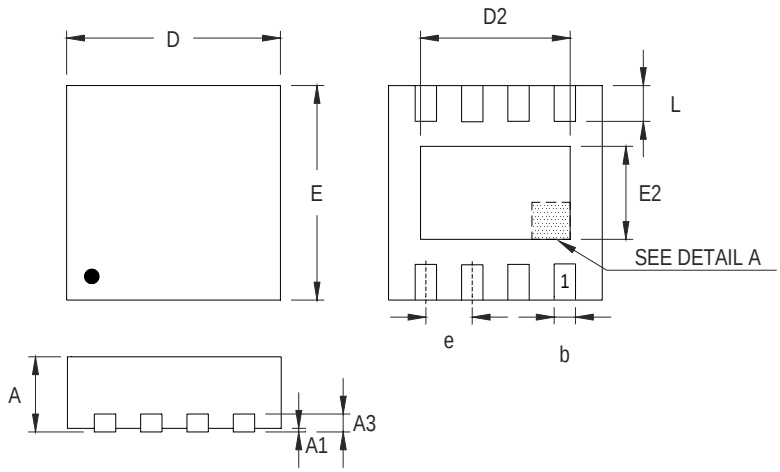
Figure 5. Two-Phase Synchronous Buck Converter Circuit

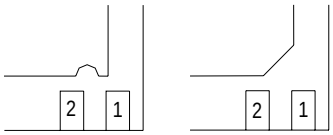
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.200	2.700	0.087	0.106
E	2.950	3.050	0.116	0.120
E2	1.450	1.750	0.057	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 8L DFN 3x3 Package, 0.5mm Lead Pitch

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