LM4755 Stereo 11W Audio Power Amplifier with Mute

Check for Samples: LM4755

FEATURES

- **Drives 4Ω and 8Ω Loads**
- **Integrated Mute Function**
- **Internal Gain Resistors**
- **Minimal External Components Needed**
- **Single Supply Operation**
- **Internal Current Limiting and Thermal Protection**
- **Compact 9-lead TO-220 Package**
- **Wide Supply Range 9V - 40V**

APPLICATIONS

- **Stereos TVs**
- **Compact Stereos**
- **Mini Component Stereos**

KEY SPECIFICATIONS

- **Output Power at 10% THD with 1kHz into 4Ω at V_{CC} = 24V 11 W (typ)**
- **Output Power at 10% THD with 1kHz into 8Ω at V_{CC} = 24V 7 W (typ)**
- **Closed Loop Gain 34 dB (typ)**
- **P_O at 10% THD+N @ 1kHz into 4Ω Single-Ended DDPAK Package at V_{CC}=12V 2.5 W (typ)**
- **P_O at 10% THD+N @ 1kHz into 8Ω Bridged DDPAK Package at V_{CC}=12V 5 W (typ)**

DESCRIPTION

The LM4755 is a stereo audio amplifier capable of delivering 11W per channel of continuous average output power to a 4Ω load or 7W per channel into 8Ω using a single 24V supply at 10% THD+N. The internal mute circuit and pre-set gain resistors provide for a very economical design solution.

Output power specifications at both 20V and 24V supplies and low external component count offer high value to consumer electronic manufacturers for stereo TV and compact stereo applications. The LM4755 is specifically designed for single supply operation.

TYPICAL APPLICATION

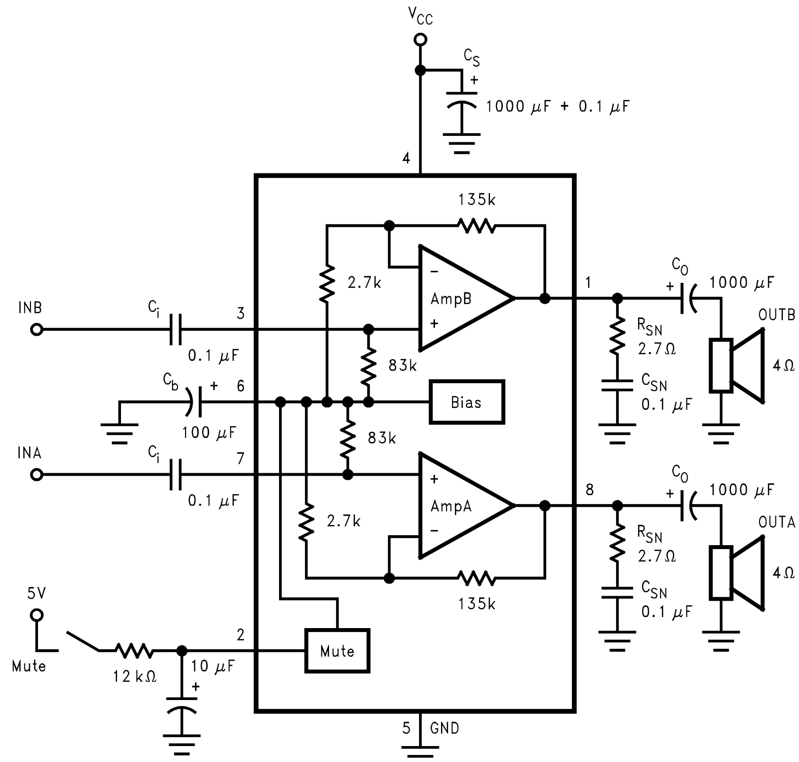
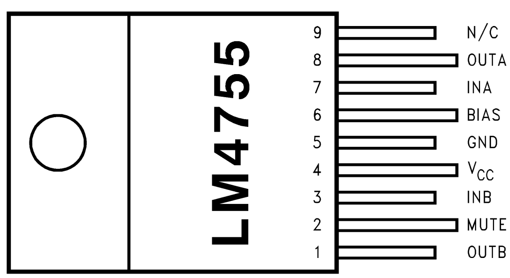
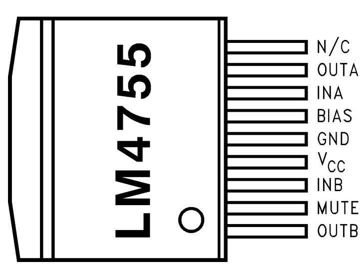


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram



9 Pin TO-220
Plastic Package (Top View)
See Package Number NEC



9 Pin DDPAK
Plastic Package (Top View)
See Package Number KTW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[(1)(2)(3)(4)]

Supply Voltage		40V
Input Voltage		±0.7V
Input Voltage at Output Pins [(5)]		GND -0.4V
Output Current		Internally Limited
Power Dissipation [(6)]		62.5W
ESD Susceptibility [(7)]		2 kV
Junction Temperature		150°C
Soldering Information	NEC Package (10 seconds)	250°C
Storage Temperature		−40°C to 150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The TO-263 Package is not recommended for V_S > 16V due to impractical heatsinking limitations.
(4) All voltages are measured with respect to the GND pin (5), unless otherwse specified.
(5) The outputs of the LM4755 cannot be driven externally in any mode with a voltage lower than -0.4V below GND or permanent damage to the LM4755 will result.
(6) For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of θ_{JC} = 2°C/W (junction to case). Refer to the section DETERMINING MAXIMUM POWER DISSIPATION in the APPLICATION INFORMATION section for more information.
(7) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

OPERATING RATINGS

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	9V to 32V
θ_{JC}	2°C/W
θ_{JA}	76°C/W

ELECTRICAL CHARACTERISTICS

The following specifications apply to each channel with V_{CC} = 24V, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4755		Units (Limits)
			Typical[(1)]	Limit	
I_{TOTAL}	Total Quiescent Power Supply Current	Mute Off	10	15	mA(max)
				7	mA(min)
		Mute On	7		mA
P_O	Output Power (Continuous Average per Channel)	f = 1 kHz, THD+N = 10%, R_L = 8Ω	7		W
		f = 1 kHz, THD+N = 10%, R_L = 4Ω	11	10	W(min)
		V_S = 20V, R_L = 8Ω	4		W
		V_S = 20V, R_L = 4Ω	7		W
		f = 1 kHz, THD+N = 10%, R_L = 4Ω V_S = 12V, DDPAK Pkg.	2.5		W
THD	Total Harmonic Distortion	f = 1 kHz, P_O = 1 W/ch, R_L = 8Ω	0.08		%
V_{OSW}	Output Swing	P_O = 10W, R_L = 8Ω	15		V
		P_O = 10W, R_L = 4Ω	14		V
X_{TALK}	Channel Separation	See Apps. Circuit (Figure 1) f = 1 kHz, V_O = 4 Vrms	55		dB

(1) Typicals are measured at 25°C and represent the parametric norm.

ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply to each channel with V_{CC} = 24V, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4755		Units (Limits)
			Typical (1)	Limit	
PSRR	Power Supply Rejection Ratio	See Apps. Circuit (Figure 1) f = 120 Hz, V_O = 1 mVrms	50		dB
V_{ODV}	Differential DC Output Offset Voltage	V_{IN} = 0V	0.09	0.4	V(max)
SR	Slew Rate		2		V/µs
R_{IN}	Input Impedance		83		kΩ
PBW	Power Bandwidth	3 dB BW at P_O = 2.5W, R_L = 8Ω	65		kHz
A_{VCL}	Closed Loop Gain (Internally Set)	R_L = 8Ω	34	33 35	dB(min) dB(max)
ε_{IN}	Noise	IHF-A Weighting Filter, R_L = 8Ω Output Referred	0.2		mVrms
I_O	Output Short Circuit Limit	V_{IN} = 0.5V, R_L = 2Ω		2	A(min)
Mute Pin V_{IL}	Mute Low Input Voltage	Not in Mute Mode		0.8	V(max)
V_{IH}	Mute High Input Voltage	In Mute Mode	2.0	2.5	V(min)
A_M	Mute Attenuation	V_{MUTE} = 5.0V	80		dB

EQUIVALENT SCHEMATIC

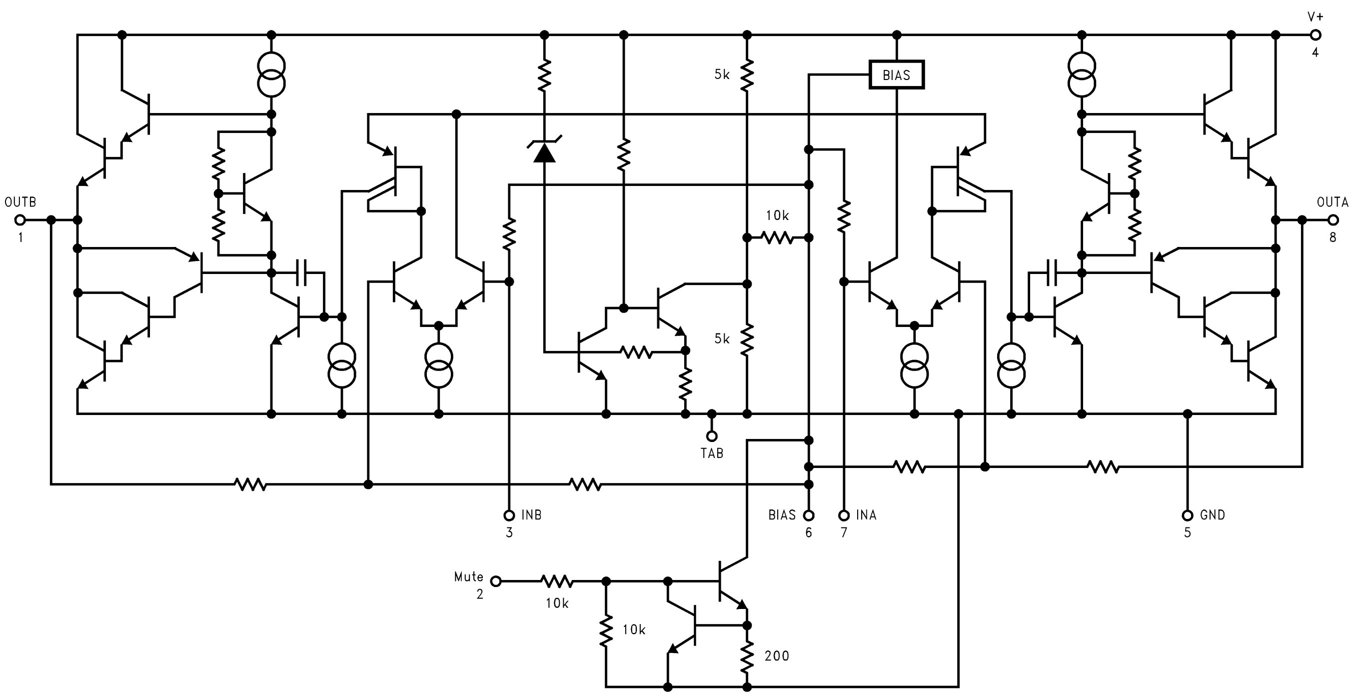


Figure 2.

TEST CIRCUIT

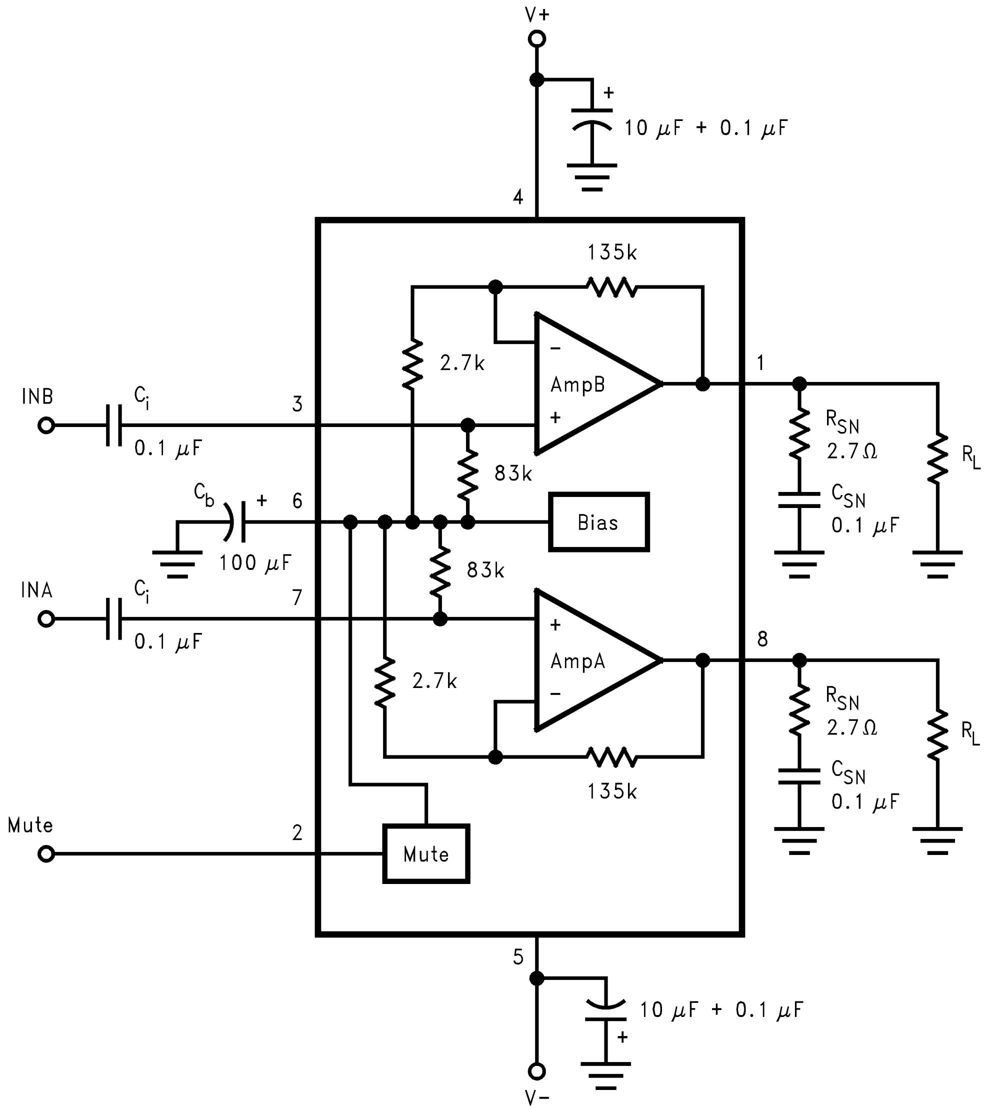


Figure 3. Test Circuit

SYSTEM APPLICATION CIRCUIT

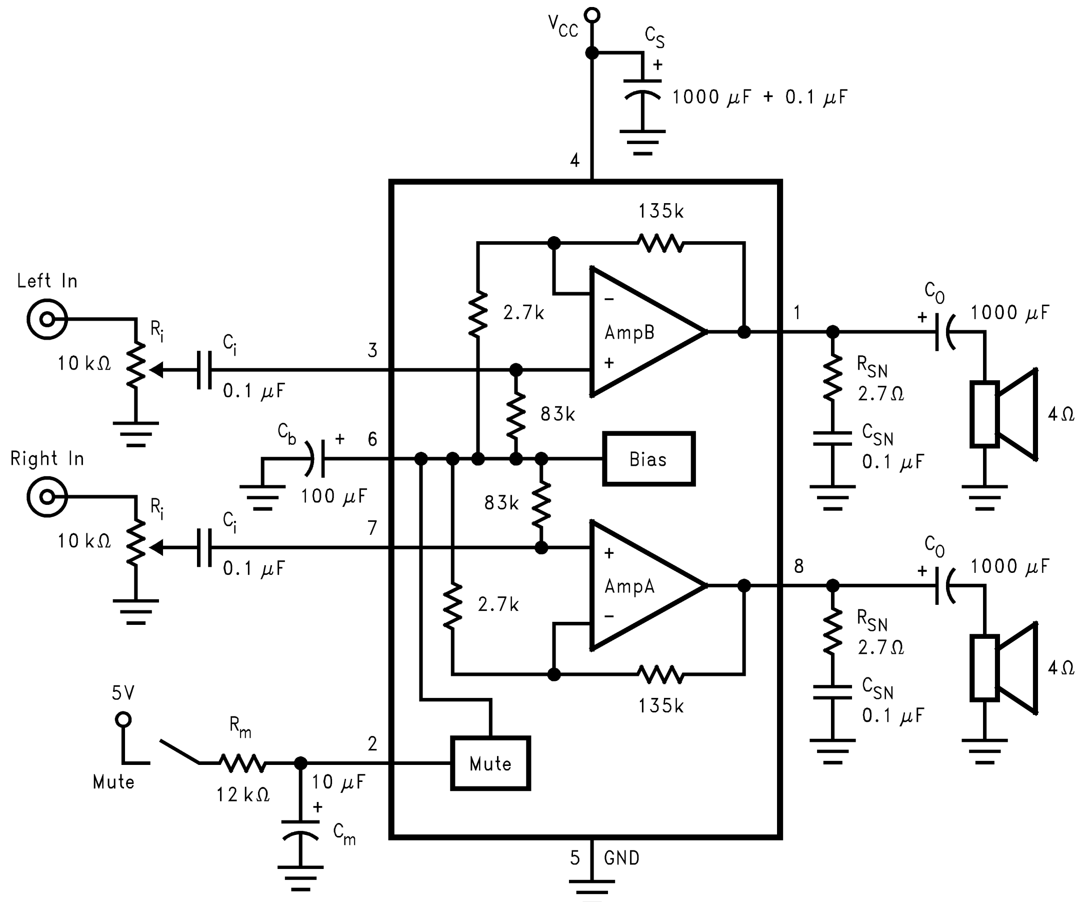


Figure 4. Circuit for External Components Description

EXTERNAL COMPONENTS DESCRIPTION

Components		Function Description
1, 2	C_S	Provides power supply filtering and bypassing.
3, 4	R_{SN}	Works with C_{SN} to stabilize the output stage from high frequency oscillations.
5, 6	C_{SN}	Works with R_{SN} to stabilize the output stage from high frequency oscillations.
7	C_b	Provides filtering for the internally generated half-supply bias generator.
8, 9	C_i	Input AC coupling capacitor which blocks DC voltage at the amplifier's input terminals. Also creates a high pass filter with fc=1/(2 • π • Rin • Cin).
10, 11	C_o	Output AC coupling capacitor which blocks DC voltage at the amplifier's output terminal. Creates a high pass filter with fc=1/(2 • π • Rout • Cout).
12, 13	R_i	Voltage control - limits the voltage level allowed to the amplifier's input terminals.
14	R_m	Works with C_m to provide mute function timing.
15	C_m	Works with R_m to provide mute function timing.

TYPICAL PERFORMANCE CHARACTERISTICS

Typicals are measured at 25°C and represent the parametric norm.

THD+N vs Output Power

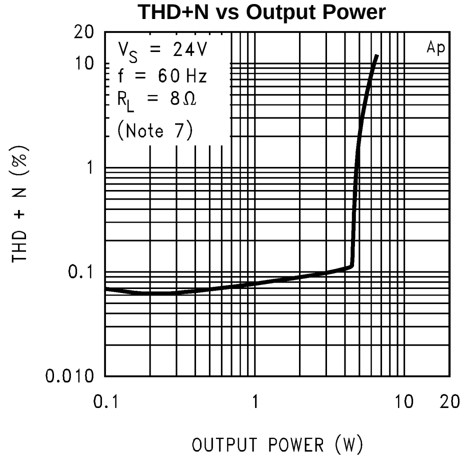


Figure 5.

THD+N vs Output Power

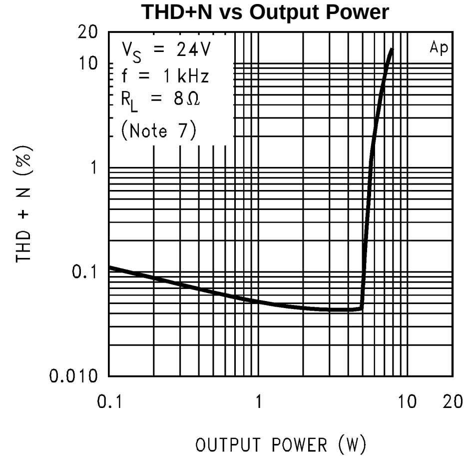


Figure 6.

THD+N vs Output Power

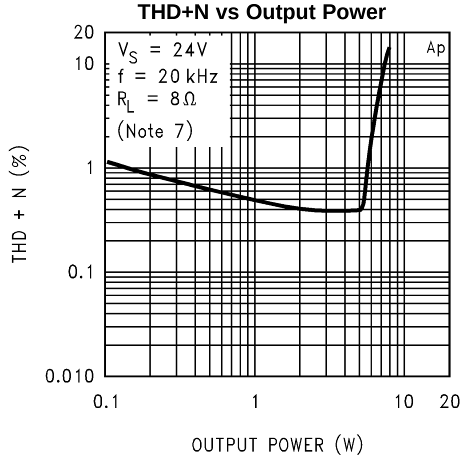


Figure 7.

THD+N vs Output Power

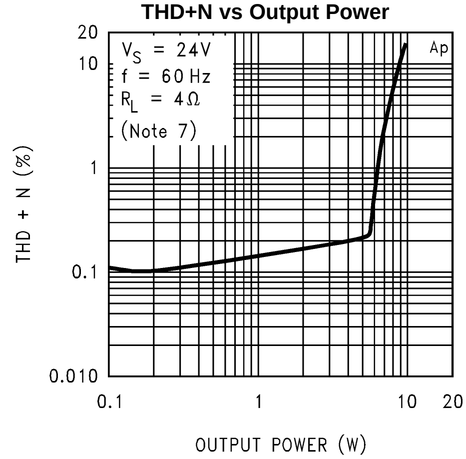


Figure 8.

THD+N vs Output Power

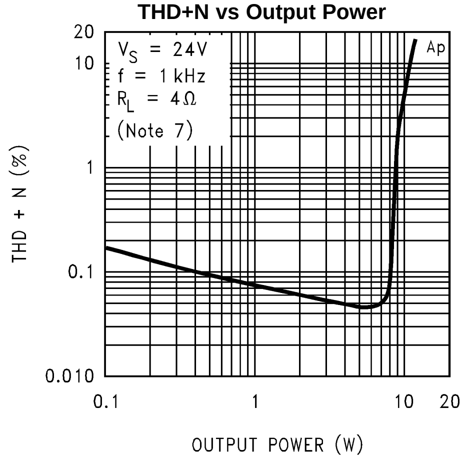


Figure 9.

THD+N vs Output Power

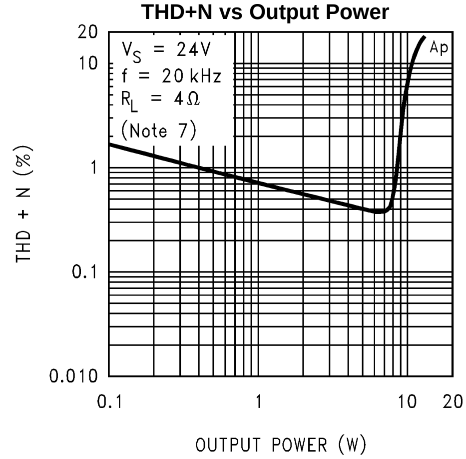


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Typicals are measured at 25°C and represent the parametric norm.

THD+N vs Output Power

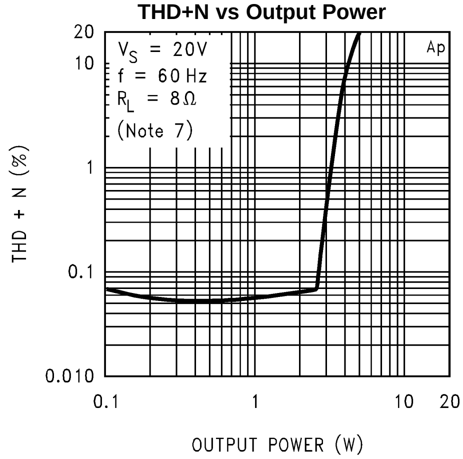


Figure 11.

THD+N vs Output Power

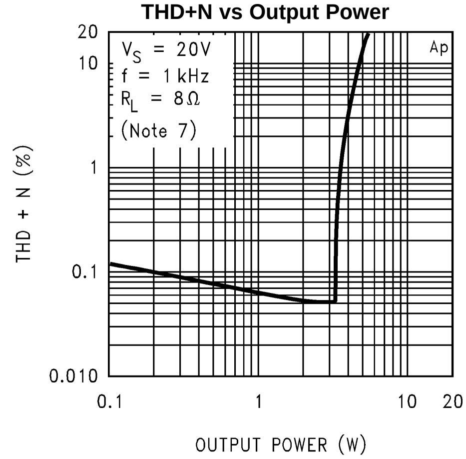


Figure 12.

THD+N vs Output Power

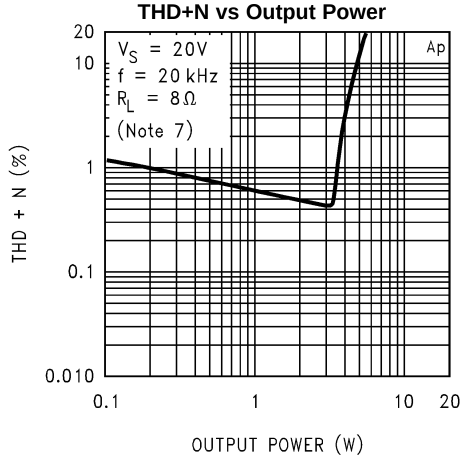


Figure 13.

THD+N vs Output Power

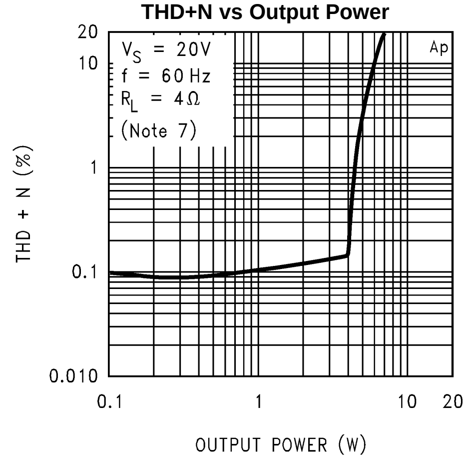


Figure 14.

THD+N vs Output Power

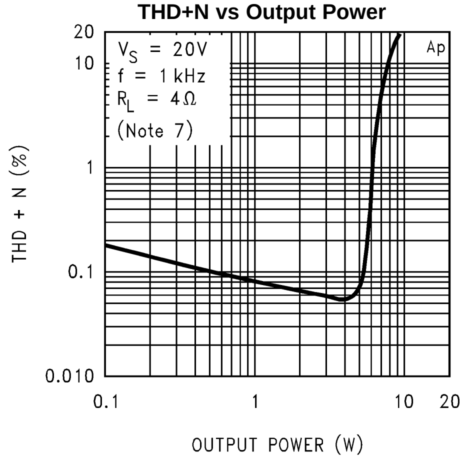


Figure 15.

THD+N vs Output Power

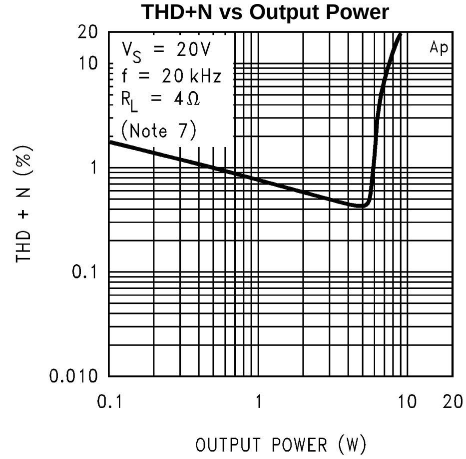


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Typicals are measured at 25°C and represent the parametric norm.

THD+N vs Output Power

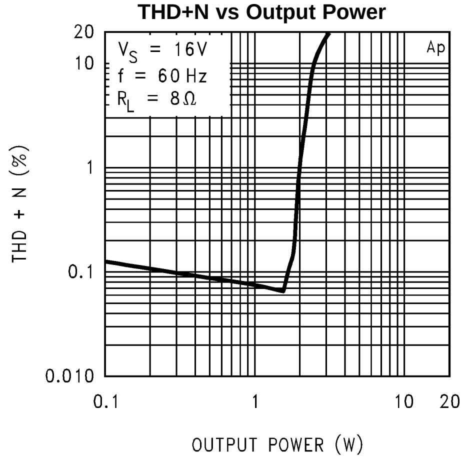


Figure 17.

THD+N vs Output Power

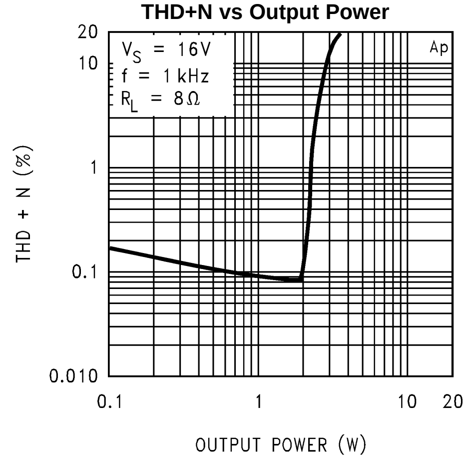


Figure 18.

THD+N vs Output Power

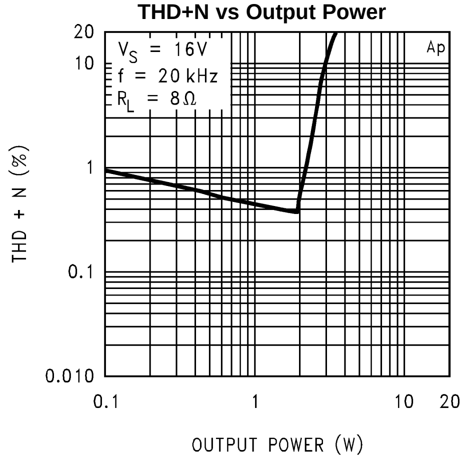


Figure 19.

THD+N vs Output Power

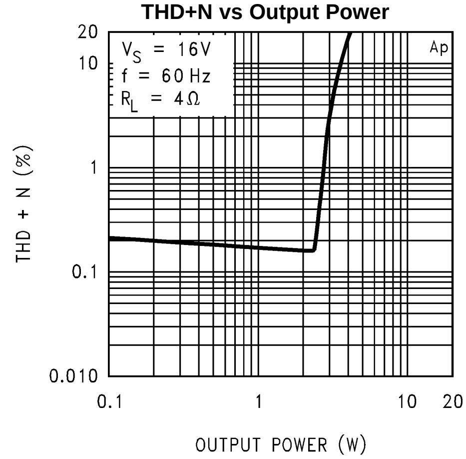


Figure 20.

THD+N vs Output Power

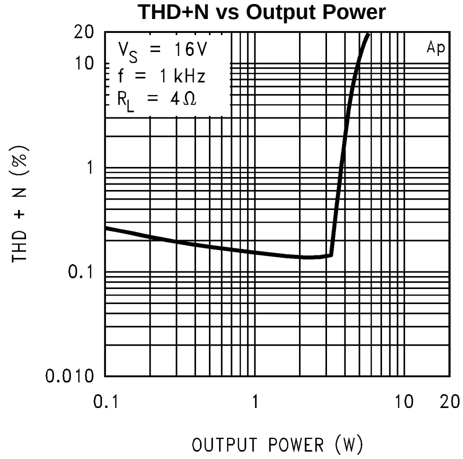


Figure 21.

THD+N vs Output Power

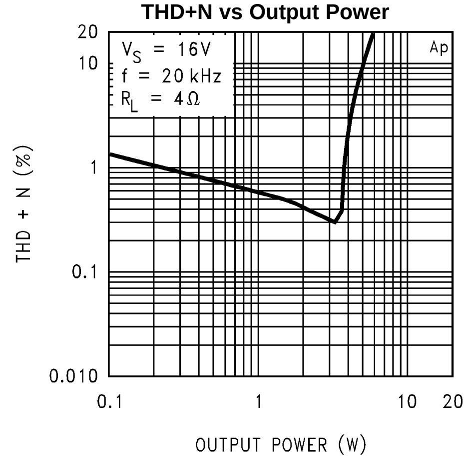


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Typicals are measured at 25°C and represent the parametric norm.

THD+N vs Output Power

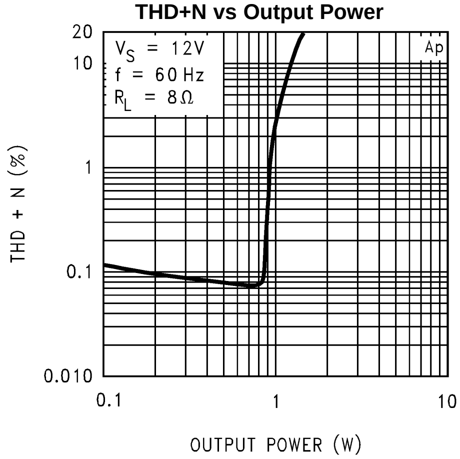


Figure 23.

THD+N vs Output Power

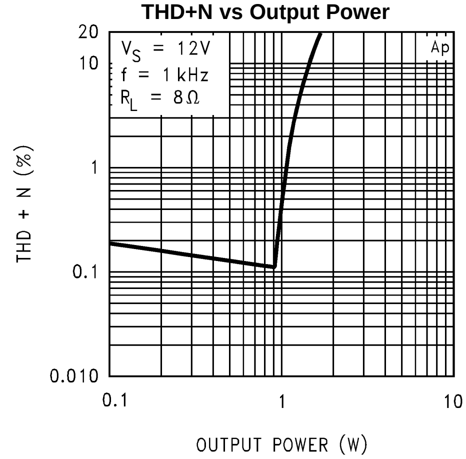


Figure 24.

THD+N vs Output Power

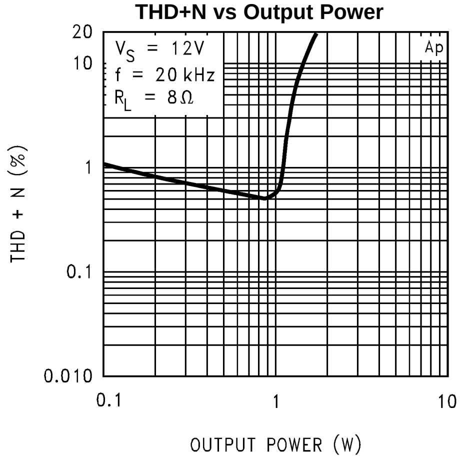


Figure 25.

THD+N vs Output Power

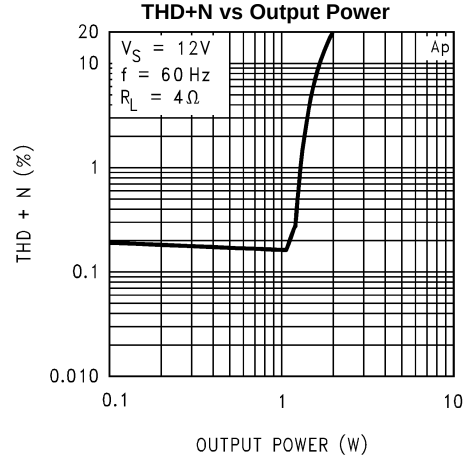


Figure 26.

THD+N vs Output Power

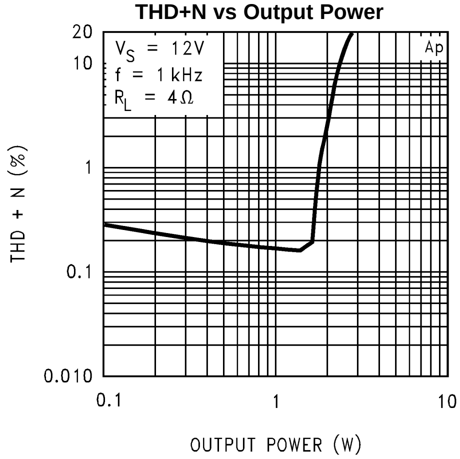


Figure 27.

THD+N vs Output Power

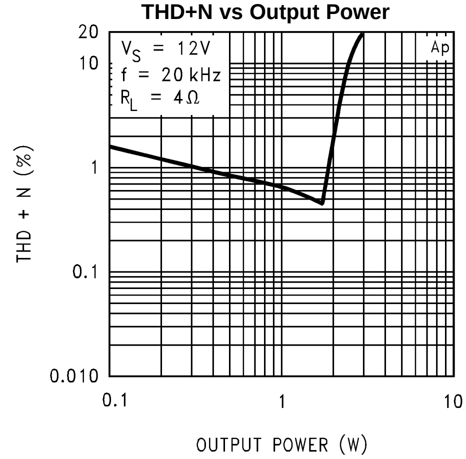


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Typicals are measured at 25°C and represent the parametric norm.

Output Power vs Supply Voltage

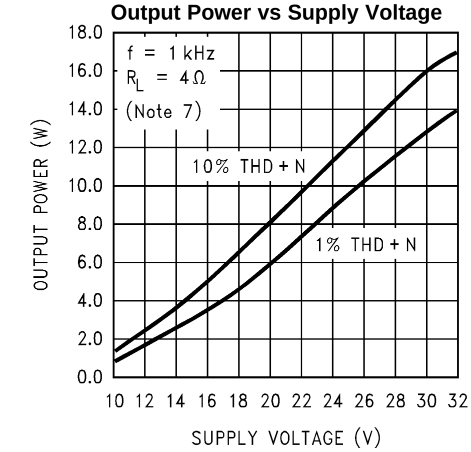


Figure 29.

Output Power vs Supply Voltage

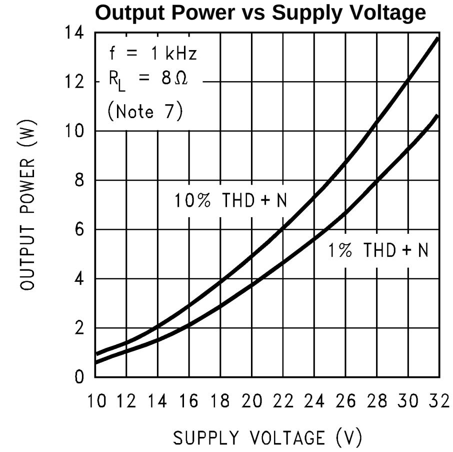


Figure 30.

Frequency Response

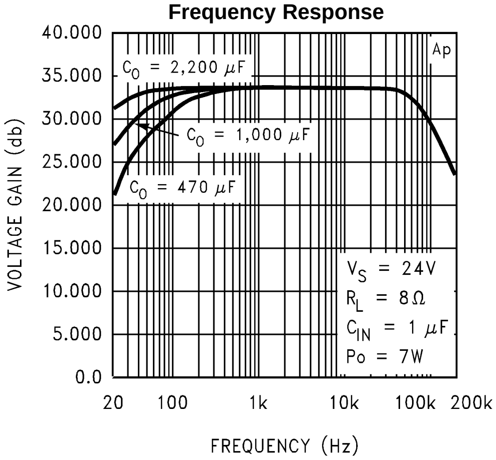


Figure 31.

THD+N vs Frequency

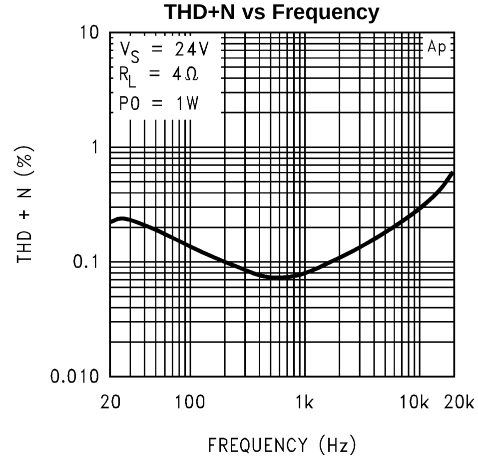


Figure 32.

THD+N vs Frequency

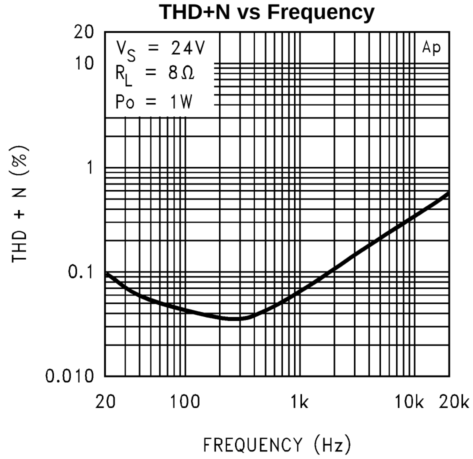


Figure 33.

Frequency Response

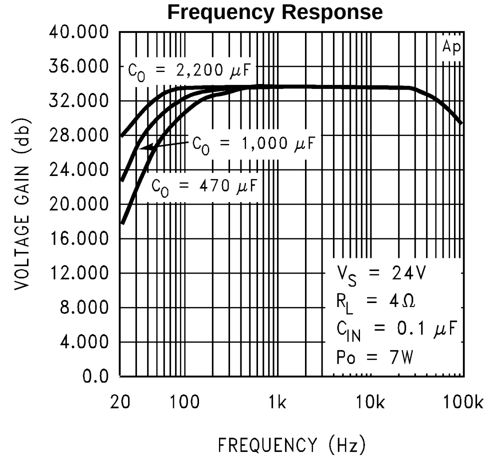


Figure 34.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Typicals are measured at 25°C and represent the parametric norm.

Channel Separation

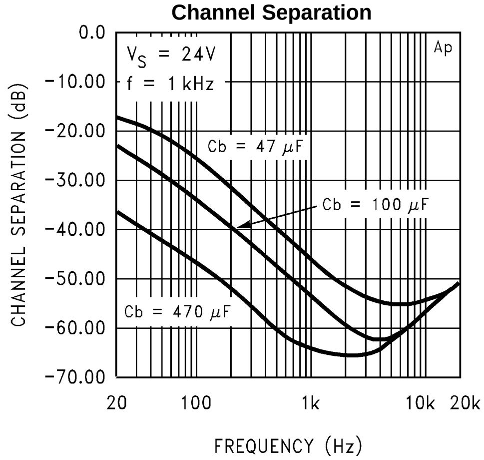


Figure 35.

PSRR vs Frequency

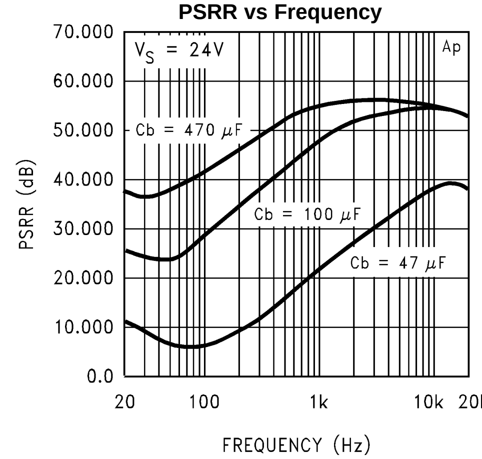


Figure 36.

Supply Current vs Supply Voltage

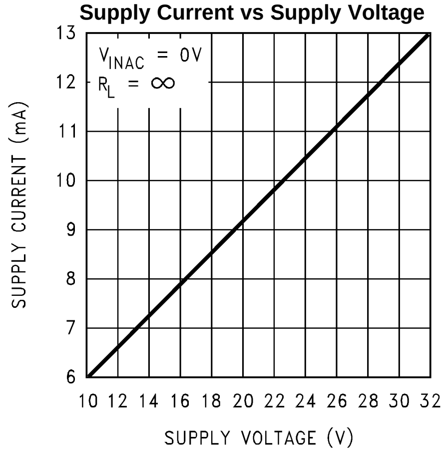


Figure 37.

Power Derating Curve

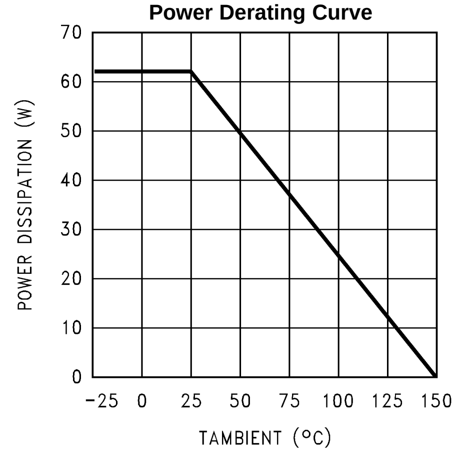


Figure 38.

Power Dissipation vs Output Power

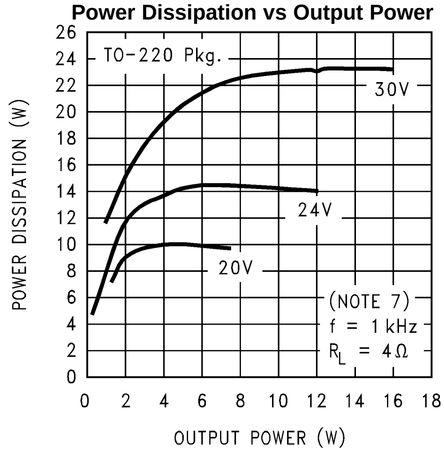


Figure 39.

Power Dissipation vs Output Power

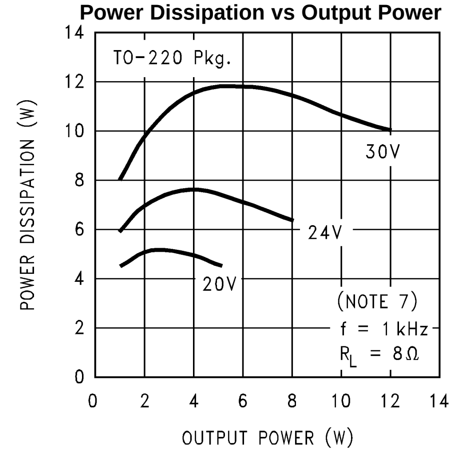


Figure 40.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Typicals are measured at 25°C and represent the parametric norm.

Power Dissipation vs Output Power

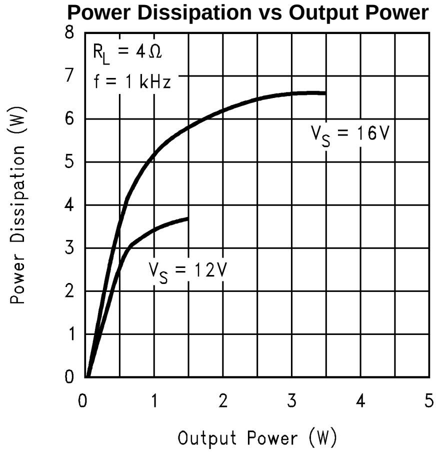


Figure 41.

Power Dissipation vs Output Power

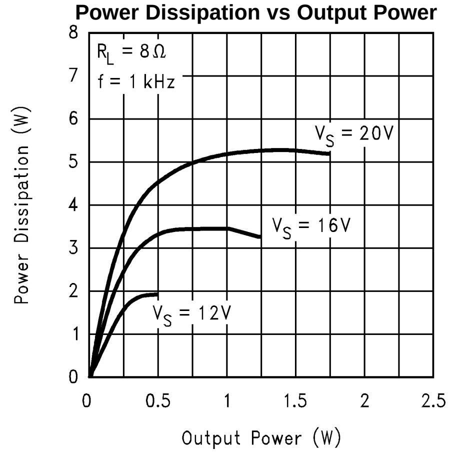


Figure 42.

APPLICATION INFORMATION

The LM4755 contains circuitry to pull down the bias line internally, effectively shutting down the input stage. An external R-C should be used to adjust the timing of the pull-down. If the bias line is pulled down too quickly, currents induced in the internal bias resistors will cause a momentary DC voltage to appear across the inputs of each amplifier's internal differential pair, resulting in an output DC shift towards Vsupply. An R-C timing circuit should be used to limit the pull-down time such that output “pops” and signal feedthroughs will be minimized. The pull-down timing is a function of a number of factors, including the internal mute circuitry, the voltage used to activate the mute, the bias capacitor, the half-supply voltage, and internal resistances used in the half-supply generator. Table 1 shows a list of recommended values for the external R-C.

Table 1. RECOMMENDED VALUES FOR MUTE CIRCUIT

V_{MUTE}	V_{CC}	Rm	Cm
5V	12V	18 kΩ	10 µF
5V	15V	18 kΩ	10 µF
5V	20V	12 kΩ	10 µF
5V	24V	12 kΩ	10 µF
5V	28V	8.2 kΩ	10 µF
5V	30V	8.2 kΩ	10 µF

CAPACITOR SELECTION AND FREQUENCY RESPONSE

With the LM4755, as in all single supply amplifiers, AC coupling capacitors are used to isolate the DC voltage present at the inputs (pins 3, 7) and outputs (pins 1, 8). As mentioned earlier in the EXTERNAL COMPONENTS DESCRIPTION section these capacitors create high-pass filters with their corresponding input/output impedances. The Typical Application Circuit shown in Figure 1 shows input and output capacitors of 0.1 µF and 1,000 µF respectively. At the input, with an 83 kΩ typical input resistance, the result is a high pass 3 dB point occurring at 19 Hz. There is another high pass filter at 39.8 Hz created with the output load resistance of 4Ω. Careful selection of these components is necessary to ensure that the desired frequency response is obtained. The Frequency Response curves in the TYPICAL PERFORMANCE CHARACTERISTICS section show how different output coupling capacitors affect the low frequency roll-off.

OPERATING IN BRIDGE-MODE

Though designed for use as a single-ended amplifier, the LM4755 can be used to drive a load differentially (bridge-mode). Due to the low pin count of the package, only the non-inverting inputs are available. An inverted signal must be provided to one of the inputs. This can easily be done with the use of an inexpensive op-amp configured as a standard inverting amplifier. An LF353 is a good low-cost choice. Care must be taken, however, for a bridge-mode amplifier must theoretically dissipate four times the power of a single-ended type. The load seen by each amplifier is effectively half that of the actual load being used, thus an amplifier designed to drive a 4Ω load in single-ended mode should drive an 8Ω load when operating in bridge-mode.

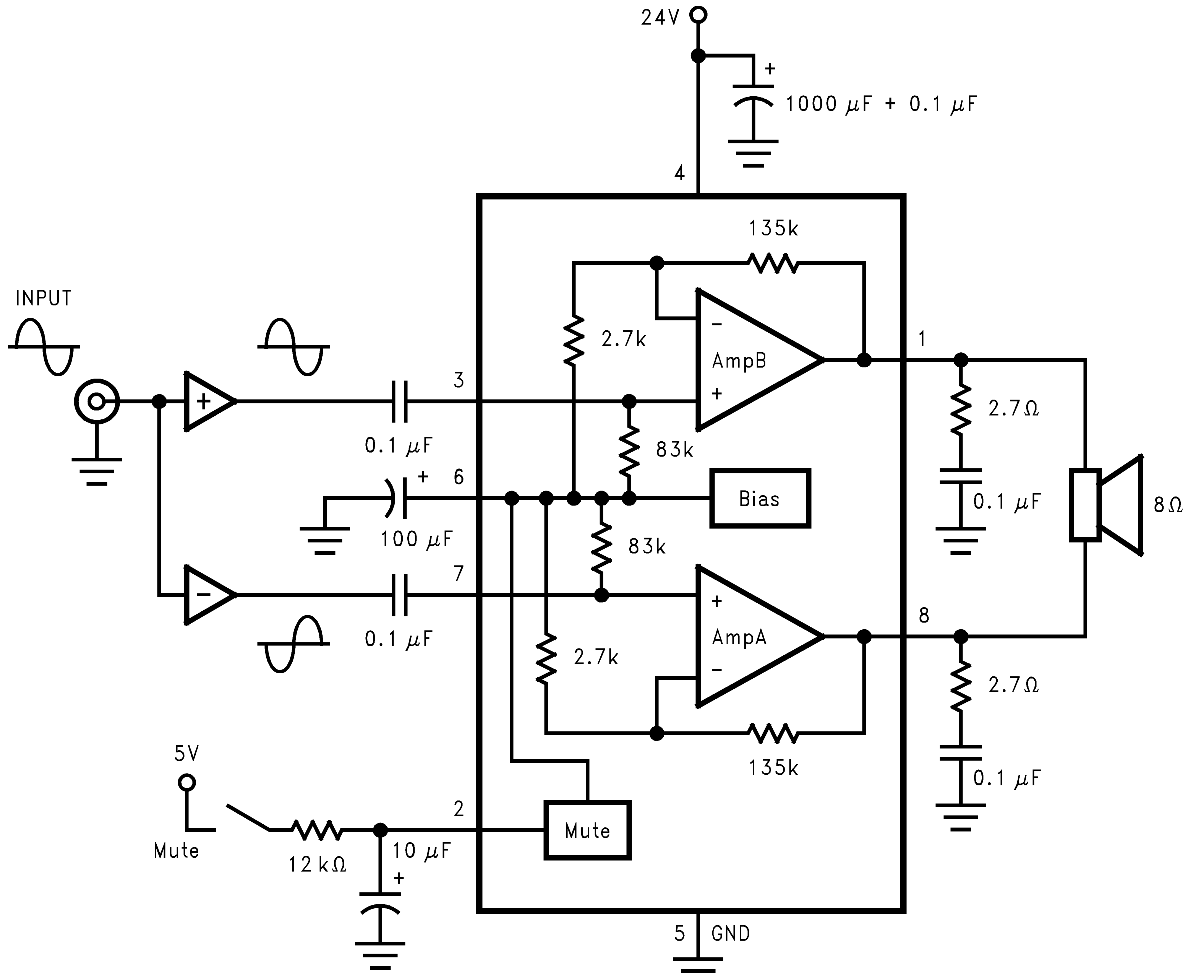


Figure 43. Bridge-Mode Application

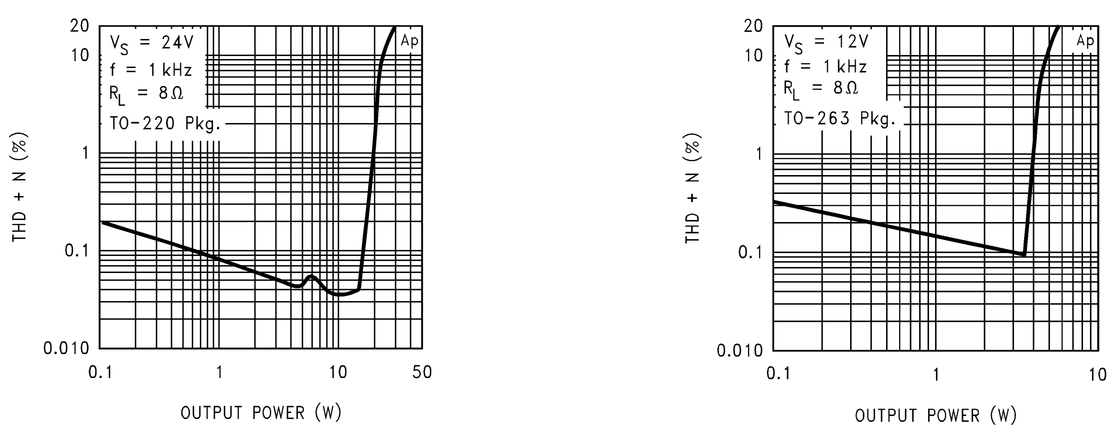


Figure 44. THD+N vs P_{OUT} for Bridge-Mode Application

PREVENTING OSCILLATIONS

With the integration of the feedback and bias resistors on-chip, the LM4755 fits into a very compact package. However, due to the close proximity of the non-inverting input pins to the corresponding output pins, the inputs should be AC terminated at all times. If the inputs are left floating, the amplifier will have a positive feedback path through high impedance coupling, resulting in a high frequency oscillation. In most applications, this termination is typically provided by the previous stage's source impedance. If the application will require an external signal, the inputs should be terminated to ground with a resistance of 50 kΩ or less on the AC side of the input coupling capacitors.

UNDERVOLTAGE SHUTDOWN

If the power supply voltage drops below the minimum operating supply voltage, the internal under-voltage detection circuitry pulls down the half-supply bias line, shutting down the preamp section of the LM4755. Due to the wide operating supply range of the LM4755, the threshold is set to just under 9V. There may be certain applications where a higher threshold voltage is desired. One example is a design requiring a high operating supply voltage, with large supply and bias capacitors, and there is little or no other circuitry connected to the main power supply rail. In this circuit, when the power is disconnected, the supply and bias capacitors will discharge at a slower rate, possibly resulting in audible output distortion as the decaying voltage begins to clip the output signal. An external circuit may be used to sense for the desired threshold, and pull the bias line (pin 6) to ground to disable the input preamp. Figure 45 shows an example of such a circuit. When the voltage across the zener diode drops below its threshold, current flow into the base of Q1 is interrupted. Q2 then turns on, discharging the bias capacitor. This discharge rate is governed by several factors, including the bias capacitor value, the bias voltage, and the resistor at the emitter of Q2. An equation for approximating the value of the emitter discharge resistor, R, is given below:

$$R = (0.7v) / (Cb \bullet (V_{CC}/2) / 0.1s) \quad (1)$$

Note that this is only a linearized approximation based on a discharge time of 0.1s. The circuit should be evaluated and adjusted for each application.

As mentioned earlier in the Built-in Mute Circuit section, when using an external circuit to pull down the bias line, the rate of discharge will have an effect on the turn-off induced distortions. Please refer to the Table 1 section for more information.

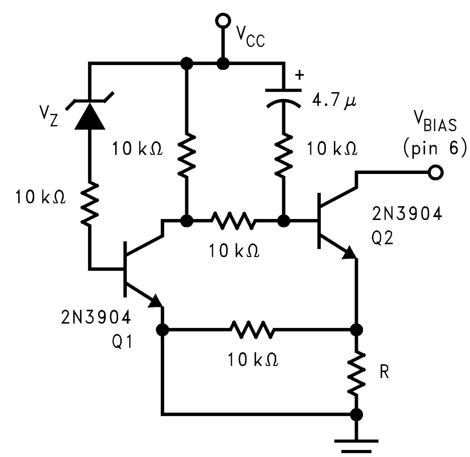


Figure 45. External Undervoltage Pull-Down

THERMAL CONSIDERATIONS

Heat Sinking

Proper heatsinking is necessary to ensure that the amplifier will function correctly under all operating conditions. A heatsink that is too small will cause the die to heat excessively and will result in a degraded output signal as the thermal protection circuitry begins to operate.

The choice of a heatsink for a given application is dictated by several factors: the maximum power the IC needs to dissipate, the worst-case ambient temperature of the circuit, the junction-to-case thermal resistance, and the maximum junction temperature of the IC. The heat flow approximation equation used in determining the correct heatsink maximum thermal resistance is given below:

$T_J – T_A = P_{DMAX} \bullet (\theta_{JC} + \theta_{CS} + \theta_{SA})$

where

- P_{DMAX} = maximum power dissipation of the IC
- T_J(°C) = junction temperature of the IC
- T_A(°C) = ambient temperature
- θ_{JC}(°C/W) = junction-to-case thermal resistance of the IC
- θ_{CS}(°C/W) = case-to-heatsink thermal resistance (typically 0.2 to 0.5 °C/W)
- θ_{SA}(°C/W) = thermal resistance of heatsink (2)

When determining the proper heatsink, the above equation should be re-written as:

$\theta_{SA} \leq [(T_J – T_A) / P_{DMAX}] - \theta_{JC} – \theta_{CS}$ (3)

DDPAK HEATSINKING

Surface mount applications will be limited by the thermal dissipation properties of printed circuit board area. The DDPAK package is not recommended for surface mount applications with V_S > 16V due to limited printed circuit board area. There are DDPAK package enhancements, such as clip-on heatsinks and heatsinks with adhesives, that can be used to improve performance.

Standard FR-4 single-sided copper clad will have an approximate Thermal resistance (θ_{SA}) ranging from:

1.5 × 1.5 in. sq.	20–27°C/W	(T_A=28°C, Sine wave testing, 1 oz. Copper)
2 × 2 in. sq.	16–23°C/W	

The above values for θ_{SA} vary widely due to dimensional proportions (i.e. variations in width and length will vary θ_{SA}).

For audio applications, where peak power levels are short in duration, this part will perform satisfactory with less heatsinking/copper clad area. As with any high power design proper bench testing should be undertaken to assure the design can dissipate the required power. Proper bench testing requires attention to worst case ambient temperature and air flow. At high power dissipation levels the part will show a tendency to increase saturation voltages, thus limiting the undistorted power levels.

DETERMINING MAXIMUM POWER DISSIPATION

For a single-ended class AB power amplifier, the theoretical maximum power dissipation point is a function of the supply voltage, V_S, and the load resistance, R_L and is given by the following equation:

(single channel)

P_{DMAX} (W) = $[V_S^2 / (2 \bullet \pi^2 \bullet R_L)]$

The above equation is for a single channel class-AB power amplifier. For dual amplifiers such as the LM4755, the equation for calculating the total maximum power dissipated is:

(dual channel)

P_{DMAX} (W) = $2 \bullet [V_S^2 / (2 \bullet \pi^2 \bullet R_L)]$

or

$V_S^2 / (\pi^2 \bullet R_L)$

(Bridged Outputs)

P_{DMAX} (W) = $4[V_S^2 / (2\pi^2 \bullet R_L)]$

HEATSINK DESIGN EXAMPLE

Determine the system parameters:

$V_S = 24V$	Operating Supply Voltage
$R_L = 4\Omega$	Minimum Load Impedance
$T_A = 55°C$	Worst Case Ambient Temperature

Device parameters from the datasheet:

$T_J = 150°C$	Maximum Junction Temperature
$\theta_{JC} = 2°C/W$	Junction-to-Case Thermal Resistance

Calculations:

$2 \bullet P_{DMAX} = 2 \bullet [V_S^2 / 2 \bullet \pi^2 \bullet R_L)] = (24V)^2 / (2 \bullet \pi^2 \bullet 4\Omega) = 14.6W$

$\theta_{SA} \leq [(T_J\text{-}T_A) / P_{DMAX}] - \theta_{JC} – \theta_{CS} = [(150°C - 55°C) / 14.6W] - 2°C/W – 0.2°C/W = 4.3°C/W$

Conclusion: Choose a heatsink with $\theta_{SA} \leq 4.3°C/W$.

DDPAK HEATSINK DESIGN EXAMPLES

Example 1: (Stereo Single-Ended Output)

Given: T_A=30°C

T_J=150°C

R_L=4Ω

V_S=12V

θ_{JC}=2°C/W

P_{DMAX} from P_D vs P_O Graph:

$$P_{DMAX} \approx 3.7W \quad (4)$$

Calculating P_{DMAX}:

$$P_{DMAX} = V_{CC}^2/(\pi^2 R_L) = (12V)^2/\pi^2(4\Omega)) = 3.65W \quad (5)$$

Calculating Heatsink Thermal Resistance:

$$\theta_{SA} < T_J - T_A / P_{DMAX} - \theta_{JC} - \theta_{CS} \quad (6)$$

$$\theta_{SA} < 120°C/3.7W - 2.0°C/W - 0.2°C/W = 30.2°C/W \quad (7)$$

Therefore the recommendation is to use 1.5 × 1.5 square inch of single-sided copper clad.

Example 2: (Stereo Single-Ended Output)

Given: T_A=50°C

T_J=150°C

R_L=4Ω

V_S=12V

θ_{JC}=2°C/W

P_{DMAX} from P_D vs P_O Graph:

$$P_{DMAX} \approx 3.7W \quad (8)$$

Calculating P_{DMAX}:

$$P_{DMAX} = V_{CC}^2/(\pi^2 R_L)= (12V)^2/(\pi^2(4\Omega)) = 3.65W \quad (9)$$

Calculating Heatsink Thermal Resistance:

$$\theta_{SA} < [(T_J - T_A) / P_{DMAX}] - \theta_{JC} - \theta_{CS} \quad (10)$$

$$\theta_{SA} < 100°C/3.7W − 2.0°C/W − 0.2°C/W = 24.8°C/W \quad (11)$$

Therefore the recommendation is to use 2.0 × 2.0 square inch of single-sided copper clad.

Example 3: (Bridged Output)

Given: T_A=50°C

T_J=150°C

R_L=8Ω

V_S=12V

θ_{JC}=2°C/W

Calculating P_{DMAX}:

$$P_{DMAX} = 4[V_{CC}^2/(2\pi^2 R_L)] = 4(12V)^2/(2\pi^2(8\Omega)) = 3.65W \quad (12)$$

Calculating Heatsink Thermal Resistance:

$$\theta_{SA} < [(T_J − T_A) / P_{DMAX}] − \theta_{JC} − \theta_{CS} \quad (13)$$

$$\theta_{SA} < 100°C / 3.7W − 2.0°C/W − 0.2°C/W = 24.8°C/W \quad (14)$$

Therefore the recommendation is to use 2.0 × 2.0 square inch of single-sided copper clad.

LAYOUT AND GROUND RETURNS

Proper PC board layout is essential for good circuit performance. When laying out a PC board for an audio power amplifier, particular attention must be paid to the routing of the output signal ground returns relative to the input signal and bias capacitor grounds. To prevent any ground loops, the ground returns for the output signals should be routed separately and brought together at the supply ground. The input signal grounds and the bias capacitor ground line should also be routed separately. The 0.1 µF high frequency supply bypass capacitor should be placed as close as possible to the IC.

PC BOARD LAYOUT-COMPOSITE

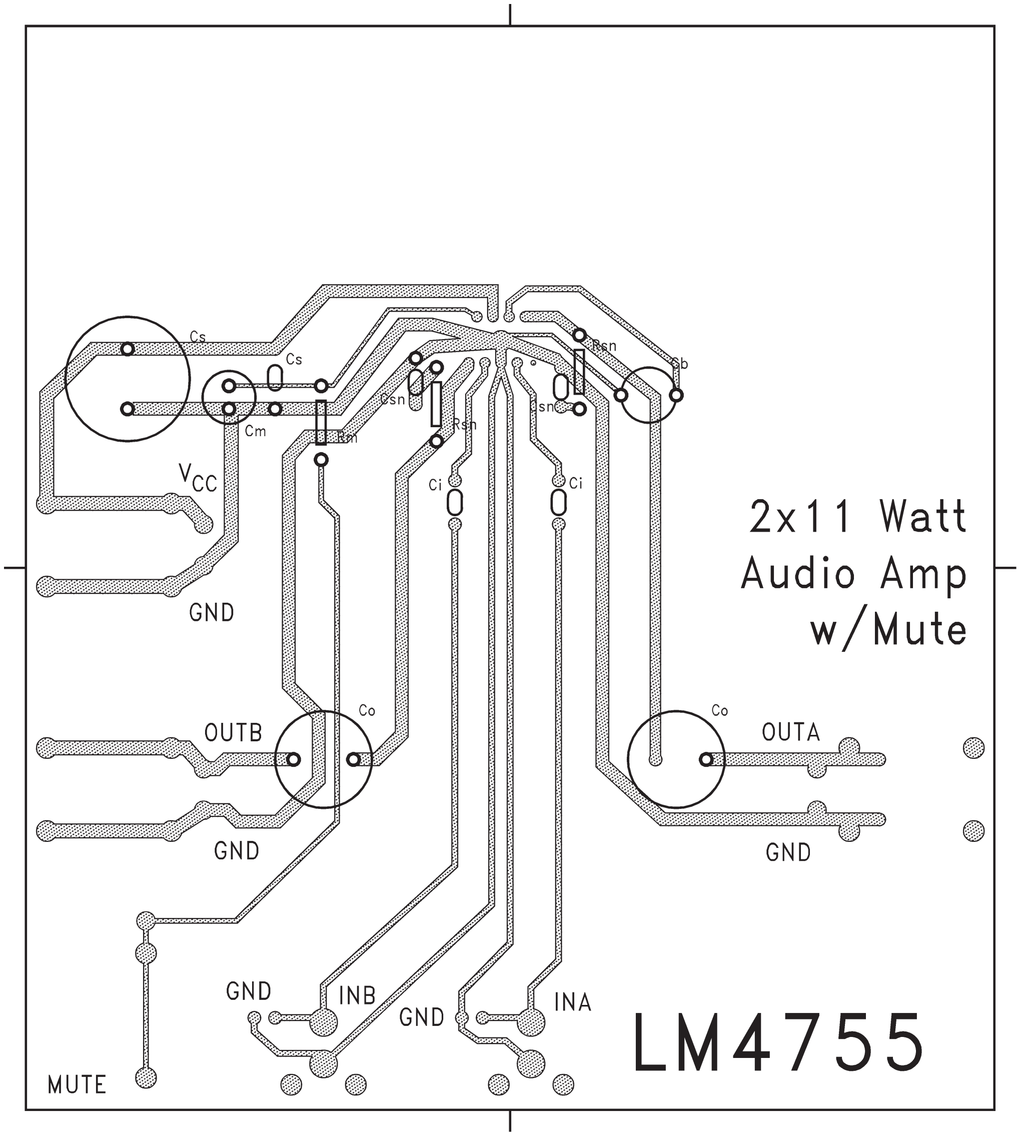


Figure 46.

PC BOARD LAYOUT-SILK SCREEN

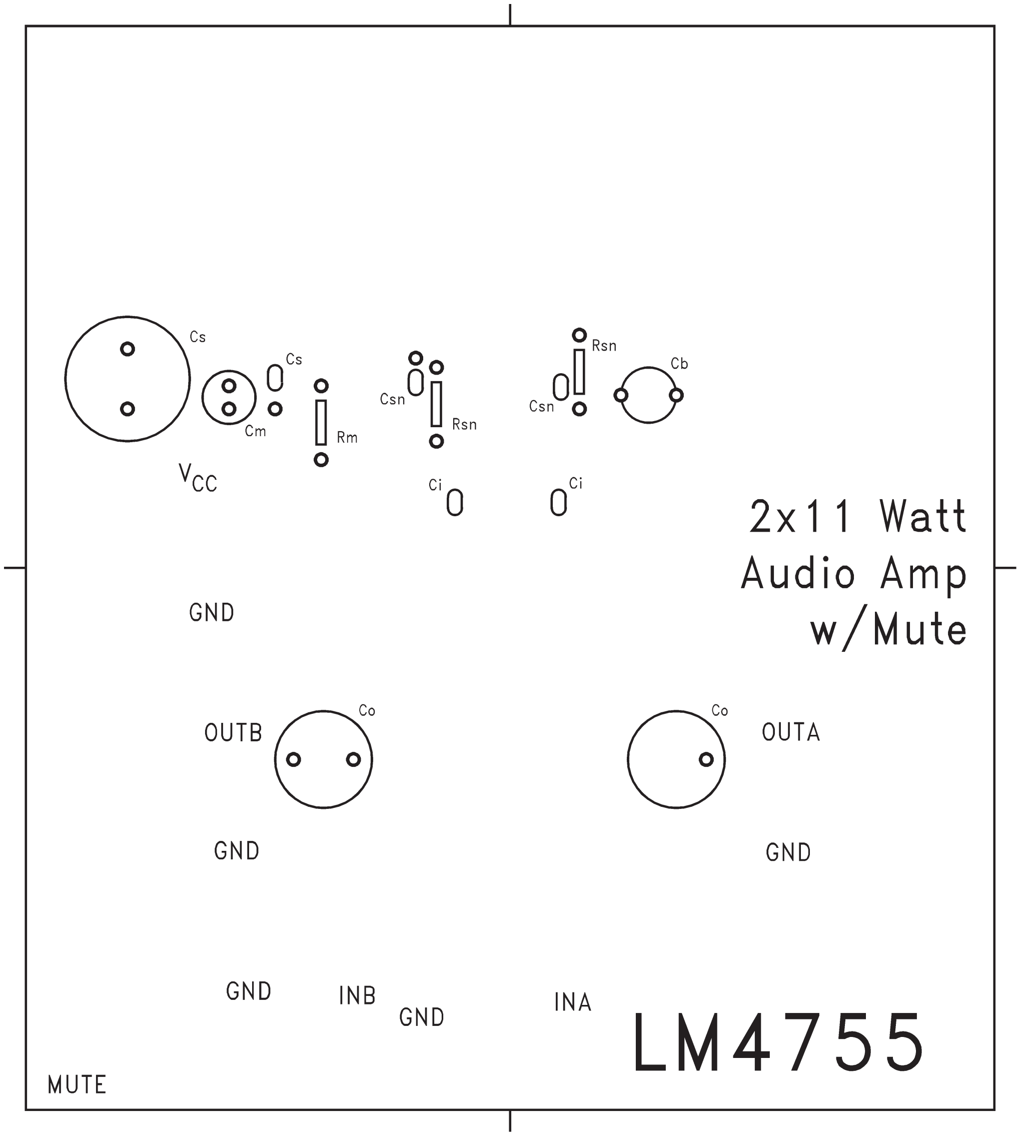


Figure 47.

PC BOARD LAYOUT-SOLDER SIDE

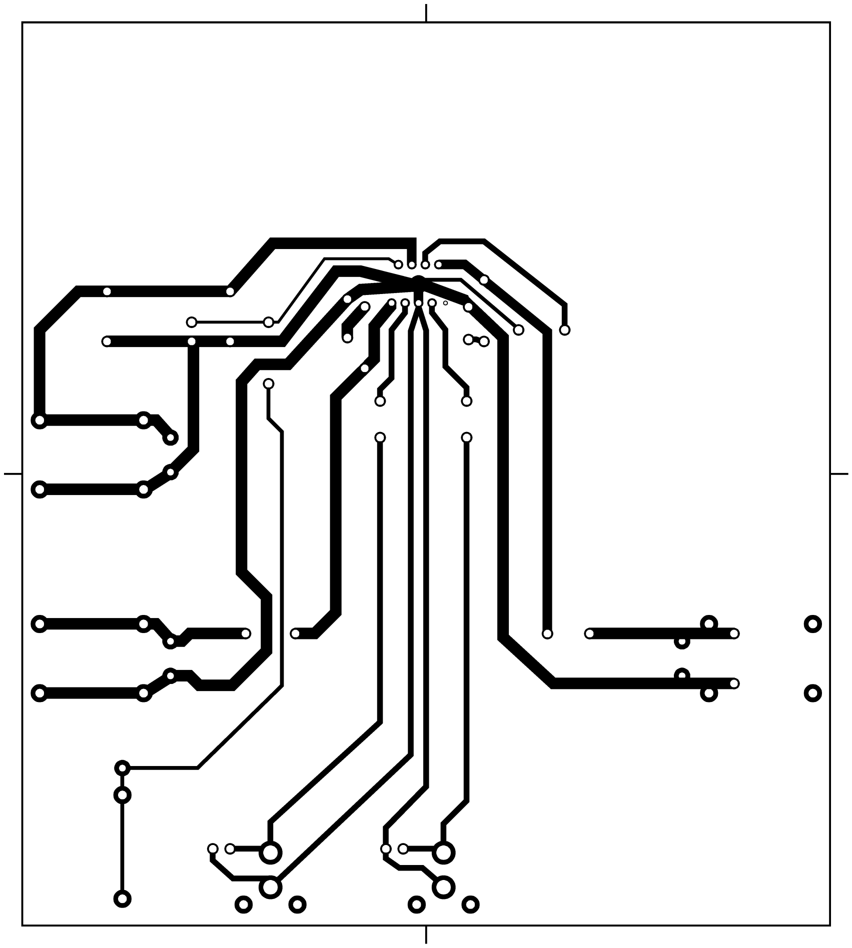


Figure 48.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	22

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265