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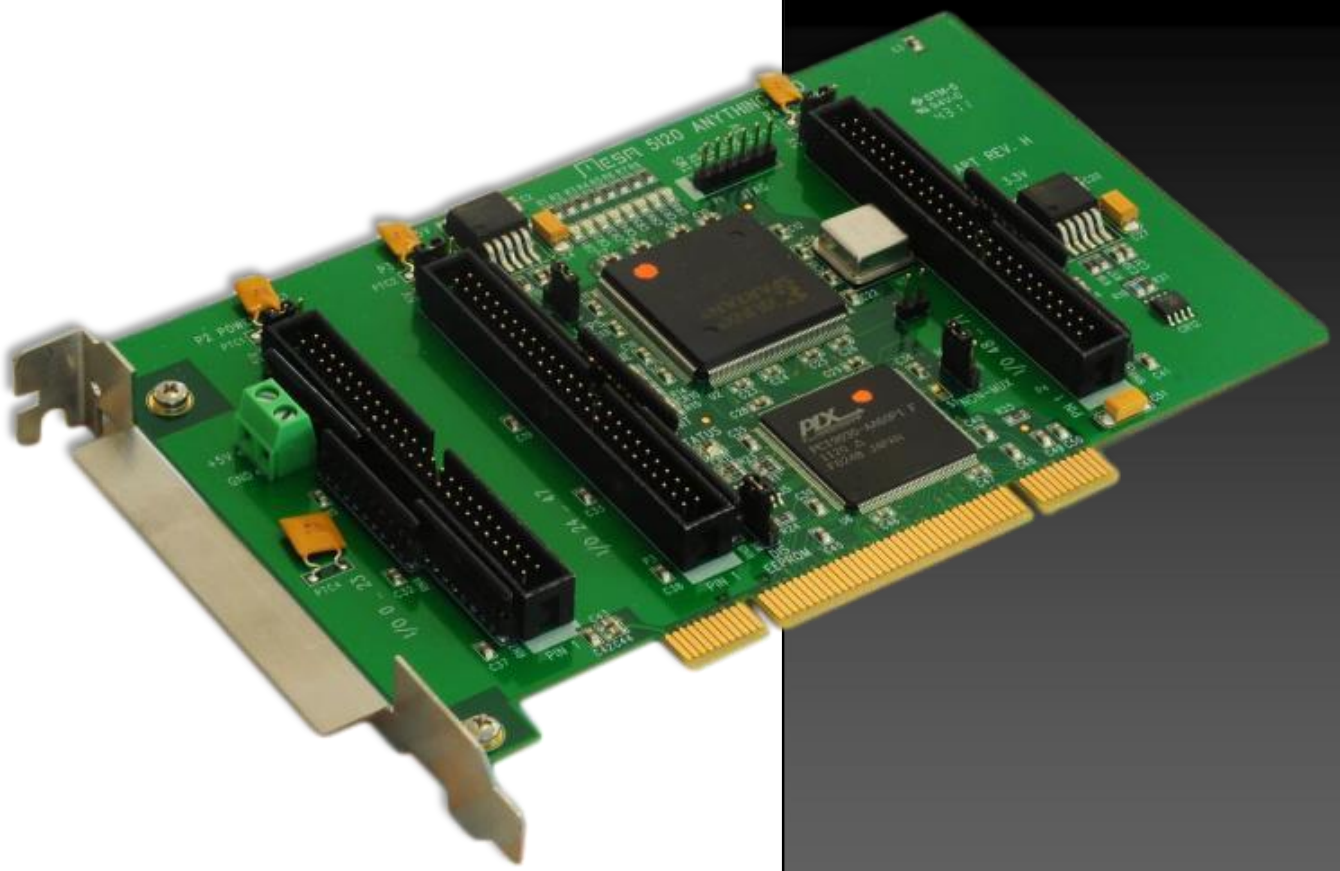
CNCPROM

MESA 5I20



GENERAL

DESCRIPTION

The MESA 5I20 is a general purpose programmable I/O card for the PCI bus. The 5I20 uses a 200K gate Xilinx FPGA for all logic, so it is truly an "Anything I/O" card. The FPGA is downloadable from the PCI bus side, allowing creation of almost any kind of specialized I/O function, even including micro-controllers in the FPGA.

Several pre-made functions are provided, including a 72 bit parallel I/O card with three 24 bit ports a 12 channel host based servo motor controller, a 8 channel micro-controller based servo motor controller (*Soft*DMC), and a 8 channel, 32 bit timer counter card capable of running at 100 MHz. VHDL source is provided for all examples.

All I/O bits are 5V tolerant and can sink 24 mA. Pullup resistors are provided for all pins so that they may be connected directly to opto-isolators, contacts etc.

The 5I20 uses three 50 pin connectors with I/O module rack compatible pinouts and interleaved grounds.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 5I20 card is oriented in an upright position, that is, with the PCI connector towards the person doing the configuration.

MULTIPLEXED/NON MULTIPLEXED MODE

The local bus interface from the PCI bridge chip to the FPGA can operate in two modes. Multiplexed and Non-multiplexed. In multiplexed mode the local bus addresses are presented on the data lines at the beginning of the local bus cycle. In non-multiplexed mode, the addresses are presented on separate local bus address pins. The multiplexed mode has the advantage that all 32 address bits are available to the FPGA chip. The disadvantage is that the FPGA configuration must latch the addresses. The Multiplexed mode is the default, and all of the provided FPGA configurations assume that the multiplexed mode is used.

W5	**MODE**
UP	MULTIPLEXED (DEFAULT)
DOWN	NON-MULTPLEXED

PULLUP ENABLE

The Xilinx FPGA on the 5I20 has the option of having weak pullups on all I/O pins at powerup or reset. The default is to enable the pullups so that the FPGA/PCI bridge chip interface pins are not floated when the FPGA is in an unconfigured state. To enable the built-in pullups, (the default condition) jumper W4 should be placed in the down position. To disable the internal pullups, W4 should be in the up position.

EEPROM ENABLE

The PLX9030 PCI-Local bus bridge chip is configured at power up via a serial EEPROM. If the EEPROM is somehow mis-programmed or corrupted, it can be impossible to re-write the EEPROM from the PCI bus. To avoid this problem, The EEPROM can be temporarily disabled. W6 controls the EEPROM enable function, When W6 is in the up position (default) the EEPROM is enabled. When W6 is in the down position, the EEPROM is disabled.

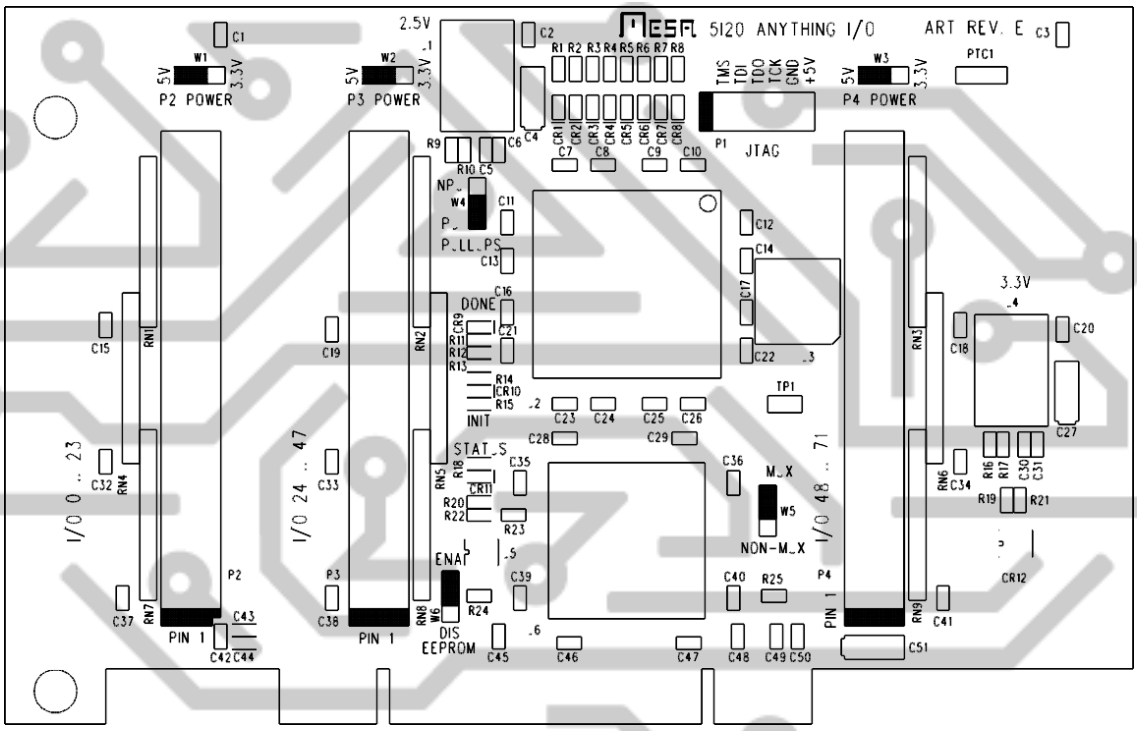
HARDWARE CONFIGURATION

CONNECTOR POWER

The power connection on the I/O connectors can supply either 3.3V or 5V power. Supplied power should be limited to 400 mA total. W1 selects the power supplied to P2, W2 selects the power supplied to P3, and W3 selects the power supplied to P4. When W1, W2 or W3 are in the left position, 5V power is supplied to the connector and associated pullup resistors. When W1, W2, or W3 are in the right position, 3.3V is supplied.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

I/O CONNECTORS

P2, P3, and P4 are the 5I20s I/O connectors. These are 50 pin box headers that mate with standard 50 conductor female IDC connectors. Suggested compatible IDC receptacle is AMP PN 1-1658621-0. For information on which I/O pin connects to which FPGA pin, please see the 5I20IO.PIN file on the 5I20 distribution disk. 5I20 IO connector pinouts are as follows:

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO0	2	GND	3	IO1	4	GND
5	IO2	6	GND	7	IO3	8	GND
9	IO4	10	GND	11	IO5	12	GND
13	IO6	14	GND	15	IO7	16	GND
17	IO8	18	GND	19	IO9	20	GND
21	IO10	22	GND	23	IO11	24	GND
25	IO12	26	GND	27	IO13	28	GND
29	IO14	30	GND	31	IO15	32	GND
33	IO16	34	GND	35	IO17	36	GND
37	IO18	38	GND	39	IO19	40	GND
41	IO20	42	GND	43	IO21	44	GND
45	IO22	46	GND	47	IO23	48	GND
49	POWER	50	GND				

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO24	2	GND	3	IO25	4	GND
5	IO26	6	GND	7	IO27	8	GND
9	IO28	10	GND	11	IO29	12	GND
13	IO30	14	GND	15	IO31	16	GND
17	IO32	18	GND	19	IO33	20	GND
21	IO34	22	GND	23	IO35	24	GND
25	IO36	26	GND	27	IO37	28	GND
29	IO38	30	GND	31	IO39	32	GND
33	IO40	34	GND	35	IO41	36	GND
37	IO42	38	GND	39	IO43	40	GND
41	IO44	42	GND	43	IO45	44	GND
45	IO46	46	GND	47	IO47	48	GND
49	POWER	50	GND				

CONNECTORS

I/O CONNECTORS

P4 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO48	2	GND	3	IO49	4	GND
5	IO50	6	GND	7	IO51	8	GND
9	IO52	10	GND	11	IO53	12	GND
13	IO54	14	GND	15	IO55	16	GND
17	IO56	18	GND	19	IO57	20	GND
21	IO58	22	GND	23	IO59	24	GND
25	IO60	26	GND	27	IO61	28	GND
29	IO62	30	GND	31	IO63	32	GND
33	IO64	34	GND	35	IO65	36	GND
37	IO66	38	GND	39	IO67	40	GND
41	IO68	42	GND	43	IO69	44	GND
45	IO70	46	GND	47	IO71	48	GND
49	POWER	50	GND				

JTAG CONNECTOR PINOUT

P1 is a JTAG programming connector. It is not normally used since the 5I20 can be programmed via the PCI interface, but can be useful when debugging. Note that the /PROGRAM pin must be de-asserted to be able to use the JTAG interface.

P1 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC
1	TMS	2	TDI	3	TDO
4	TCK	5	GND	6	+5V

OPERATION

FPGA

The 5I20 use a Xilinx Spartan-II 200k gate FPGA in a 208 pin QFP package: XC2S200-PQ208.

FPGA PINOUT

The local bus and I/O interface FPGA pinouts are described in the 5I20INFC.PIN and 5I20IO.PIN files in CONFIGS directory of the distribution disk. The 5I20IO.PIN file may be used as a template for custom configurations

MEMORY AND I/O REGIONS

The PLX9030 maps 6 different IO/memory regions into host address space. Two of these address spaces are for PLX9030 configuration register access.

PLX9030 CONFIGURATION REGISTERS

BUS SPACE	MEM - I/O	WIDTH	RANGE
BUS SPACE 0	MEMORY	32 BITS	128 BYTES
BUS SPACE 1	I/O	32 BITS	128 BYTES

The PLX9030 PCI bridge allows for 4 separate memory or I/O regions to be mapped to the local bus that connects to the FPGA. The default EEPROM configuration sets these up as follows:

LOCAL BUS (FPGA) ACCESS AREA

BUS SPACE	MEM - I/O	WIDTH	RANGE
BUS SPACE 2	I/O	16 BITS	256 BYTES (128 WORDS)
BUS SPACE 3	I/O	32 BITS	256 BYTES (64 LONGS)
BUS SPACE 4	MEM	16 BITS	64K BYTE (32K WORDS)
BUS SPACE 5	MEM	32 BITS	64K BYTE (16K LONGS)

Note that the bus space numbers are referred to as BAR indexes in the PLX API documentation.

OPERATION

CONFIGURATION

Before the 5I20 can do anything useful it must have its FPGA configuration data downloaded from the host CPU to the FPGA on the 5I20. This is done by writing a series of bytes from the configuration file to the 5I20 card's configuration data register. Configuration data is written a byte at a time to any of the I/O or memory bus space regions mapped to the 5I20s local bus.

The FPGA configuration control bits must be manipulated before configuration data can be sent to the FPGA. These control bits are controlled via GPIO pins of the PLX9030 PCI bridge. The PLX9030s GPIO pins are connected to the following FPGA configuration pins:

GPIO	DIRECTION	FPGA
GPIO3	IN	DONE
GPIO4	IN	/INIT
GPIO5	OUT	STATUS LED
GPIO7	OUT	/WRITE
GPIO8	OUT	/PROGRAM

The GPIO pin functions and directions are setup by the EEPROM so need not normally be changed. Refer to the PLX 9030 manual if you need low level access to these control bits

SC5I20

A DOS utility program SC5I20.EXE is provided to send configuration files to the 5I20. SC5I20 is usable under DOS and Windows 9X where direct I/O access to the 5I20 card is available. The Pascal and C source for this program is available on the distribution disk, and can be used as an example for writing a custom version of download software. The C source can also be compiled under Linux. SC5I20 is invoked with the FPGA configuration file and the 5I20 configuration base address on the command line:

```
SC5I20 FPGAFILE.BIN
```

SC9030W

Another utility SC9030W is provided for Windows 2000 and Windows XP This utility requires the PLX9030.SYS driver and PLXAPI.DLL API SHIM to work. The source for SC9030W can be used as an example of how to access the configured 5I20 cards under Windows 2K or XP.

SC5I20 and SC9030W use binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The utilities send PROM files directly to the 5I20. BIT files have their headers stripped and are bit reversed before being sent to the 5I20.

CLOCK SIGNALS

The 4 FPGA clock signals on the 5I20 are routed to 4 separate clock sources. GCLK0 connects IO0, GCLK1 connects to IO48, GCLK2 connects to the local bus clock which is the sameas the PCI clock, normally 33 MHz, and GCLK3 connects to a 50 MHz crystal oscillator on the 5I20 card.

LEDS

The 5I20 has 8 FPGA driven user LEDs, and 3 status LEDs. The user LEDs can be used for any purpose, and can be helpful as a simple debugging feature. A low output signal from the FPGA lights the LED. See the 5I20IO.PIN file for FPGA pin locations of the LED signals. The status LEDs reflect the state of the FPGA's DONE, /INIT, and the PCI bridge's GPIO5 bit.

PULLUP RESISTORS

All I/O pins are provided with pullup resistors to allow connection to open drain, open collector, or OPTO devices. These resistors are 10 pin, 9 resistor SIP networks. The resistor networks are socketed to allow the user to select different values. Pin 10 of all the resistor networks is grounded, allowing the use of 220/330 Ohm termination networks if desired on the receiving end of a high speed bus.

IO LEVELS

The Xilinx FPGAs used on the 5I20 have programmable I/O levels for interfacing with different logic families. The 5I20 does not support use of the I/O standards that require input reference voltages, so only 5 I/O options can be used. The available I/O options are LVTTL (5V tolerant), PCI33_5 (5V tolerant), PCI33_3, PCI66_3, and LVCMOS2. Two of the I/O options allow 5V inputs. I/O levels of the users I/O pins do not have to be +5V compatible if not needed, but it is suggested to use one of the 5V tolerant I/O standards to avoid possible damage if larger than 3.3V signals are applied to I/O pins.

Note that even though the 5I20s FPGA can tolerate 5V signal inputs, its outputs will not swing to 5V. The outputs are push pull CMOS that will drive to the output supply rail of 3.3V. This is sufficient for TTL compatibility but may cause problems with some types of loads. For example when driving an LED that has its anode connected to 5V, in such devices as OPTO isolators and I/O module rack SSRs, the 3.3V high level may not completely turn the LED off. To avoid this problem, either drive loads that are ground referred, Use 3.3V as the VCC for VCC referred loads, or tristate the output signals when no drive is desired (open drain).

STARTUP I/O VOLTAGE

After power-up or system reset and before the FPGA is configured, the pull-up resistors will pull all I/O signals to a high level. If the FPGA is used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state results in a safe condition.

SUPPLIED CONFIGURATIONS

IOPR12

The IOPR12 configuration creates a simple 72 bit parallel I/O port. IOPR12 is a word device, all accesses read or write 16 bit words. IOPR12 creates six 12 bit ports, 2 ports per I/O connector. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the IOPR12 configuration, see the regmap file in the /configs/IOPR12 directory of the 5I20 distribution disk.

IOPR24

The IOPR24 configuration creates a simple 72 bit parallel I/O port. IOPR24 is 32 bit device, all accesses read or write 16 bit words. IOPR24 creates three 24 bit ports, one port per I/O connector.. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the IOPR24 configuration, see the regmap file in the /configs/IOPR24 directory of the 5I20 distribution disk.

5I20LOOP

The IOPR24 configuration provides a simple way to check that all the I/O pins are OK and that most of the host interface is working. A loopback program (5I20LOOP) is provided for doing this testing. 5I20LOOP depends on an external loopback cable between I/O connectors P2, P3, and P4. 5I20LOOP perform a rotating bit test with one I/O connector programmed as outputs and the other two as inputs. All combinations of inputs and outputs are tested. In addition, a 32 bit register readback test is performed to verify 32 bit local data bus functionality.

HOSTMOT

The HOSTMOT2 configuration is a up to 12 channel host based servo motor or step motor controller. Host based controllers depend on the host CPU to "close" the servo loop. This has advantages and disadvantages. One advantage is that less hardware is needed, since host based software does all the math and handles all the control bits. Another advantage is that since the host based software is easily examined and modified, it is more amenable to customization and is more useful as a teaching tool. One disadvantage is that host based motor controllers depend on fast interrupt response time, since the control loop is an interrupt driven background task. This means that host based motor controllers don't tend to work well with multitasking operating systems such as Windows or Unix. They will work with real-time operating systems or simple operating systems like DOS.

SUPPLIED CONFIGURATIONS

HOSTMOT2

HOSTMOT2 is available in several configurations the vary the number of servo or step generator channels, plus miscellaneous I/O options including 32 bit buffered UARTs, SPI interfaces, SSI interfaces etc.

Demonstration software provided with the 5I20 implements a PID + feedforward control loop, plus a ramp-up, slew, ramp-down, profile generator for position control applications. Demo program (newmove.exe) and sources are located in the /configs/hostmot2/support directory of the 5I20 distribution disk..

SUPPLIED CONFIGURATIONS

*SOFT*DMC

The *Soft*DMC configuration creates a 4 or 8 axis processor based servo motor controller, with the processor embedded in the FPGA. The *Soft*DMC configuration has the advantage that the embedded processor takes care of all time critical functions, so it can control motor position and motions without host intervention.

The *Soft*DMC configuration has programmable sample and PWM rates, and can operate 4 axis at up to 30 KHz sample rate and 8 axis at up to 15 KHz sample rate.

The control loop is a PID+F loop (F=feedforward) with 16 bit tuning parameters. Position and Velocity use 32 bit parameters for wide range.

The profile generator supports position,velocity, and homing modes. Position mode includes ramp-up, slew, ramp-down motions. Velocity mode supports breakpoints and a linked list parameter loading system for accurate profiling. Profile generator uses 48 bit accumulator to allow velocities down to ~2 turns per day (500 line - 2000 count encoder, 4 KHz sample rate)

There is a separate manual available for the *Soft*DMC motion controller.

Demo program softdemo.exe), and tuning program (newdmc.exe) and sources are located in the /configs/softdmc/support directory of the 5I20 distribution disk.

REFERENCE

SPECIFICATIONS

POWER	**MIN**	**MAX**	**NOTES**:
POWER SUPPLY	4.5V	5.5V	
POWER CONSUMPTION:	----	1000 mA	Depends on FPGA Configuration
MAX 5V CURRENT TO I/O CONNS	---	500 mA	Total of all three
MAX 3.3V CURRENT TO I/O CONNS	---	500 mA	Total of all three
TEMPERATURE RANGE -C version	0 ºC	+70 ºC	
TEMPERATURE RANGE -I version	-40 ºC	+85 ºC	