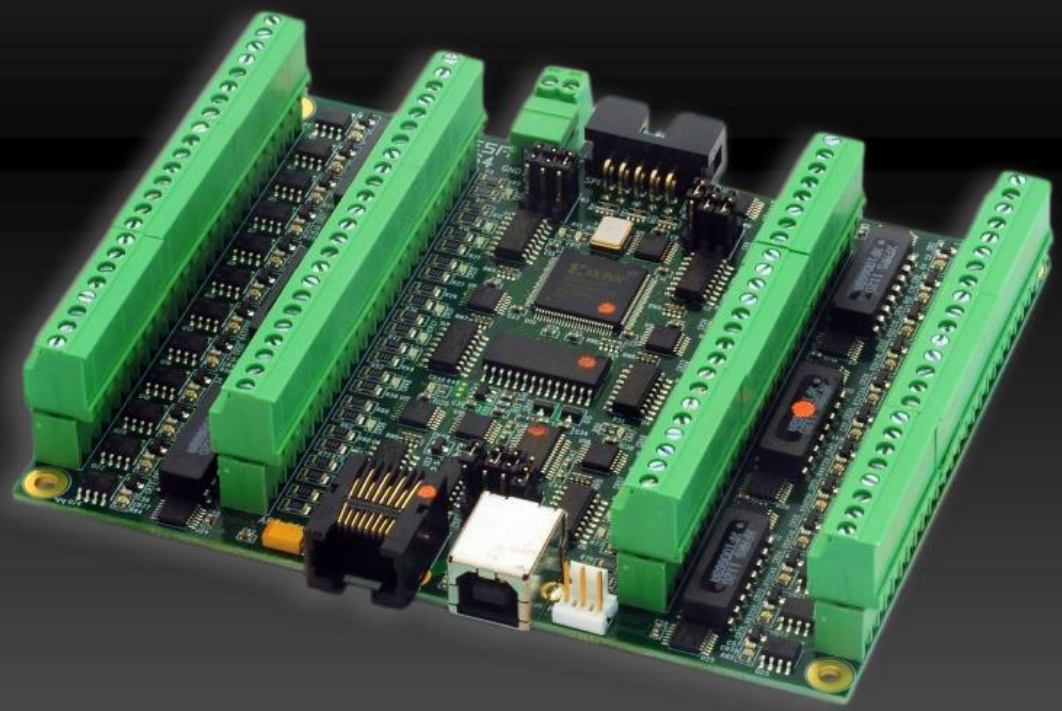
CNCPROM

Інтернет–магазин комплектуючих для верстатів з ЧПУ

MESA 7I64



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GENERAL

DESCRIPTION

The 7I64 is an 24 output, 24 input isolated I/O card. The 7I64 provides 24 isolated 48VDC 2.5A output drivers. All output drivers are low saturation voltage MOSFETS for low power dissipation. Each of the 24 output switches is isolated from the others, allowing high side, low side, push-pull and other output switch configurations. A built in watchdog timer turns all outputs off if the 7I64 is not accessed with in a selectable watchdog timeout interval.

The 24 OPTO isolated inputs will operate with input voltages from 5 to 24 V. Reverse protection diodes are provided to allow use with AC inputs.

The 7I64 has three host interface methods, USB, Serial RS-422 and SPI. The 7I64 can be USB powered. The serial interface supports baud rates from 115.2 K baud to 2.5 M baud. The SPI interface is compatible with MESAs Anything I/O cards and support high speed real time I/O. A SPI breakout card (7I46) allows up to six 7I64s to connect to a single 50 pin Anything I/O connector. The SPI interface supports data rates to 8 Mbps so a full read/write of all 48 I/O bits takes approximately 4 uSec. 3.5 mm pluggable screw terminals are used for all isolated I/O.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I64 card is oriented in an upright position, that is, with the 10 pin SPI connector is on top and the USB and RJ-45 serial connectors on the bottom.

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1,W3	SERIAL BAUD RATE SELECT	UP,UP,UP = USB
W4,W5	WATCHDOG TIMEOUT	UP,DOWN = 210 MS
W6	SPI MODE SELECT	DOWN = NO SPI
W7,W8	RS-422 TERMINATION	UP,UP = TERMINATED
W9	USB POWER SOURCE	UP = USB CABLE POWER
W10	USB POWER ENABLE	DOWN = ENUMERATE NEEDED FOR USB POWER UP.

BAUD RATE SELECTION

The 7I64 has 7 jumper selectable baud rates on its RS-422/RS-485 serial interface. Jumpers W1 through W3 select the serial port baud rate. In addition the baud rate jumpers can select the USB interface. The following table show the selectable baud rates:

W1	W2	W3	BAUD RATE
DOWN	DOWN	DOWN	115.2 KBAUD
DOWN	DOWN	UP	230.4 KBAUD
DOWN	UP	DOWN	460.8 KBAUD
DOWN	UP	UP	921 KBAUD

HARDWARE CONFIGURATION

BAUD RATE SELECTION

W1	W2	W3	BAUD RATE	NOTE
UP	DOWN	DOWN	1.25 MBAUD	
UP	DOWN	UP	2.5 MBAUD	FOR SSERIAL
UP	UP	DOWN	5.0 MBAUD	
UP	UP	UP	USB INTERFACE SELECTED	

Note: for operation with HOSTMOT2 SSERIAL/SSLBP interfaces, the baud rate must be set for 2.5 M Baud.

WATCHDOG TIMEOUT SELECTION

The 7I64 incorporates a watchdog circuit to disable all 24 outputs when the host interface has not updated the output register for a selectable period of time. The timeout period is selectable via jumpers W5 and W6.

W4	W5	TIMEOUT
DOWN	DOWN	13 MS
DOWN	UP	52 MS
UP	DOWN	210 MS
UP	UP	WATCHDOG DISABLED

SPI MODE SELECTION

The 7I64 can use Serial, USB, or SPI interface to the host. If the SPI interface is used, W6 must be in the"'UP" position. When serial or USB interfaces are used, W6 must be in the "DOWN" position. Note that when the SPI interface is used (W6 up), the USB and serial interfaces are not active, and when the serial or USB interfaces are used (W6 down), the SPI interface is not active.

RS-422/RS-485 TERMINATION

The RS-422/RS-485 serial interface can be terminated at the 7I64 card. Termination should be enabled if the 7I64 is the only card on a RS-422/RS-485 link, or if it is end card of a multi-drop RS-485 connected system. Termination is enabled when W7 and W8 are in the "UP" position, and disabled when W7 and W8 are in the "DOWN" positiion.

HARDWARE CONFIGURATION

USB POWER SOURCE

The 7I64 can gets it operating power via a USB cable or from the AUX 5V connector. Jumper W9 selects USB cable power when "UP". This is the suggested mode for USB operation of the 7I64.

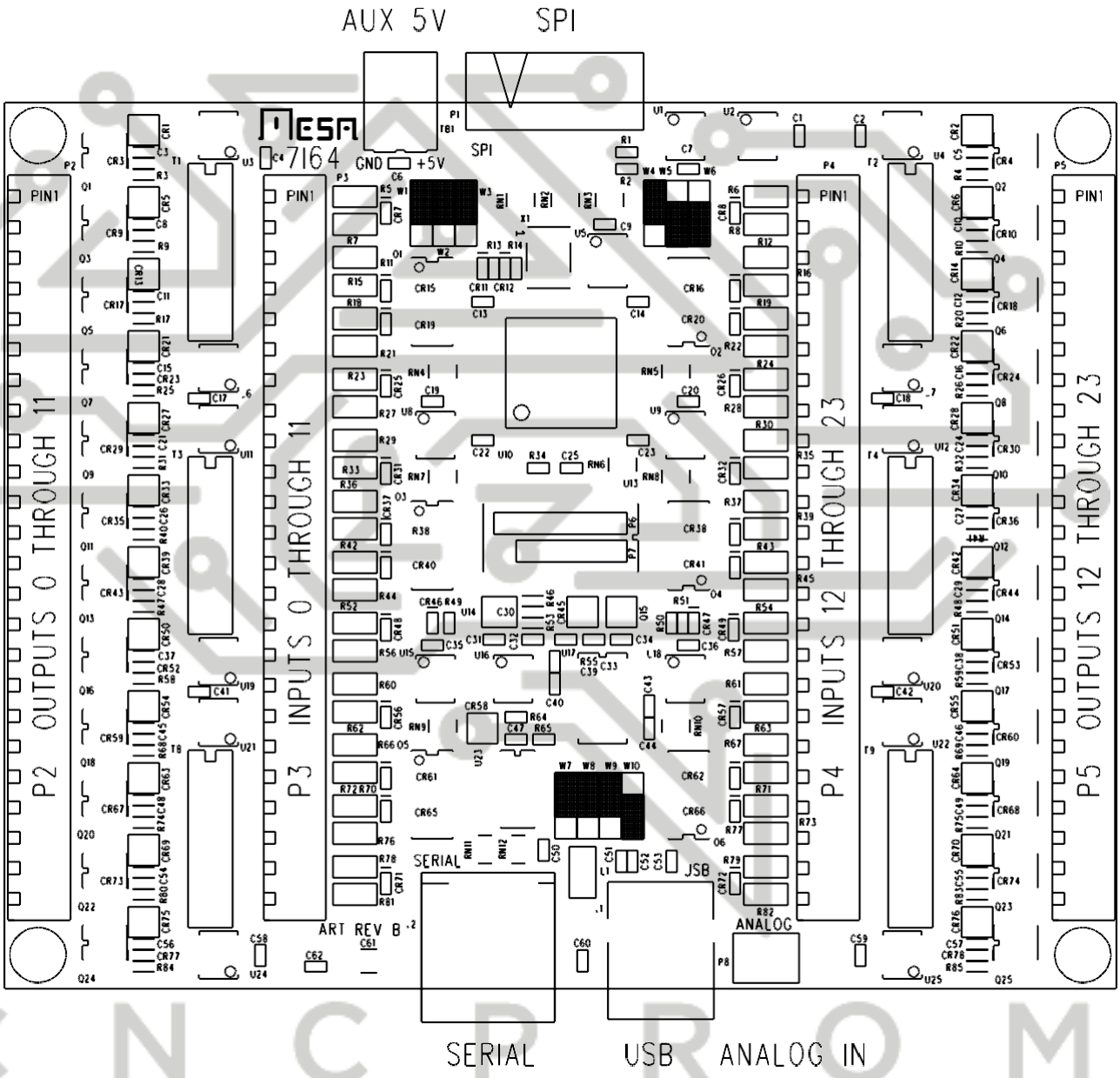
WARNING: ***Connecting an external 5V supply to the AUX power connectir of the 7I64 while W9 is in the "UP" position and a USB cable connects the 7I64 to a host computer is likely to damage the computer by feeding external power 'backwards' into the USB port!***

USB POWER ENABLE

A USB powered 7I64 can be set to power-up only after the USB interface is activated. This is the suggested operational mode when the 7I64 is interfaced via USB. W10 controls the USB power enable mode. When W10 is in the "UP" position, the 7I64 USB power source is always enabled. When W10 is in the "DOWN" position, the 7I64 USB power source will only be enabled when the USB interface is active, that is after the OS enumerates the USB device.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

SPI CONNECTOR

10 pin header connector P1 is the SPI interface connector. P1 can also supply power to the 7I64 as long as the cable length is less than 5 feet. The 7I46 breakout card allows up to six 7I64s to connect to a single "Anything I/O" connector.

PIN	FUNCTION	DIRECTION
1	+5V	TO 7I64
2	GND	TO 7I64
3	/FRAME	TO 7I64
4	GND	TO 7I64
5	SDI	TO 7I64
6	GND	TO 7I64
7	SCLK	TO 7I64
8	GND	TO 7I64
9	SDO	FROM 7I64
10	+5V	TO 7I64

AUX 5V POWER

Two pin 3.5 mm connector TB1 is normally used to supply 5V power to the 7I64 when not powered via the USB, Serial, or SPI connectors. TB1has the following pinout:

PIN	FUNCTION
1	5V (SQUARE PAD)
2	GND

ANALOG IN

The 7I64 provides two 0 to 3.3V analog inputs when used in the serial or USB interfaced modes. Analog input connector is three pin header P8. P8 pinout is as follows:

PIN	FUNCTION
1	ANALOG IN 0
2	ANALOG IN 1
3	GND

CONNECTORS

SERIAL CONNECTOR

The 7I64 uses a RJ-45 (J2) connector for its RS-422/RS-485 serial interface. Normal Ethernet type CAT5 cables should be used for the serial interface. The serial interface cable can also supply power to the 7I64 as long as the cable length does not exceed 5 feet. MESAs 7I44 breakout card can be used to interface a single 50 pin "Anything I/O" connector to up to eight RJ-45 connected RS-422/RS-485 serial interfaces. J2 pinout is as follows:

PIN	FUNCTION	DIRECTION
1	RX-	TO 7I64
2	RX+-	TO 7I64
3	TX-	FROM 7I64
4	GND	TO 7I64
5	GND	TO 7I64
6	TX+	FROM 7I64
7	+5V	TO 7I64
8	+5V	TO 7I64

CONNECTORS

TERMINAL BLOCK I/O CONNECTORS

The 7I64 isolated I/O connectors are pluggable (2 piece) 3.5 mm screw terminal blocks. Pin one is at the top of the 7I64 card.

OUTPUTS 0 THROUGH 11

P2 is the output connector for outputs 0 through 11. P2 pinout is as follows:

P2 PIN	FUNCTION	DIR	P2 PIN	FUNCTION	DIR
1	OBIT0+	FROM 7I64	2	OBIT0-	FROM 7I64
3	OBIT1+	FROM 7I64	4	OBIT1-	FROM 7I64
5	OBIT2+	FROM 7I64	6	OBIT2-	FROM 7I64
7	OBIT3+	FROM 7I64	8	OBIT3-	FROM 7I64
9	OBIT4+	FROM 7I64	10	OBIT4-	FROM 7I64
11	OBIT5+	FROM 7I64	12	OBIT5-	FROM 7I64
13	OBIT6+	FROM 7I64	14	OBIT6-	FROM 7I64
15	OBIT7+	FROM 7I64	16	OBIT7-	FROM 7I64
17	OBIT8+	FROM 7I64	18	OBIT8-	FROM 7I64
19	OBIT9+	FROM 7I64	20	OBIT9-	FROM 7I64
21	OBIT10+	FROM 7I64	22	OBIT10-	FROM 7I64
23	OBIT11+	FROM 7I64	24	OBIT11-	FROM 7I64

CONNECTORS

OUTPUTS 12 THROUGH 23

P5 is the output connector for outputs 12 through 23. P5 pinout is as follows:

P5 PIN	FUNCTION	DIR	P5 PIN	FUNCTION	DIR
1	OBIT12+	FROM 7I64	2	OBIT12-	FROM 7I64
3	OBIT13+	FROM 7I64	4	OBIT13-	FROM 7I64
5	OBIT14+	FROM 7I64	6	OBIT14-	FROM 7I64
7	OBIT15+	FROM 7I64	8	OBIT15-	FROM 7I64
9	OBIT16+	FROM 7I64	10	OBIT16-	FROM 7I64
11	OBIT17+	FROM 7I64	12	OBIT17-	FROM 7I64
13	OBIT18+	FROM 7I64	14	OBIT18-	FROM 7I64
15	OBIT19+	FROM 7I64	16	OBIT19-	FROM 7I64
17	OBIT20+	FROM 7I64	18	OBIT20-	FROM 7I64
19	OBIT21+	FROM 7I64	20	OBIT21-	FROM 7I64
21	OBIT22+	FROM 7I64	22	OBIT22-	FROM 7I64
23	OBIT23+	FROM 7I64	24	OBIT23-	FROM 7I64

INPUTS 0 THROUGH 11

P3 is the input connector for isolated inputs 0 through 11. P3 pinout is as follows:

P3 PIN	FUNCTION	DIR	P3	FUNCTION	DIR
1	IBIT0+	FROM 7I64	2	IBIT0-	FROM 7I64
3	IBIT1+	FROM 7I64	4	IBIT1-	FROM 7I64
5	IBIT2+	FROM 7I64	6	IBIT2-	FROM 7I64
7	IBIT3+	FROM 7I64	8	IBIT3-	FROM 7I64
9	IBIT4+	FROM 7I64	10	IBIT4-	FROM 7I64
11	IBIT5+	FROM 7I64	12	IBIT5-	FROM 7I64
13	IBIT6+	FROM 7I64	14	IBIT6-	FROM 7I64
15	IBIT7+	FROM 7I64	16	IBIT7-	FROM 7I64
17	IBIT8+	FROM 7I64	18	IBIT8-	FROM 7I64
19	IBIT9+	FROM 7I64	20	IBIT9-	FROM 7I64
21	IBIT10+	FROM 7I64	22	IBIT10-	FROM 7I64
23	IBIT11+	FROM 7I64	24	IBIT11-	FROM 7I64

INPUTS 12 THROUGH 23

P4 is the input connector for isolated inputs 12 through 23. P4 pinout is as follows:

P4 PIN	FUNCTION	DIR	P4 PIN	FUNCTION	DIR
1	IBIT12+	TO 7I64	2	IBIT12-	TO 7I64
3	IBIT13+	TO 7I64	4	IBIT13-	TO 7I64
5	IBIT14+	TO 7I64	6	IBIT14-	TO 7I64
7	IBIT15+	TO 7I64	8	IBIT15-	TO 7I64
9	IBIT16+	TO 7I64	10	IBIT16-	TO 7I64
11	IBIT17+	TO 7I64	12	IBIT17-	TO 7I64
13	IBIT18+	TO 7I64	14	IBIT18-	TO 7I64
15	IBIT19+	TO 7I64	16	IBIT19-	TO 7I64
17	IBIT20+	TO 7I64	18	IBIT20-	TO 7I64
19	IBIT21+	TO 7I64	20	IBIT21-	TO 7I64
21	IBIT22+	TO 7I64	22	IBIT22-	TO 7I64
23	IBIT23+	TO 7I64	24	IBIT23-	TO 7I64

OPERATION

SPI INTERFACE

The 7I64 can be interfaced via SPI. This is especially useful where real time operation is desired. When the SPI interface is used, the on card processor is bypassed, and the USB, serial, and analog interfaces are non-functional. SPI data format is MSB first, 32 data bits:

SPI DATA BITS 31 .. 24

COM3	COM2	COM1	COM0	WHB	XX	XX	XX

SPI DATA BITS 23 .. 16

I/O23	I/O22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16

SPI DATA BITS 15 .. 8

I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8

SPI DATA BITS 7 .. 0

I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0

The most significant bits of the SPI data, bits 28,29,30, and 31 are the command bits. The command bits determine if the SPI operation is a read or write. A command of 0xA is a write and a command of 0xB is a read. Other commands are invalid and will clear any outputs and set the watchdog has bitten flag. Bit 27 is the Watchdog_Has_Bitten flag (WHB). On a read command, a one in this bit indicates that the 7I64s watchdog has bitten. On a write if this bit is a one, the watchdog has bitten flag will be cleared. A write command always echos the input data, so a single SPI cycle can be used to both update the outputs and read the inputs.

Note that a write command will fail if the WatchDog_Has_Bitten flag is set. This means that initialization and error recovery code must first clear the WHB bit before writing data to the 7I64. It is suggested that normal write code not clear the WHB flag as a watchdog timeout could be missed if this is done.

OPERATION

SPI SETTINGS

The SPI interface will support SPI clock rate up to 8.33 Mhz. This assumes a 5 foot maximum controller cable length. For use with Mesa HostMot2 configuration SPI interfaces (SSPI or BSPI), channel setup is as follows:

CPOL	= 1
CPHA	= 0
BITS PER FRAME	= 0x1F (For 32 bits)
SPI BIT RATE	= 1 for 33MHz ClockLow FPGAs
	= 2 for ~50 MHz ClockLow FPGAs.
	This results in a ~ 8MHZ SPI clock

USB INTERFACE

The 7I64s USB interface uses a FTDI FT245R USB interface chip. Drivers for this chip make the 7I64 appear as a standard serial port. All 7I64 communication is done via the LBP protocol when the USB interface is used. Note that even though the 7I64 appears as a serial port when the USB interface is used, the driver baud rate parameter is unused and has no effect on communication rate.

Because USB is polled and a shared interface, it is normally not suitable for hard real-time applications. The serial (good at high baud rates) or SPI (better) interfaces are more suited to hard real time applications.

SERIAL INTERFACE

The 7I64s serial interface is a RS-422 or RS-485 link that supports baud rates from 115.2 KBaud to 5M Baud. All 7I64 communication is done via the LBP protocol when the serial interface is used. The serial interface should be terminated (jumpers W7 and W8 in up position) when used in RS-422 mode, and when used in RS-485 mode and the 7I64 is the last physical device and a shared interface cable.

The baud rate selection jumpers are only read at power up, so if the baud rate is changed, the 7I64 must be power cycled before the new baud rate will be used.

Serial data format is 8 bits, no parity.

OPERATION

LBP PROTOCOL

GENERAL

When the serial or USB interface are used, a byte oriented protocol is used to allow register access over the USB or serial link. This protocol is called LBP. LBP is a simple master slave protocol where the host sends read, write, or RPC commands to the 7I64, and the 7I64 responds. LBP commands always start with a command header byte. This header specifies whether the command is a read or a write, the number of address bytes(0, or 2), and the number of data bytes(1 through 8).The 0 address size option indicates that the current address pointer should be used. This address pointer will be post incremented by the data size if the auto increment bit is set. RPC commands allow any of up to 64 stored commands to be executed in response to the single byte command.

LBP DATA READ/WRITE COMMAND

0	1	WR	RID	AI	AS	DS1	DS0

Bit 7.. 6 **CommandType:** Must be 01b to specify data read/write command

Bit 5 **Write:** 1 to specify write, 0 to specify read

Bit 4 **RPCIncludesData:** 0 specifies that data is from stream, 1, that data is from RPC (RPC only, ignored for non RPC commands)

Bit 3 **AutoInc:** 0 leaves address unchanged, 1 specifies that address is post incremented by data size in bytes.

BIT 2 **AddressSize:** 0 to specify current address, 1 to specify 2 byte address.

Bit 1..0 **DataSize:** Specifies data size, 00b = 1 bytes, 01b = 2 bytes, 10 b= 4 bytes, 011b = 8 bytes.

When multiple bytes are specified in a read or write command, the bytes are always written to or read from successive addresses. That is, a 4 byte read at location 0x21 will read locations 0x21, 0x22, 0x23, 0x24. The address pointer is not modified after the command unless the AutoInc bit is set.

OPERATION

LBP PROTOCOL

WRITE EXAMPLE

Write 4 bytes (0xAA,0xBB,0xCC,0x00) to addresses 0x0000, 0x0001, 0x0002, 0x0003 (Isolated output port) with AutoInc so that the address pointer will be set to 0x0004 when the command is completed:

COMMAND BITS	CT1	CT0	WR	RID	AI	AS	DS1	DS0
LBPWrite: 2 add 4 data	0	1	1	0	1	1	1	0
Write Address LSB	0	0	0	0	0	0	0	0
Write Address MSB	0	0	0	0	0	0	0	0
Write data 0	1	0	1	0	1	0	1	0
Write Data 1	1	0	1	1	1	0	1	1
Write Data 2	1	1	0	0	1	1	0	0
Write Data 3	0	0	0	0	0	0	0	0

READ EXAMPLE

Next, Read 4 bytes at 0x0004,0x0005,0x0006,0x0007(Isolated input port):

COMMAND BITS	CT1	CT0	WR	RID	AI	AS	DS1	DS0
LBPRead: 0 add 4 data	0	1	0	0	0	0	1	0

Note that this read command uses the "0" address format as it relies on the address pointer being left a 4 by the preceding write instruction. Since no AutoInc was specified in the read command, the address pointer will be left at 0x0004 after the read command.

OPERATION

LBP PROTOCOL

LOCAL LBP COMMANDS

In addition to the basic data access commands there are a set of commands that access LBP status and control the operation of LBP itself. These are organized as READ and WRITE commands

LOCAL LBP READ COMMANDS

(HEX), all of these commands return a single byte of data.

0xC0 Get unit address (dont-care for USB devices)

0xC1 Get LBP status

LBP Status bit definitions:

BIT 7 Reserved

BIT 6 Command Timeout Error

BIT 5 Invalid write Error (attempted write to protected area)

BIT 4 Buffer overflow error

BIT 3 Watchdog timeout error

BIT 2 Reserved

BIT 1 Reserved

BIT 0 Reserved

0xC2 .. 0xC9 Reserved

0xCA Get Enable_RPCMEM access flag

0xCB Get Command timeout (in mS for USB and character times for serial)

0xCC .. 0xCF Reserved

0xD0 .. 0xD3 4 character card name

OPERATION

LBP PROTOCOL

LOCAL LBP READ COMMANDS

0xD5 .. 0xD7 4 character configuration name (only on some configurations)

0xD8 Get low address

0xD9 Get high address

0xDA Get LBP version

0xDB Get LBP Unit ID (Serial only, not used with USB)

0xDC Get RPC Pitch

0xDD Get RPC SizeL (Low byte of RPCSize)

0xDE Get RPC SizeH (High byte of RPCSize)

0xDF Get LBP cookie (returns 0x5A)

OPERATION

LBP PROTOCOL

LOCAL LBP WRITE COMMANDS

(HEX), all of these commands except 0xFF expect a single byte of data following the command.

0xE0 Reserved

0xE1 Set LBP status (0 to clear errors)

0xE2 .. 0xE9 Reserved

0xEA Set Enable_RPCMEM access flag (non zero to enable access to RPC memory)

0xEB Set Command timeout (in mS for USB and character times for serial)

0xEC .. 0xEF Reserved

0xF0 .. 0xF6 Reserved

0xF7 Write LEDs

0xF8 Set low address

0xF9 Set high address

0xFA Add byte to current address

0xFB .. 0xFC Reserved

0xFD Set unit ID (serial only)

0xFE Reset LBP processor if followed by 0x5A

0xFF Reset LBP parser (no data follows this command)

OPERATION

LBP PROTOCOL

RPC COMMANDS

RPC commands allow previously stored sequences of read/write commands to be executed with a single byte command. Up to 64 RPC's may be stored. RPC write commands may include data if desired, or the data may come from the USB or serial data stream. RPCs allow significant command compression which improves communication bandwidth.

LBP RPC COMMAND

1	0	RPC5	RPC4	RPC3	RPC2	RPC1	RPC0

Bit 7..6 **CommandType:** must be 10b to specify RPC

Bit 5..0 **RPCNumber:** Specifies RPC 0 through 63

In the 7I64 LBP implementation, RPCPitch is 0x08 bytes so each RPC command has native size of 0x08 bytes and start 0x08 byte boundaries in the RPC table area. RPCs can cross RPCPitch boundaries if larger than RPCPitch RPCs are needed. The stored RPC commands consist of LBP headers and addresses, and possibly data if the command header has the RID bit set. RPC command lists are terminated by a 0 byte.

The RPC table is accessed at addresses 0 through RPCSize-1 This means with a RPCPitch of 0x08 bytes, RPC0 starts at 0x0000, RPC1 starts at 0x0008, RPC2 starts at 0x0010 and so on.

Before RPC commands can be written to the RPC table,the RPCMEM access flag must be set. The RPCMEM access flag must be clear for normal operation.

OPERATION

LBP PROTOCOL

EXAMPLE RPC COMMAND LIST

This is an example stored RPC command list. Note RPC command lists must start at a RPCPitch boundary in the RPC table but an individual RPC list can extend until the end of the table. This particular RPC example contains 3 LBP commands and uses 10 bytes starting at 0x0028 (RPC5 for 0x08 pitch RPC table). Since 10 bytes is larger than the 7I64s 8 byte RPC pitch, RPC 6 would be unavailable.

Command1. Writes four data bytes to port 0x0000 with the four data bytes supplied by host (7I64 output port update)

Command2. Reads four data bytes from port 0x0004 (7I64 input port read)

Command3. Reads two data bytes from port 0x0010 (7I64 analog input read)

COMMAND BITS	CT1	CT0	WR	RID	I	AS	DS1	DS0
LBPWrite: 2 add 4 data	0	1	1	0	0	1	1	0
Write Address LSB	0	0	0	0	0	0	0	0
Write Address MSB	0	0	0	0	0	0	0	0
LBPRead: 2 add 4 data	0	1	0	0	0	1	1	0
Read Address LSB	0	0	0	0	0	1	0	0
Read Address MSB	0	0	0	0	0	0	0	0
LBPRead 2 add 2 data	0	1	0	0	0	1	0	1
Write Address LSB	0	0	0	1	0	0	0	0
Write Address MSB	0	0	0	0	0	0	0	0
Terminator	0	0	0	0	0	0	0	0

OPERATION

LBP PROTOCOL

EXAMPLE RPC COMMAND LIST

The outgoing data stream for this RPC would consist of these 5 bytes:

COMMAND BITS	CT1	CT0	R5	R4	R3	R2	R1	R0
RPC 5	1	0	0	0	0	1	0	1
Data 0 for Command 1	1	1	1	1	1	1	1	0
Data 1 for Command 1	1	1	0	0	1	0	1	0
Data 2 for Command 1	1	0	1	0	1	0	1	0
Data 3 for Command 1	0	1	0	1	0	1	0	1

The returned data would consist of the 4 bytes of Input port read data from command 2 followed by the2 bytes of analog data from command 3:

Data 0 from Command 2	1	1	1	1	1	1	1	0
Data 1 from Command 2	1	1	0	0	1	0	1	0
Data 2 from Command 2	1	1	0	0	1	1	1	0
Data 3 from Command 2	1	1	1	1	1	0	1	0
Data 0 from Command 3	1	0	1	0	1	1	0	1
Data 1 from Command 3	1	1	0	1	1	1	1	0

CRC

When using the serial interface, LBP on the 7I64 uses CRC checking of all commands and data to insure validity. The CRC used is a 8 bit CRC using the same polynomial as the Dallas/Maxim one wire devices (X^8+X^5++X^4+X^0). The CRC must be appended to all LBP commands and all returned data will have a CRC byte appended. Commands with no returned data (writes or RPCs with no reads) will still cause a CRC byte to be returned, this CRC byte will always be 00H. The USB interface does not use CRC by default because the USB packets have their own error checking system.

OPERATION

REGISTER MAP

When the 7I64 is used with USB or serial interfaces, the LBP protocol is used for register access. The 7I64s register map for LBP is very simple, having only seven 32 bit registers available. The registers are as follows:

REGISTER 0x0000: 32 BIT ISOLATED DATA-OUT

The data out register controls the 24 isolated outputs. A one bit in the data-out register turns the corresponding output switch on. Only the least significant 24 bits control outputs. Bit 27 (WHB) has a special function, when set it clears the watchdog-has-bitten status bit. Whenever the watchdog has bitten, this bit must be cleared to resume normal operation. Reads from the data-out register will return the last written data. Note that this register only supports 32 bit operations, accesses with other data sizes will result in undefined operation.

REGISTER 0x0004: 32 BIT ISOLATED DATA-IN

The data in register reads the 24 isolated inputs, A one bit in the data-in register indicates a "high" input signal. The least significant 24 bits of the data register correspond to the 7I64 inputs. In addition to reading the input status, the data-in register returns the watchdog_has_bitten status bit (WHB). This is returned in bit 27 of the data-in register. If bit 27 of the data register is high, this indicates that the output shutdown watchdog has "bitten". Writes to the data-in register are no-ops. Note that this register only supports 32 bit operations, accesses with other data sizes will result in undefined operation.

REGISTER 0x0008: 32 BIT SCRATCH

This register is just a scratch register for LBP testing, it has no I/O function.

REGISTER 0x0010: 16 BIT ANALOG IN 0

This register reads the most recent A-D conversion of channel 0. A-D data is 10 bits, left justified in a 16 bit data register.

REGISTER 0x0014: 16 BIT ANALOG IN 1

This register reads the most recent A-D conversion of channel 1. A-D data is 10 bits, left justified in a 16 bit data register.

REGISTER 0x0018: 16 BIT ANALOG IN 0

This register reads the running average of A-D conversions of channel 0. A-D data is 10 bits, left justified in a 16 bit data register.

REGISTER 0x001C: 16 BIT ANALOG IN 1

This register reads the running average of A-D conversions of channel 0. A-D data is 10 bits, left justified in a 16 bit data register.

OPERATION

LBPCOM

LBPCOM is a simple windows console mode communication program for testing and getting familiar with LBP on serial and USB connected LBP devices. LBPCOM accepts a string of hexadecimal bytes and sends them to the LBP device. It then waits for returned data and prints the result in hexadecimal. LBPCOM only sends and receives data bytes in the order types, it doesn't parse the sent or returned data, so the least significant byte first order of data sent or received may be confusing at first.

LBPCOM in invoked with the COM port on the command line:

LBPCON COM12

LBPCOM then prints a prompt:

<

To send a LBP command, type the hexadecimal command followed by any needed data or addresses:

< DF

> 5A

(request LBP cookie 0xDF always returns 0x5A)

< D0 D1 D2 D3

> 37 49 36 34

(Request card name)

< 66 00 00 55 55 55 08

>

(32 bit write of 08555555 to location 0 = isolated outputs with bit 27 set to clear WHB, this will turn on all of the even outputs:0,2,4,6,8 etc. Note the least significant byte first order)

> 46 04 00

> 01 00 00 00

(32 bit read of location 0x0004 = isolated input bits, only bit 0 is on)

OPERATION

WATCHDOG

As a safety feature, the 7I64 incorporates a watchdog circuit to disable the outputs (all outputs off) if the isolated outputs register has not been updated within a preset time interval. The outputs are also turned off in the following conditions:

1. Power UP

2. Invalid command in SPI command register (not 0xA or 0xB)

The watchdog has three timeout values selectable via on card jumpers, plus a watchdog disabled state. Timeout values are approximately 10 mS, 52 mS, and 210 mS. For normal control applications, a 10 or 52 mS timeout is suggested. ***The watchdog disable feature is for manual testing and should not be used for normal control applications.***

If the watchdog "bites", the watchdog_has_bitten (WHB) flag is set, and further updates to the output register are blocked until the WHB flag is cleared. It is recommended that host software only clear the WHB flag when it detects a watchdog timeout event. The reason for this is that if the WHB is cleared every output register update (by including a WHB = '1' bit in the output data), a watchdog timeout event might be missed.

OPERATION

ISOLATED INPUTS

The 7I64s 24 isolated inputs are standard OPTO isolators with 4.4K input resistors and reversed input protection diodes. The inputs will operate with DC I/O voltages from 4 to 24VDC. 48VDC inputs can be accommodated by adding a 4.7K external series resistor. Input protection diodes prevent damage from reversed inputs. The reverse input protection diodes are red LEDs. These diodes will illuminate if the inputs have the wrong polarity. Input switching speed is approximately 5 uSec on and 25 uSec off.

The OPTO isolators have a 2500V isolation rating but PCB clearances reduce the maximum isolation voltage to 500 VDC.

Note that 7I64 isolated inputs are not to be used for line voltage isolation applications!

ISOLATED OUTPUTS

The 7I64s 24 isolated outputs are transformer driven MOSFET switches. Each output switch is individually isolated, allowing high side drive, low side drive, and other configurations. The MOSFETS are rated 48VDC and 2.5A continuous load current. Switching times are approximately 1 uSec for turn on and 5 uSec for turn off. MOSFET on resistance is typically 30 mOhms, resulting in about 75 mV voltage drop at maximum current.

When used with inductive loads, the load should be clamped with a diode to prevent excessive MOSFET voltage, Small inductive loads with less than 50 mJoules of energy, (Stored inductive energy is ½ LI^2) can be used without a clamp diode, but his will result in high voltage spikes (~80V) that may interfere with other circuitry and higher MOSFET switching dissipation. This dissipation will limit switching rates of unclamped inductive loads.

AC loads can be driven by connecting isolated outputs in series. The outputs must be series connected in opposition, that is for example to use OBIT0 and OBIT1 in series you would connect OBIT0- to OBIT1- and use OBIT0+ and OBIT1+ as the switch leads. When AC loads are switched, both output register bits should be changed at once. When AC inductive loads are switched, A varistor across the load is suggested for inductive energy dissipation. Maximum switched AC supply voltage is 36V in this configuration.

Caution: The MOSFETS have inherent source-drain diodes, so a reverse connected output will drive the load when off and the MOSFET will likely be damaged by excessive power dissipation.

Note that 7I64 isolated outputs are not to be used for line voltage isolation applications!

OPERATION

ANALOG INPUTS

When used with USB or serial interface, two analog inputs are available. These inputs have a 0 to 3.3V unipolar input range and a resolution of 10 bits. The data presented to the interface is left justified so that the numeric range of analog data read via the serial or USB ports is 0 to 65472 (1023 * 64). Each channel has raw and averaged data available. The raw data is simply the raw 10 bit A-D data left shifted 6 places. Raw data is sampled at the 7I64 at a fixed 16 KHz rate. The averaged data is a running average of the A-D data. The averaged data has a bandwidth of ~10 Hz.

Analog inputs should not exceed the 0 to +3.3V input range. The analog inputs are protected against permanent damage for inputs from +12V to -12V but voltages in excess of 4V or less than -.7V may cause the processor to malfunction.

LEDS

The 7I64 has many on card LEDS for status and debugging information. These include LEDs for watchdog status, input polarity checking, output status monitoring an serial transmit enable monitoring

One LED pair, CR11 and CR12, near the center top of the card display the Watchdog_Has_Bitten status (WHB). CR11 is Red and CR12 is green. If the Watchdog has bitten, CR11, the red LED will be illuminated. If the WHB status is clear, CR12, the green LED will be illuminated. When the 7I64 is first powered up, only the red LED, CR11 should be illuminated.

Each output has a monitor LED. The LEDs are yellow and are mounted near the MOSFET output switch transistors.

Every isolated input has a reverse protection diode. The diodes are red LEDs so a input connected with reverse polarity will illuminate one of these LEDs.

CR47 is a Green LED on the lower right hand side of the card. It is illuminated when the serial interface is used and data is being transmitted.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	+4.5	+5.25	VDC
5V POWER CONSUMPTION	----	350	mA
ISOLATED OUTPUT SWITCH CURRENT	----	2.5	A
ISOLATED OUTPUT SWITCH VOLTAGE	----	48	VDC
ISOLATED OUTPUT ISOLATION VOLTAGE	----	500	VDC
ISOLATED INPUT SENSE VOLTAGE	4	24	VDC
ISOLATED INPUT ISOLATION VOLTAGE	----	500	VDC
ANALOG INPUT VOLTAGE ACCURACY	----	5	%
ANALOG INPUT RESOLUTION	----	10	BITS
ANALOG INPUT RANGE	0	3.3	VDC
OPERATING TEMP.	0	+70	ºC
OPERATING TEMP. (-I version)	-40	+85	ºC
OPERATION HUMIDITY	0	95%	NON-COND