Vitkovets CNC

Комплектуючі систем ЧПУ

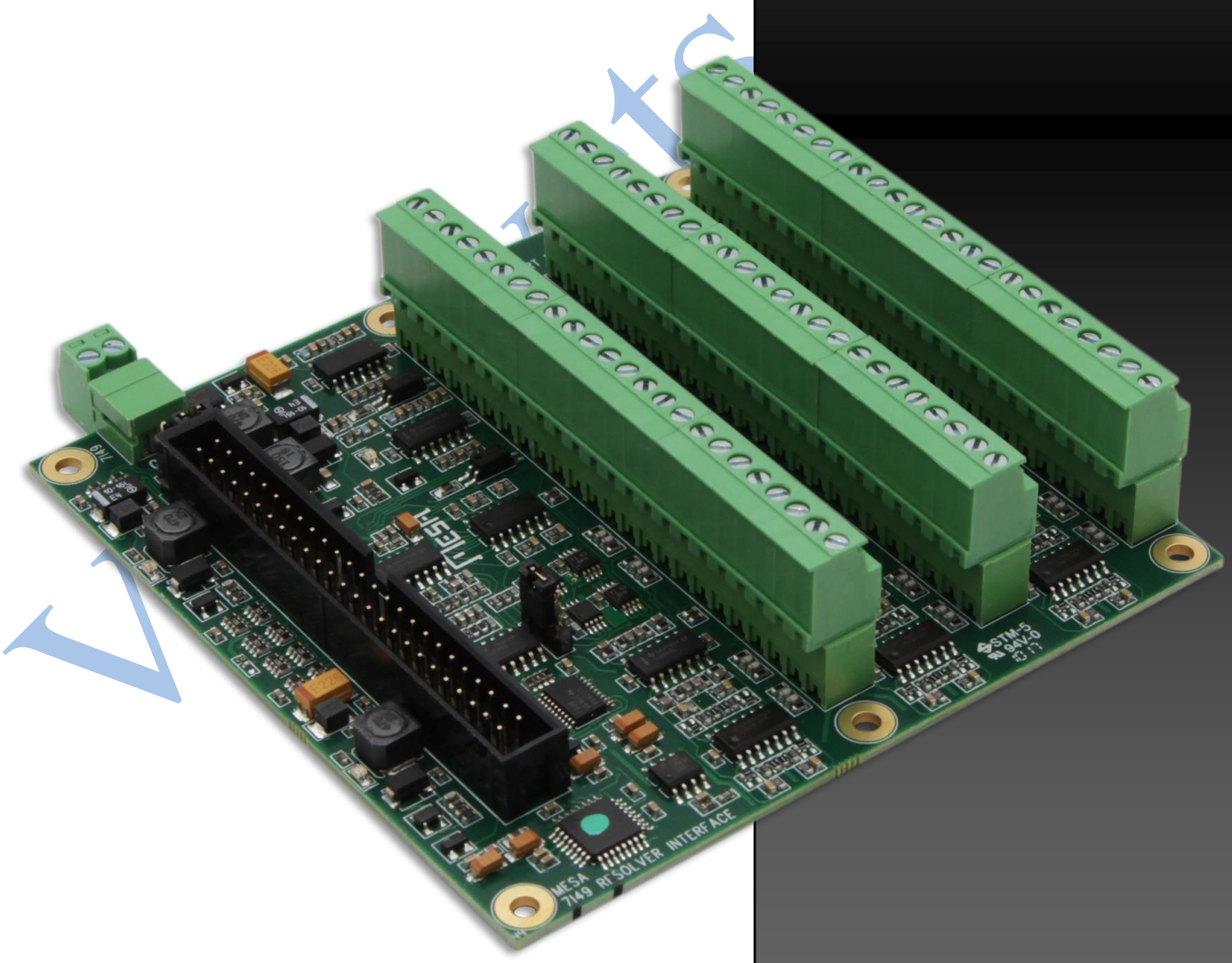
http://cnc.prom.ua/

+380 (096)-665-71-06
+380 (098)-821-25-90

cncprom@ukr.net

CNCPROM

Контролер MESA 7I49HV



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GENERAL

DESCRIPTION

The 7I49 is a daughtercard for Mesa's Anything I/O FPGA cards. The 7I49 provides a six channel resolver interface with six additional +-10V analog outputs. The 7I49 is intended for applications that read standalone resolvers, as the 7I49 generates the resolver reference carrier.

The 7I49 can be used with 1:1 and 1:2 transformation ratio resolvers. The 7I49 has approximately 14 bits of resolution and 12 bits of absolute accuracy. The 7I49 FPGA interface module allows velocity and absolute position readout from the host. The 7I49 has selectable carrier frequencies, from 2.5 KHz up to 10 KHz. Host position readout is updated at 256 times the resolver carrier frequency to reduce aliasing when host sampling is not synchronous with the carrier frequency.

Velocity resolution is approximately 1 RPM with default filter parameters. The 7I49 uses a oversampling A-D followed by a tracking filter. Filter coefficients may be changed to trade off noise versus acceleration tracking ability.

The controller connection is a 50 pin header that matches the pinout of the Mesa anything I/O series of cards. All resolver and analog I/O is via 3.5 MM pluggable screw terminal blocks. The 7I49 requires a single 5V power supply.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I49 card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side,

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1	CABLE POWER SELECT	RIGHT = CABLE POWER
W2	RESOLVER DRIVE SELECT	UP = CHAN 3,4,5 = FULL

CABLE POWER/P1 POWER SELECTION

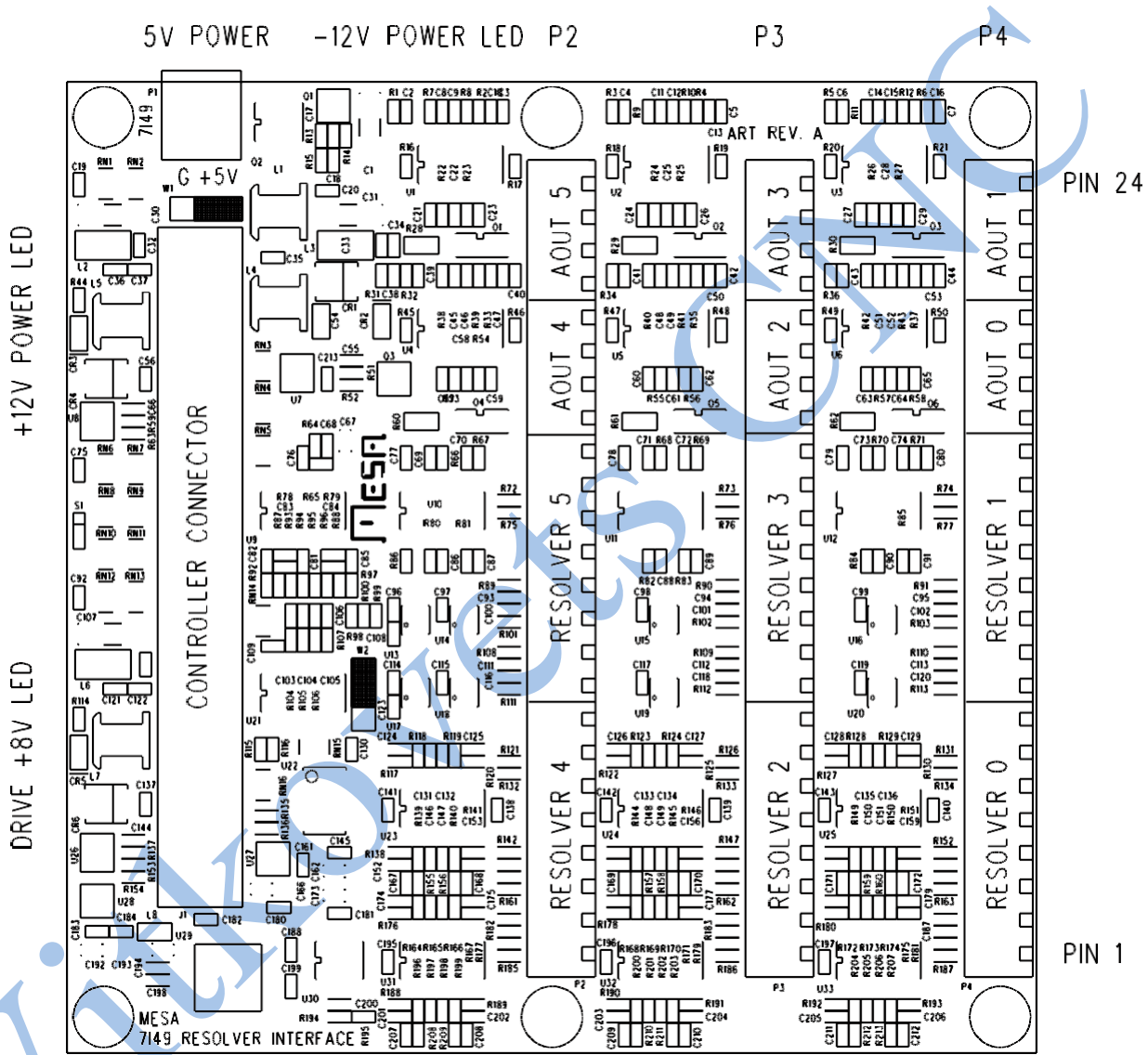
The 7I49 can get its operating power from the flat FPGA cable or from P1. For testing with only 1 or 2 resolvers, cable power can be used. W1 selects whether cable power connects to the 7I49s 5V supply. If W1 is in the "RIGHT" position, cable power is selected. If W1 is in the "LEFT" position, external 5V power must be supplied via P1.

RESOLVER DRIVE SELECT

The reference sine wave for all resolver channels on the 7I49 comes from a single PDM source in the FPGA. To accommodate resolvers with different transformation ratios, the 7I49 has the option to lower the reference drive voltage on channels 3,4 and 5. Default 7I49 firmware setup assumes a standard 2:1 reference:output ratio. To accommodate 1:1 resolvers on some channels the reference drive voltage on the last three channels can be set to ½ of full scale if desired. When W2 is in the up position, channels 3, 4, and 5 have standard reference signal levels. When W2 is in the down position, channels 3, 4, and 5 have ½ scale reference signal levels.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the anything I/O card/motion controller. This can be a male 50 pin header on the top of the 7I49 card or a female 50 conductor header on the bottom side of the 7I49 depending on 7I49 model. Controller connector pin-out is as follows:

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	/ENA0	TO 7I49	25	PWM-0	TO 7I49
3	NC	XX	27	PWM+1	TO 7I49
5	SPIDO0	FROM 7I49	29	PWM-1	TO 7I49
7	SPIDO1	FROM 7I49	31	PWM+2	TO 7I49
9	AMUX2	TO 7I49	33	PWM-2	TO 7I49
11	AMUX1	TO 7I49	35	PWM+3	TO 7I49
13	AMUX0	TO 7I49	37	PWM-3	TO 7I49
15	SPICLK	TO 7I49	39	PWM+4	TO 7I49
17	SPICS	TO 7I49	41	PWM-4	TO 7I49
19	REFPDM-	TO 7I49	43	PWM+5	TO 7I49
21	REFPDM+	TO 7I49	45	PWM-5	TO 7I49
23	PWM+0	TO 7I49	47	/ENA1	TO 7I49
			49	+5V PWR	TO 7I49

Note: all even pins are grounded.

AUX 5V POWER

The 7I49 can get its 5V power from the FPGA cable or connector P1. Normally P1 should be used for power as the 5V current draw from 6 resolvers will exceed what the FPGA flat cable can deliver. Note that the 7I49 will only connect to P1 power if the cable 5V is present.

PIN	FUNCTION
1	5V
2	GND

CONNECTORS

TERMINAL BLOCK SERVO AMP/RESOLVER CONNECTORS

The 7I49's servo amplifier / encoder connectors (P2,P3, and P4) are 3.5MM 24 pin headers compatible with Phoenix style screw terminal blocks (supplied). Connector P4 has the I/O signals for channels 0 and 1:

P4 PIN	FUNCTION	DIR
1	RESSIN0-	TO 7I49
2	RESSIN0+	TO 7I49
3	RESCOS0-	TO 7I49
4	RESCOS0+	TO 7I49
5	GND	FROM 7I49
6	RESDRV0-	FROM 7I49
7	RESDRV0+	FROM 7I49
8	GND	FROM 7I49
9	RESSIN1-	TO 7I49
10	RESSIN1+	TO 7I49
11	RESCOS1-	TO 7I49
12	RESCOS1+	TO 7I49
13	GND	FROM 7I49
14	RESDRV1-	FROM 7I49
15	RESDRV1+	FROM 7I49
16	GND	FROM 7I49
17	ENA0-	FROM 7I49
18	ENA0+	FROM 7I49
19	GND0	FROM 7I49
20	AOUT0	FROM 7I49
21	ENA1-	FROM 7I49
22	ENA1+	FROM 7I49
23	GND1	FROM 7I49
24	AOUT1	FROM 7I49

CONNECTORS

TERMINAL BLOCK SERVO AMP/ENCODER CONNECTORS

Connector P3 has the I/O signals for channels 2 and 3:

P3 PIN	FUNCTION	DIR
1	RESSIN2-	TO 7I49
2	RESSIN2+	TO 7I49
3	RESCOS2-	TO 7I49
4	RESCOS2+	TO 7I49
5	GND	FROM 7I49
6	RESDRV2-	FROM 7I49
7	RESDRV2+	FROM 7I49
8	GND	FROM 7I49
9	RESSIN3-	TO 7I49
10	RESSIN3+	TO 7I49
11	RESCOS3-	TO 7I49
12	RESCOS3+	TO 7I49
13	GND	FROM 7I49
14	RESDRV3-	FROM 7I49
15	RESDRV3+	FROM 7I49
16	GND	FROM 7I49
17	ENA2-	FROM 7I49
18	ENA2+	FROM 7I49
19	GND2	FROM 7I49
20	AOUT2	FROM 7I49
21	ENA3-	FROM 7I49
22	ENA3+	FROM 7I49
23	GND3	FROM 7I49
24	AOUT3	FROM 7I49

CONNECTORS

TERMINAL BLOCK SERVO AMP/ENCODER CONNECTORS

Connector P2 has the I/O signals for channels 4 and 5:

P2 PIN	FUNCTION	DIR
1	RESSIN4-	TO 7I49
2	RESSIN4+	TO 7I49
3	RESCOS4-	TO 7I49
4	RESCOS4+	TO 7I49
5	GND	FROM 7I49
6	RESDRV4-	FROM 7I49
7	RESDRV4+	FROM 7I49
8	GND	FROM 7I49
9	RESSIN5-	TO 7I49
10	RESSIN5+	TO 7I49
11	RESCOS5-	TO 7I49
12	RESCOS5+	TO 7I49
13	GND	FROM 7I49
14	RESDRV5-	FROM 7I49
15	RESDRV5+	FROM 7I49
16	GND	FROM 7I49
17	ENA4-	FROM 7I49
18	ENA4+	FROM 7I49
19	GND4	FROM 7I49
20	AOUT4	FROM 7I49
21	ENA5-	FROM 7I49
22	ENA5+	FROM 7I49
23	GND5	FROM 7I49
24	AOUT5	FROM 7I49

OPERATION

PWM RATE

The 7I49 is meant to operate with PWM rates from 24 KHz to 500 KHz. Operation at lower PWM rates will result in excessive output ripple, operation at higher PWM rates or with PDM with higher than 10 MHz base frequency will result in poor linearity. When used with HostMot2 firmware, the PWM generators should be set for UP/DOWN mode and the PWM frequency set for 24 KHz.

AOUT STEP RESPONSE

The 7I49 AOUT channels have a 5 pole PWM filter with an approximate 150 uSec time constant. This value is selected as a compromise between output ripple and settling time. This is much faster than most controlled devices and will not normally have any effect on loop stability or performance. The 7I49 can be assembled with different components if necessary to change this time constant.

RESOLVER DRIVE VOLTAGE

The 7I49 is intended to operate with common 2:1 transformation ratio resolvers. Default drive voltage is approximately 2V RMS which is suitable for most resolvers. The sine and cosine inputs expect an analog signal level of approximately 1V RMS, so a 2V RMS drive voltage will use the full A-D input range with 2:1 ratio resolvers. For other resolver ratios, the drive voltage can be lowered. If a mix of 2:1 and 1:1 resolvers must be supported, the 7I49 can supply ½ drive on channels 3, 4, and 5 (1V RMS), allowing 1:1 ratio resolvers to be connected to channels 3,4, and 5 and 2:1 ratio resolvers to be connected to channels 0, 1, and 2. Higher stepdown ratio resolvers can be used, but will result in low signal levels which will show up as increased position and velocity noise.

OPERATION

RESOLVER WIRING

Resolver signals are analog and susceptible to noise. The 7I49 has differential drive and sine/cos signaling to improve noise rejection. To take full advantage of the differential signaling, resolver wiring should always be done with individually shielded twisted pairs. One shielded pair is used for the drive signal (RESDRVx+ and RESDRVx-), one shielded pair for the sine signals (RESSINx+ and RESSINx-) and one shielded pair for the cosine signals (RESCOSx+ and RESCOSx-). Shields should be terminated only at the 7I49 end of the cable.

RESOLVER FIRMWARE

It is expected that the 7I49 with be operated with an "Anything I/O" card using the RESMOD firmware. The RESMOD firmware generates the reference sine wave for the resolvers, interfaces with the A-D chip on the 7I49 card, acquires oversampled sine and cosine data from this A-D synchronously with the reference sine wave and feeds the A-D data into a second order tracking filter that tracks the resolver position and velocity. The outputs of this filter are then presented to the host in 32 bit read only registers for velocity and position. The RESMOD firmware also allows access to internal parameters for fine tuning. The default settings should be fine for most 7I49 applications, but most parameters can be tuned suit different applications.

RESMOD REGISTERS

The RESMOD FPGA firmware communicates to the host via three global registers (COMMAND, DATA, and STATUS) and 12 per channel registers (POSITION and VELOCITY per channel). *Note: If RESMOD defaults are satisfactory, there is no need to access the command or data registers as these are only for changing operational parameters and resolver frequency.*

VELOCITY REGISTERS

There are six 32 bit velocity registers per RESMOD firmware module. Velocity scaling is resolver frequency dependent. Velocity scaling in RPM is:

Velocity register*Carrier frequency*60 / 2^32

POSITION REGISTERS

There are six position registers. Each register reads absolute position in turns/2^32. Scaling for degrees is:

Position register*360/2^32

Note that there are no multi-turn counters, so the position register must be sampled frequently enough to guarantee that no turns are lost.

COMMAND REGISTER

The command register is where parameter read and write commands and setup commands are written. Host handshaking is done by polling the command register. When the RESMOD firmware is busy, the command register will be non-zero. Only when the command register is zero should a command be written.

DATA REGISTER

The data register is where parameter data is written to and read from, as part of a parameter read/write sequence.

PARAMETER READ SEQUENCE

Parameter read sequence is as follows:

1. Write command register with parameter address

2. Wait for command register to be = 0

3. Read parameter from data register

PARAMETER WRITE SEQUENCE

Parameter write sequence is as fiollows:

1. Write data register with parameter data

2. Write command register with parameter address Ored with 0x00008000

3. Wait for command register to be = 0

RESOLVER STATUS

The status register of the RESMOD interface reports resolver status. Bits 0 though 5 in the status register indicate status of resolver channels 0 though 5. A 1 bit indicates an error in the corresponding channel and that the position and velocity of that channel are invalid.

RESOLVER FREQUENCY

The current RESMOD firmware can operate with 3 selectable resolver frequencies, ~2.5 KHz, ~5 KHz and ~10 KHz. Resolver frequency is selectable for the 7I49 card, not per channel, so if a mix of resolvers is used, a frequency that is acceptable to all resolvers must be chosen. The default frequency is ~10 KHz. Lower rates will result in lower noise, but more lag between physical motion and the readout position. Actual resolver frequency depends on the FPGA reference clock (CLOCKLOW) with the following relationship:

~10 KHz CLOCKLOW/5000

~5 KHz CLOCKLOW/10000

~2.5 KHz CLOCKLOW/20000

SETTING RESOLVER FREQUENCY

The default resolver carrier frequency is ~10 KHz. Writing a 0x801, 0x802, or 0x803 command to RESMOD's command register will set the resolver frequency to ~2.5 KHz, ~5 KHz and ~10 KHz respectively.

RESOLVER TRACKING RATE

The second order tracking filter will track velocities up to ½ turn per sample. This is 75,000 RPM at 2.5 KHz, 150,000 RPM at 5 KHz and 300,000 RPM at 10 KHz. Note that "speed voltage" and other effects will limit accuracy at very high speeds, so suggested maximum speeds are 1/10 of the tracking maximums, that is 7,500 RPM at 2.5 KHz, 15,000 RPM at 5 KHz and 30,000 RPM at 10 KHz.

The second order filter will "lock" onto constant velocities with essentially zero error other than noise, but will lag the resolver rotor position when the resolver is accelerating. The amount of lag depends on the tracking filter tuning and resolver frequency. The tracking filter tuning allows a compromise between position and velocity noise and the ability of the tracking filter to follow rapid acceleration with minimum error. With the RESMOD tuning defaults and 10 KHz resolver frequency, the position lag is less than 1/4 degree with a 30,000 RPM/sec acceleration.

In addition to the position delay under acceleration, there is a fixed delay of 1/(resolver carrier frequency) + ~25 uSec in the position output. This is due to the synchronous sampling of the carrier frequency plus a fixed processing time (the ~25 uSec).

5V POWER

The 7I49 requires ~400 mA of 5V power for operation. Power for the 7I49 is normally supplied from P1 but can also be supplied via pin 49 of the 50 conductor controller cable when testing or when low power resolvers are used.

ENABLE INPUTS

There are two active low enable inputs on the 7I49 that come from the FPGA. When either of these enable inputs is high, all AOUTs are forced to 0V, and all enable outputs are turned off. Pullup resistors keep the enable inputs high if the controller connection is lost.

ENABLE OUTPUTS

Each 7I49 channel has a OPTO-isolated transistor output that can be used to enable external amplifiers. All six outputs are on when both input enable signals are low, that is all enable outputs are switched at once. Maximum switched voltage is 36VDC. Maximum output current is 10 mA. Even though all outputs are switched in common, they are all isolated to allow different enable connections on a per amplifier basis.

Example connections:

1. Active high 12V amplifier enable on ch 0:

   Connect ENA0+ to +12V source

   Connect ENA0- to amplifier enable input

2. Active low TTL input

   Connect ENA2- to ground

   Connect ENA2+ to amplifier enable input

ANALOG OUTPUT

The analog output of the 7I49 swings from -10 v to +10V. Positive outputs are generated when PWM+ is input is driven, and negative outputs when PWM- is driven. A 50 % duty cycle PWM signal will generate a 5V output. This mode of operation requires the PWM generator be set for "up/down" mode

The 7I49 has limited DC output drive capability and should not have loads of less than 2K Ohms on its analog outputs.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.75	5.25	VDC
5V POWER CONSUMPTION	---	400	mA
(no external load)			
ANALOG OUTPUT VOLTAGE	+-9.8	+-10.2	V
ANALOG OUTPUT STEP RESPONSE	120	160	uSec
MINIMUM AOUT LOAD RESISTANCE	2K	---	Ohm
OUTPUT RIPPLE @ 24 KHZ PWM	---	.1%	% FS
LINEARITY	---	.1%	% FS
(no missing codes, 13 bit resolution with 24 KHz PWM)			
ZERO OFFSET ERROR	-10	+10	mV
RESOLVER FREQUENCY	2.5	10	KHz
RESOLVER RESOLUTION	12	---	Bits
Typically 14-15 bits with 2:1 resolvers			
RESOLVER ABSOLUTE ACCURACY	11	---	Bits
Typically 12 bits +- resolver inaccuracies			
Can be trimmed			
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND

DRAWINGS