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CNCPROM

Контролер MESA 5I24

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GENERAL

DESCRIPTION

The MESA 5I24 is a low cost, general purpose, FPGA based programmable I/O card for the PCI bus. The 5I24 is a low profile PCI card (available with low profile and standard brackets)

Dual FPGA configuration EEPROMs allow simple recovery from programming mistakes. Firmware modules are provided for hardware step generation, quadrature encoder counting, PWM generation, digital I/O, Smart Serial remote I/O, BISS, SSI, SPI, UART interfaces and more. All motion control firmware is open source and easily modified to support new functions or different mixes of functions.

All I/O bits are 5V tolerant and can sink 24 mA. All I/O pins support 3.3V LVDS inputs. Pullup resistors are provided for all pins so that they may be connected directly to opto-isolators, contacts etc. The 5I24 has 72 I/O bits available on three 50 pin connectors, all connectors use I/O module rack compatible pinouts and are compatible with all Mesa 50 pin FPGA daughtercards.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 5I24 card is oriented in an upright position, that is, with the PCI connector towards the person doing the configuration.

CONNECTOR POWER

The power connection on the I/O connectors pin 49 can supply either 3.3V or 5V power. Supplied power should be limited to 400 mA per connector.

When the following jumpers are in the 'left' position, 5V power is supplied to pin 49 of the associated connector. When the jumper is in the 'right' position, 3.3V power is supplied to to pin 49 of the associated connector.

W8 selects the voltage supplied to P4. (I/O connector for bits 0..23)

W5 selects the voltage supplied to P3. (I/O connector for bits 24..47)

W2 selects the voltage supplied to P2. (I/O connector for bits 48..71)

5V I/O TOLERANCE

The FPGA used on the 5I24 has a 4V absolute maximum input voltage specification. To allow interfacing with 5V inputs, the 5I24 has bus switches on all I/O pins. The bus switches work by turning off when the input voltage exceeds a preset threshold. *The 5V I/O tolerance option is the default and should normally be left enabled.*

For high speed applications where only 3.3V maximum signals are present and overshoot clamping is desired, the 5V I/O tolerance option can be disabled.

When 5V mode is selected, the bus switch is always fully on unless input voltages >3.5V are applied, at which point the bus switch disconnects the FPGA from the I/O pin. 5V mode is suggested for general use.

When the bus switch mode jumper is in the 'up' position, 5V mode is selected, when 'down', 3.3V bus switch mode is selected.

W6 selects the voltage supplied to P4. (I/O connector for bits 0..23)

W3 selects the voltage supplied to P3. (I/O connector for bits 24..47)

W1 selects the voltage supplied to P2. (I/O connector for bits 48..71)

HARDWARE CONFIGURATION

PRECONFIG PULLUP ENABLE

The Xilinx FPGA on the 5I24 has the option of having weak pull-ups on all I/O pins at power-up or reset. The default is to enable the pull-ups To enable the built-in pull-ups, (the default condition) jumper W4 should be placed in the UP position. To disable the internal pull-ups, W4 should be in the DOWN position.

PCI BUS ISOLATION

The 5I24 uses bus switches to provide 5V tolerance on the PCI bus. These bus switches can be turned off to disconnect the FPGA from the PCI bus. This is valuable when debugging FPGA PCI firmware as it allows the system to boot with a non functional PCI interface. W9 controls the PCI bus isolate function. For normal operation W9 must be in the UP position. To disconnect the FPGA from the BUS, move W9 to the DOWN position.

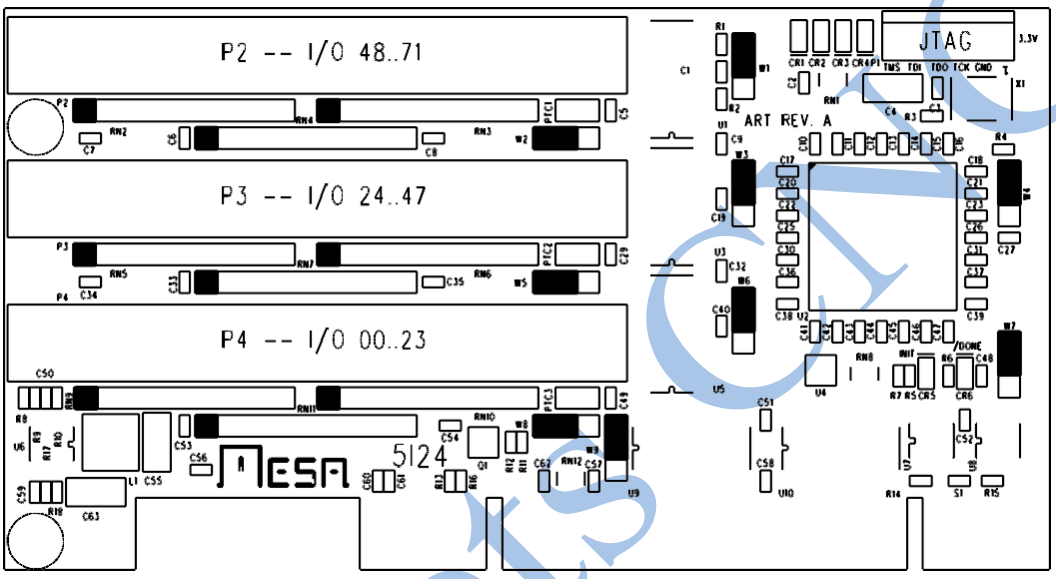
FPGA FLASH SELECT

To make recovery from FPGA configuration errors easier, there are two FPGA configuration flash memories on the 5I24 card. Jumper W7 selects between the two flash memories. That is, if one flash memory is inadvertently corrupted, the other one can be used to boot the 5I24, allowing the corrupted flash memory to be re-written. It is suggested that W7 be left in the UP position (primary flash memory) for normal operation, and only changed to the DOWN position (secondary flash memory) if configuration fails. Once rebooted via a power cycle, jumper W7 should be promptly restored to the UP position to allow the primary flash memory to be re-written.

W7	**MEMORY**
UP	PRIMARY (NORMAL OPERATION)
DOWN	SECONDARY (BACKUP)

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

I/O CONNECTORS

P2, P3, and P4 are the 5I24s I/O connectors. These are 50 pin box headers that mate with standard 50 conductor female IDC connectors. Suggested mating connector is AMP PN 1-1658621-0. Note that the power pin (pin 49) maybe 3.3V or 5V depending on the connector power option.

P4 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO0	2	GND	3	IO1	4	GND
5	IO2	6	GND	7	IO3	8	GND
9	IO4	10	GND	11	IO5	12	GND
13	IO6	14	GND	15	IO7	16	GND
17	IO8	18	GND	19	IO9	20	GND
21	IO10	22	GND	23	IO11	24	GND
25	IO12	26	GND	27	IO13	28	GND
29	IO14	30	GND	31	IO15	32	GND
33	IO16	34	GND	35	IO17	36	GND
37	IO18	38	GND	39	IO19	40	GND
41	IO20	42	GND	43	IO21	44	GND
45	IO22	46	GND	47	IO23	48	GND
49	POWER	50	GND				

DIFFERENTIAL PAIRS

The 5I24 supports LVDS inputs on all I/O pin pairs. 16 LVDS outputs are supported on GPIO pins 44 through 59.

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO24	2	GND	3	IO25	4	GND
5	IO26	6	GND	7	IO27	8	GND
9	IO28	10	GND	11	IO29	12	GND
13	IO30	14	GND	15	IO31	16	GND
17	IO32	18	GND	19	IO33	20	GND
21	IO34	22	GND	23	IO35	24	GND
25	IO36	26	GND	27	IO37	28	GND
29	IO38	30	GND	31	IO39	32	GND
33	IO40	34	GND	35	IO41	36	GND
37	IO42	38	GND	39	IO43	40	GND
41	IO44*	42	GND	43	IO45*	44	GND
45	IO46*	46	GND	47	IO47*	48	GND
49	POWER	50	GND				

* These pins support LVDS output.

CONNECTORS

I/O CONNECTORS

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO48*	2	GND	3	IO49*	4	GND
5	IO50*	6	GND	7	IO51*	8	GND
9	IO52*	10	GND	11	IO53*	12	GND
13	IO54*	14	GND	15	IO55*	16	GND
17	IO56*	18	GND	19	IO57*	20	GND
21	IO58*	22	GND	23	IO59*	24	GND
25	IO60	26	GND	27	IO61	28	GND
29	IO62	30	GND	31	IO63	32	GND
33	IO64	34	GND	35	IO65	36	GND
37	IO66	38	GND	39	IO67	40	GND
41	IO68	42	GND	43	IO69	44	GND
45	IO70	46	GND	47	IO71	48	GND
49	POWER	50	GND				

* These pins support LVDS output.

CONNECTORS

JTAG CONNECTOR PINOUT

P1 is a JTAG programming connector. This is normally used only for debugging or if the EEPROM configuration has been corrupted. In case of corrupted EEPROM contents the EEPROM can be re-programmed using Xilinx's Impact tool. For reprogramming, the card can be powered in a standard PCI slot or if desired, 3.3V power can be applied via the JTAG connector.

P1 JTAG CONNECTOR PINOUT

PIN	FUNCTION
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	+3.3V

OPERATION

FPGA

The 5I24 use a Xilinx Spartan6 X16 or X25 FPGA in a 256 ball BGA package: XC6SLX16FTG256 or XC6SLX25FTG256 depending on 5I24 model.

FPGA PINOUT

The local bus and I/O interface FPGA pinouts are described in the 5i24.ucf file in the /configs/hostmot2/source directory of the 5I24.zip file.

PCI ACCESS

The 5I24 normally uses 5I24 specific HostMot2 firmware which currently has a simple target only PCI core with a single Base Address Register (BAR 0). Card specific PCI identifiers are as follows:

VENDOR ID	0X2718
DEVICE ID	0x5124
SUBSYSTEM VENDOR ID	0x2718
SUBSYSTEM DEVICE ID	0x5124

The single base address register (BAR0) maps a 64K Byte region of non-cacheble 32 bit wide memory.

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OPERATION

CONFIGURATION

GENERAL

The 5I24 is configured at power up by a SPI FLASH memory. This flash memory is an 16M bit chip that has space for two configuration files. Since all PCI logic in the 5I24 is in the FPGA, a problem with configuration means that PCI access will not be possible. For this reason there are two backup methods to recover from FPGA boot failures.

FALLBACK

The first backup system is called Fallback. The 5I24 flash memory normally contains two configuration file images, A user image and a fallback image. If the primary user configuration is corrupted, the FPGA will load the fallback configuration so the flash memory image can be repaired remotely without having to resort to switching memories or JTAG programming.

DUAL EEPROMS

The second backup method relies on the fact that there are two flash memories on the 5I24 card, selectable via jumper W7. If a configuration fails in such a way that it loads correctly (has a valid CRC) but does not work, the fallback configuration will not be invoked. To recover from this problem, the secondary flash can be selected by moving W7 to the DOWN position and using it to boot the FPGA (by cycling the power), restoring host access and allowing the primary configuration to be repaired via the host PCI bus. The backup EEPROM is not write protected so if the primary EEPROM has been corrupted, you should always restore W7 to the UP position to avoid writing a bad configuration to both EEPROMS, necessitating a slow and awkward JTAG bootstrap. .

OPERATION

CONFIGURATION

EEPROM LAYOUT

The EEPROM used on the 5I24 for configuration storage is the M25P16. The M25P16 is a 16 M bit (2 M byte) EEPROM with 32 64KByte sectors. Configuration files are stored on sector boundaries to allow individual configuration file erasing and updating. Standard EEPROM sector layout is as follows:

0x000000	**BOOT BLOCK**
0x010000	**FALLBACK CONFIGURATION BLOCK 0**
0x020000	**FALLBACK CONFIGURATION BLOCK 1**
0x030000	**FALLBACK CONFIGURATION BLOCK 2**
0x040000	**FALLBACK CONFIGURATION BLOCK 3**
0x050000	**FALLBACK CONFIGURATION BLOCK 4**
0x060000	**FALLBACK CONFIGURATION BLOCK 5**
0x070000	**FALLBACK CONFIGURATION BLOCK 6**
0x080000	**FALLBACK CONFIGURATION BLOCK 7 / UNUSED 5I24-16**
0x090000	**FALLBACK CONFIGURATION BLOCK 8 / UNUSED 5I24-16**
0x0A0000	**FALLBACK CONFIGURATION BLOCK 9 / UNUSED 5I24-16**
0x0B0000	**FALLBACK CONFIGURATION BLOCK 10 / UNUSED 5I24-16**
0x0C0000	**FALLBACK CONFIGURATION BLOCK 11 / UNUSED 5I24-16**
0x0D0000	**FALLBACK CONFIGURATION BLOCK 12 / UNUSED 5I24-16**
0x0E0000	**UNUSED/FREE**
0x0F0000	**UNUSED/FREE**

OPERATION

EEPROM LAYOUT

0x100000	USER CONFIGURATION BLOCK 0
0x110000	USER CONFIGURATION BLOCK 1
0x120000	USER CONFIGURATION BLOCK 2
0x130000	USER CONFIGURATION BLOCK 3
0x140000	USER CONFIGURATION BLOCK 4
0x150000	USER CONFIGURATION BLOCK 5
0x160000	USER CONFIGURATION BLOCK 6
0x170000	USER CONFIGURATION BLOCK 7 / UNUSED 5I24-16
0x180000	USER CONFIGURATION BLOCK 8 / UNUSED 5I24-16
0x190000	USER CONFIGURATION BLOCK 0 9 / UNUSED 5I24-16
0x1A0000	USER CONFIGURATION BLOCK 0 10 / UNUSED 5I24-16
0x1B0000	USER CONFIGURATION BLOCK 0 11 / UNUSED 5I24-16
0x1C0000	USER CONFIGURATION BLOCK 0 12 / UNUSED 5I24-16
0x1D0000	UNUSED/FREE
0x1E0000	UNUSED/FREE
0x1F0000	UNUSED/FREE

OPERATION

BITFILE FORMAT

The configuration utilities expects standard FPGA bitfiles without any multiboot features enabled. If multiboot FPGA files are loaded they will likely cause a configuration failure. In addition for fallback to work, the -g next_config_register_write:disable, -g reset_on_error:enable and -g CRC:enable bitgen options must be set.

NMFLASH

The DOS utility program NMFLASH is provided to write configuration files to the 5I24 EEPROM under DOS. NMFLASH depends on a simple SPI interface built into both the standard user FPGA bitfiles and the fallback bitfile.

NMFLASH FPGAFILE.BIT

Writes a standard bitfile FPGAFILE.BIT to the user area of the EEPROM

NMFLASH FPGAFILE.BIT V

Verifies the user EEPROM configuration against the bit file FPGAFILE.BIT

NMFLASH FALLBACK.BIT FallBack

Writes the fallback EEPROM configuration to the fallback area of the EEPROM. In addition if the bootblock is not present in block 0 of the EEPROM, it re-writes the bootblock.

NMFLASH requires the following environment variables to be set before operation: INTERFACE=PCIMEM and PROTOCOL=DIRECT.

MESAFLASH

Linux and Windows utility programs mesaflash and mesaflash.exe are provided to write configuration files to the 5I24 EEPROM. These files depend on a simple SPI interface built into both the standard user FPGA bitfiles and the fallback bitfile.

If mesaflash is run with no command line arguments it will print usage information.

mesaflash --device 5I24 --write FPGAFILE.BIT

Writes a standard bitfile FPGAFILE.BIT to the user area of the EEPROM.

mesaflash --device 5I24 --verify FPGAFILE.BIT

Verifies the user EEPROM configuration against the bit file FPGAFILE.BIT.

mesaflash --device 5I24 --fallback --write FALLBACK.BIT

Writes FALLBACK.BIT to the fallback area of the 5I24's EEPROM.

OPERATION

FPGA CONFIGURATION

Once the flash EEPROM has been written by either the nmflash or mesaflash utility, the 5I24 power must be cycled to load the new firmware into the FPGA. This must be a full power cycle, a reboot operation will not reload the FPGA.

SPI INTERFACE DESCRIPTION

This is the register level description of the simple SPI interface to the 5I24's configuration EEPROM. This hardware is built into all Mesa 5I24 configurations. This information is only needed if you are writing your own programming utility.

DATA REGISTER at offset 0x74 from 5I24 base address

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CONTROL REGISTER at offset 0x70 from 5I24 base address

X	X	X	X	X	DAV	BUSY	CS
X	X	X	X	X	R/O	R/O	R/W

The SPI interface is very minimal, just enough hardware to avoid slow bit banging of the SPI data when reading or writing the configuration EEPROM. Operation is as follows: To transfer SPI data, CS is asserted low and an outgoing command/data byte is written to the data register. This write to the data register causes the SPI interface to clear its DAV bit, shift out its outgoing data byte, and shift in its incoming data. This shifting is done at a fixed PCI Clock/3 rate or about 11 MHz. When the byte data transfer is done, The DAV bit is set in the control register. Host software can poll this bit to determine when the transfer is done. When the transfer is done the incoming data from the EEPROM can be read in the data register, and the next byte sent out.

Note that CS operation is entirely controlled by the host, that is for example with a 5 byte command sequence, the host must assert CS low, transfer 5 bytes with 5 write/read commands to the data register with per byte DAV bit polling and finally assert CS high when done.

OPERATION

FREE EEPROM SPACE

Three 64K byte blocks of EEPROM space are free when both user and fallback configurations are installed. It is suggested that only the last two blocks, 0xE0000 and 0xF0000 in the user area, be used for FPGA application EEPROM storage.

FALLBACK INDICATION

Mesa's supplied fallback configurations blink the red INIT LED on the top right hand side of the card if the primary configuration fails and the fallback configuration loaded successfully. If this happens it means the user configuration is corrupted or not a proper configuration for the 5I24s FPGA. This can be fixed by running the configuration utility and re-writing the user configuration**.**

FAILURE TO CONFIGURE

The 5I24 should configure its FPGA within a fraction of a second of power application. If the FPGA card fails to configure, both red LEDs on the right hand side of the card will remain illuminated after power up. If this happens the 5I24s EEPROM must be re-programmed via the JTAG connector.

CLOCK SIGNALS

The 5I24 has two FPGA clock signals. One is the PCI clock and the other is a 50 MHz crystal oscillator on the 5I24 card. Both clocks a can be multiplied and divided by the FPGAs clock generator block to generate a wide range of internal clock signals. Note that the PCI bus clock is often not known to a high degree of accuracy so for accurate timing applications, the on card 50 MHz oscillator should be used.

OPERATION

LEDS

The 5I24 has 4 FPGA driven user LEDs, and 2 status LEDs (red and yellow). The user LEDs can be used for any purpose, and can be helpful as a simple debugging feature. A low output signal from the FPGA lights the LED. The status LEDs reflect the state of the FPGA's DONE, and /INIT pins. The /DONE LED lights until the FPGA is configured at power-up. The /INIT LED lights when the power on reset is asserted, when there has been a CRC error during configuration. When using Mesas configurations, the /INIT LED blinks when the fallback configuration has been loaded.

PULLUP RESISTORS

All I/O pins are provided with pull-up resistors to allow connection to open drain, open collector, or OPTO devices. These resistors have a value of 3.3K so have a maximum pull-up current of 1.5 mA (5V pull-up) or 1 mA (3.3V pull-up).

Note that all pull-up resistor networks are socketed so can be removed if pull-up resistors on the I/O pins are not wanted. In addition the pull-up resistors can be reversed in their sockets if pull-downs are required.

IO LEVELS

The Xilinx FPGAs used on the 5I24 have programmable I/O levels for interfacing with different logic families. The 5I24 does not support use of the I/O standards that require input reference voltages. All standard Mesa configurations use LVTTL levels.

Note that even though the 5I24 can tolerate 5V signal inputs, its outputs will not swing to 5V. The outputs are push pull CMOS that will drive to the output supply rail of 3.3V. This is sufficient for TTL compatibility but may cause problems with some types of loads. For example when driving an LED that has its anode connected to 5V, in such devices as OPTO isolators and I/O module rack SSRs, the 3.3V high level may not completely turn the LED off. To avoid this problem, either drive loads that are ground referred, Use 3.3V as the VCC for VCC referred loads, or use open drain mode.

STARTUP I/O VOLTAGE

After power-up or system reset and before the the FPGA is configured, the pull-up resistors in there default position will pull all I/O signals to a high level. If the FPGA is used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state results in a safe condition.

SUPPLIED CONFIGURATIONS

HOSTMOT2

All supplied configurations are part of the HostMot2 motion control firmware set. All HostMot2 firmware is open source and easily extendible to support new interfaces or different sets of interfaces embedded in one configuration. For detailed register level information on Hostmot2 firmware modules, see the regmap file in the hostmot2 source code directory.

SVST8_4IM2

SVST8_4IM2 is a 8 axis servo/ 4 axis stepmotor configuration with 8 PWM outputs, 8 encoder inputs with index mask, 4 hardware stepgenerators, a watchdog timer and GPIO.

SVST4_8

SVST4_8 is a 4 axis servo/ 8 axis stepmotor configuration with 4 PWM outputs, 4 encoder inputs, 8 hardware stepgenerators, a watchdog timer and GPIO.

SVST8_8IM2

SVST8_8IM2 is a 8 axis servo/ 8 axis stepmotor configuration with 8 PWM outputs, 8 encoder inputs with index mask, 8 hardware stepgenerators, a watchdog timer and GPIO.

SVST1_4_7I47S

SVST1_4_7I47S is a 4 axis stepmotor configuration with 1 PWM output for spindle, and 4 encoder inputs, a watchdog timer and GPIO. For the 7I47S card.

2X7I65

2X7I65 is a configuration for up to two 7I65 octal analog servo interface cards. It has 16 encoder inputs, 2 SPI ports, a watchdog timer and GPIO.

SV12IM_2X7I48

SV12IM_7I48 is a 12 axis servo configuration fro two 7I48 daughter cards. It has 12 encoder inputs, 12 PWM outputs, a watchdog timer and GPIO.

SV6_7I49

SV6_7I49 is a six axis servo configuration for use with the 7I49 resolver input daughter card. Its has a 6 channel resolver interface, 6 pwm channels, a watchdog timer and GPIO.

SUPPLIED CONFIGURATIONS

PIN FILES

Each of the configurations has an associated file with file name extension .pin that describes the FPGA functions included in the configuration and the I/O pinout. These are plain text files that can be printed or viewed with any text editor.

REFERENCE

SPECIFICATIONS

POWER	MIN	MAX	NOTES:
3.3V POWER SUPPLY	3.1V	3.5 V	PCI supplied 3.3V
5V POWER SUPPLY	4.5V	5.5V	PCI supplied 5V
3.3V POWER CONSUMPTION:	----	400 mA	Depends on FPGA Configuration
MAX 5V CURRENT TO I/O CONNS	----	700 mA	Each (PTC Limit)
TEMPERATURE RANGE -C version	0 ^{o}C	+70 ^{o}C	
TEMPERATURE RANGE -I version	-40 ^{o}C	+85 ^{o}C	