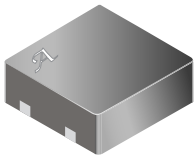
# A3212

Data Sheet
27622.61G

## *MICROPOWER, ULTRA-SENSITIVE HALL-EFFECT SWITCH*

2 x 2 mm MLPD
Package A3212EELLT-T



Approximate actual size

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$ ..... **5 V**

Magnetic Flux Density, B ..... **Unlimited**

Output Off Voltage, $V_{OUT}$ ..... **5 V**

Output Current, $I_{OUT}$ ..... **1 mA**

Junction Temperature, $T_J$ ..... **+170°C**

Operating Temperature, $T_A$

Range 'E-' ..... **-40°C to +85°C**

Range 'L-' ..... **-40°C to +150°C**

Storage Temperature Range,

$T_S$ ..... **-65°C to +170°C**

*Caution: These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.*

The A3212 integrated circuit is an ultra-sensitive, pole independent Hall-effect switch with a latched digital output. This sensor is especially suited for operation in battery-operated, hand-held equipment such as cellular and cordless telephones, pagers, and palmtop computers. A 2.5 volt to 3.5 volt operation and a unique clocking scheme reduce the average operating power requirements to less than 15 µW with a 2.75 volt supply.

Unlike other Hall-effect switches, either a north or south pole of sufficient strength will turn the output on; in the absence of a magnetic field, the output is off. The polarity independence and minimal power requirement allow these devices to easily replace reed switches for superior reliability and ease of manufacturing, while eliminating the requirement for signal conditioning.

Improved stability is made possible through chopper stabilization (dynamic offset cancellation), which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

This device includes on a single silicon chip a Hall-voltage generator, small-signal amplifier, chopper stabilization, a latch, and a MOSFET output. Advanced BiCMOS processing is used to take advantage of low-voltage and low-power requirements, component matching, very low input-offset errors, and small component geometries.

Four package styles provide magnetically optimized solutions for most applications. Miniature low-profile surface-mount package types *EH* and *EL* (0.75 and 0.50 mm nominal height) are leadless, *LH* is a leaded low-profile SMD, and *UA* is a three-lead SIP for through-hole mounting. Each package is available in a lead (Pb) free version (suffix, *–T*) with 100% matte tin plated leadframe. EL package for limited release, engineering samples available.

FEATURES

- Micropower Operation
- Operation with North or South Pole
- 2.5 V to 3.5 V Battery Operation
- Chopper Stabilized
  Superior Temperature Stability
  Extremely Low Switch-Point Drift
  Insensitive to Physical Stress
- ESD Protected to 5 kV
- Solid-State Reliability
- Small Size
- Easily Manufacturable with Magnet Pole Independence

Pb

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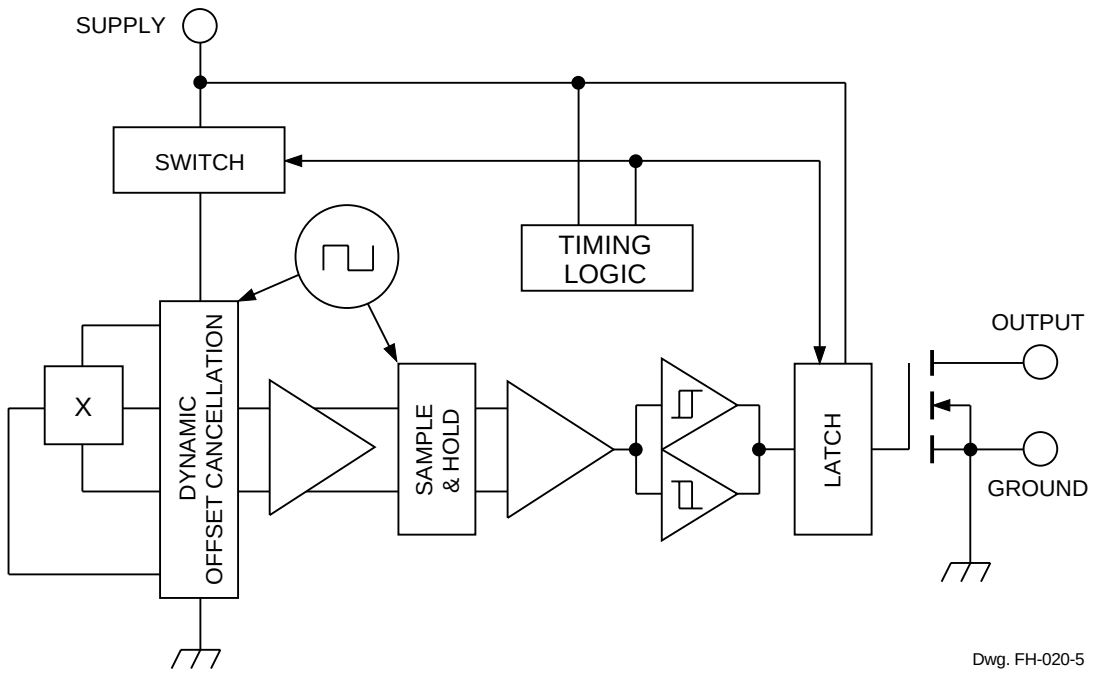
## Product Selection Guide

Use complete part numbers when ordering

| Part Number | Pb-free | Packing* (Units/Pack) | Package | Ambient Temperature $T_A$ (°C) |
|---|---|---|---|---|
| A3212EEHLT | – | Tape and Reel (3000) | Leadless Surface Mount | –40 to 85 |
| A3212EEHLT–T | Yes | Tape and Reel (3000) | | |
| A3212EELLT–T | Yes | Tape and Reel (2000) | | |
| A3212ELHLT | – | Tape and Reel (3000) | 3-Pin Surface Mount | |
| A3212ELHLT–T | Yes | Tape and Reel (3000) | | |
| A3212EUA | – | Bulk Pack (500) | SIP-3 Through Hole, Straight Lead | |
| A3212EUA–T | Yes | Bulk Pack (500) | | |
| A3212LLHLT | – | Tape and Reel (3000) | 3-Pin Surface Mount | –40 to 150 |
| A3212LLHLT–T | Yes | Tape and Reel (3000) | | |
| A3212LUA | – | Bulk Pack (500) | SIP-3 Through Hole, Straight Lead | |
| A3212LUA–T | Yes | Bulk Pack (500) | | |

*Contact Allegro for additional packaging and handling options.

### FUNCTIONAL BLOCK DIAGRAM



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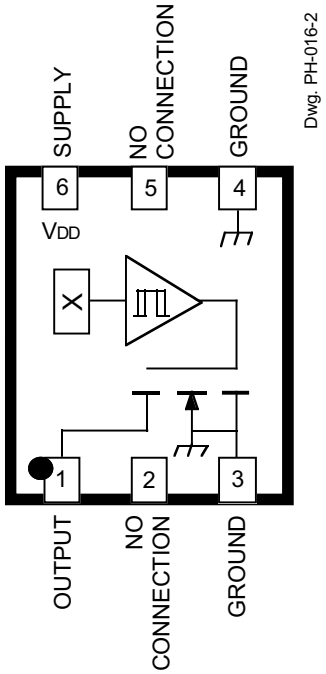
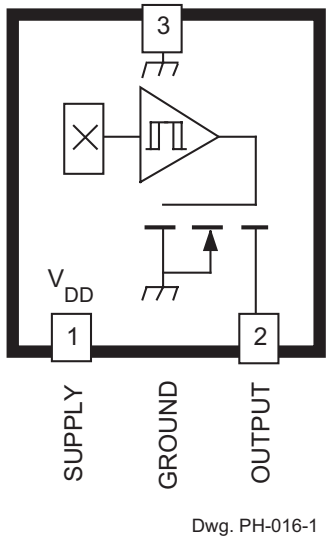
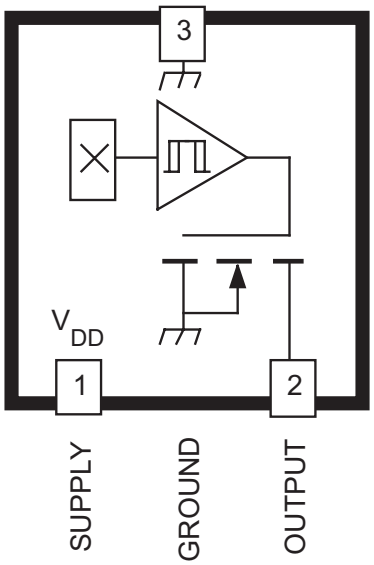
**Package Suffix 'EH' Pinning**
**(Leadless Chip Carrier)**



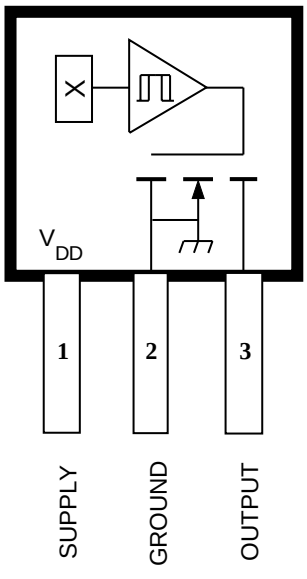

**Package Suffix 'EL' Pinning**
**(Leadless Chip Carrier)**




**Package Suffix 'LH' Pinning**
(SOT23W)




**Package Suffix 'UA' Pinning**
(SIP)




Pinning is shown viewed from branded side.

## ELECTRICAL CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified).

| Characteristic | Symbol | Test Conditions | Limits | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Units |
| Supply Voltage Range | $V_{DD}$ | Operating[1] | 2.5 | 2.75 | 3.5 | V |
| Output Leakage Current | $I_{OFF}$ | $V_{OUT}$ = 3.5 V, $B_{RPN} < B < B_{RPS}$ | – | <1.0 | 1.0 | µA |
| Output On Voltage | $V_{OUT}$ | $I_{OUT}$ = 1 mA, $V_{DD}$ = 2.75 V | – | 100 | 300 | mV |
| Awake Time | $t_{awake}$ | | – | 45 | 90 | µs |
| Period | $t_{period}$ | | – | 45 | 90 | ms |
| Duty Cycle | d.c. | | – | 0.1 | – | % |
| Chopping Frequency | $f_C$ | | – | 340 | – | kHz |
| Supply Current | $I_{DD(EN)}$ | Chip awake (enabled) | – | – | 2.0 | mA |
| | $I_{DD(DIS)}$ | Chip asleep (disabled) | – | – | 8.0 | µA |
| | $I_{DD(AVG)}$ | $V_{DD}$ = 2.75 V | – | 5.1 | 10 | µA |
| | | $V_{DD}$ = 3.5 V | – | 6.7 | 10 | µA |

NOTES: 1. Operate and release points will vary with supply voltage.
2. $B_{OPx}$ = operate point (output turns on); $B_{RPx}$ = release point (output turns off).
3. Typical Data is at $T_A$ = +25°C and $V_{DD}$ = 2.75 V and is for design information only.

## MAGNETIC CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified).

| Characteristic | Symbol | Test Conditions | Limits | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Units |
| Operate Points | $B_{OPS}$ | South pole to branded side | – | 37 | 55 | G |
| | $B_{OPN}$ | North pole to branded side | -55 | -40 | – | G |
| Release Points | $B_{RPS}$ | South pole to branded side | 10 | 31 | – | G |
| | $B_{RPN}$ | North pole to branded side | – | -34 | -10 | G |
| Hysteresis | $B_{hys}$ | $\lvert B_{OPx} - B_{RPx} \rvert$ | – | 5.9 | – | G |

NOTES: 1. Negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.
2. $B_{OPx}$ = operate point (output turns on); $B_{RPx}$ = release point (output turns off).
3. Typical Data is at $T_A$ = +25°C and $V_{DD}$ = 2.75 V and is for design information only.
4. 1 gauss (G) is exactly equal to 0.1 millitesla (mT).



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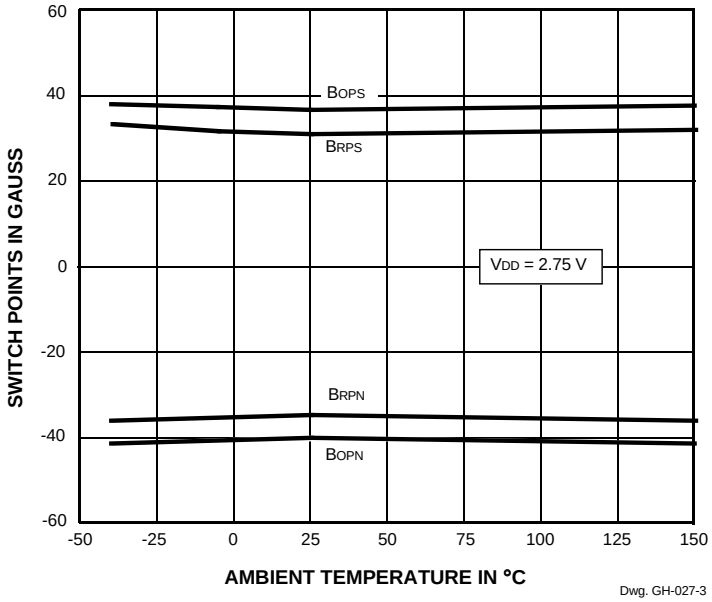
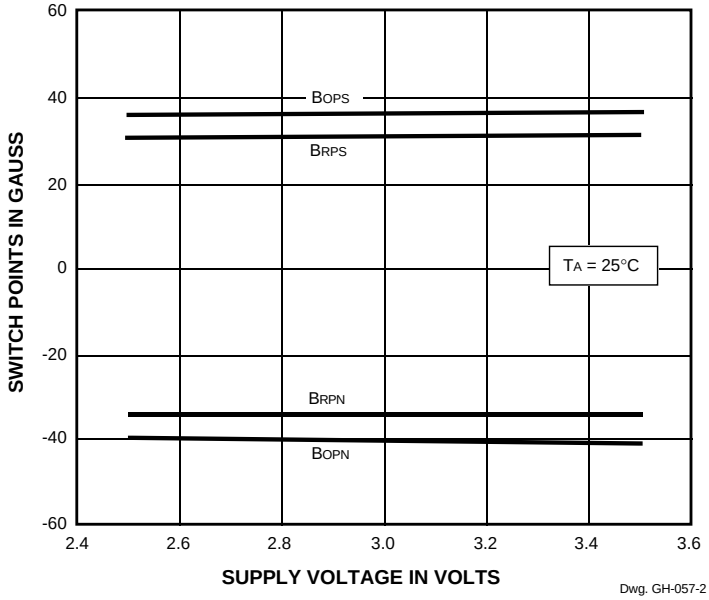
## TYPICAL OPERATING CHARACTERISTICS

### SWITCH POINTS

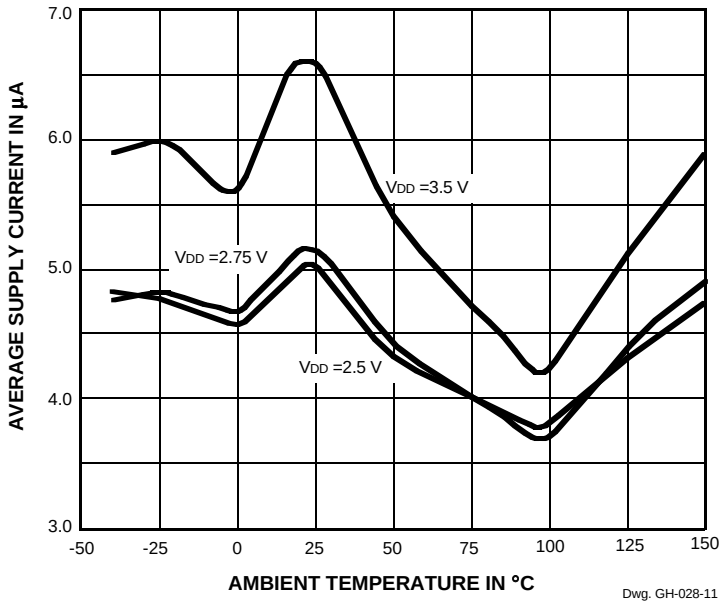



Dwg. GH-027-3

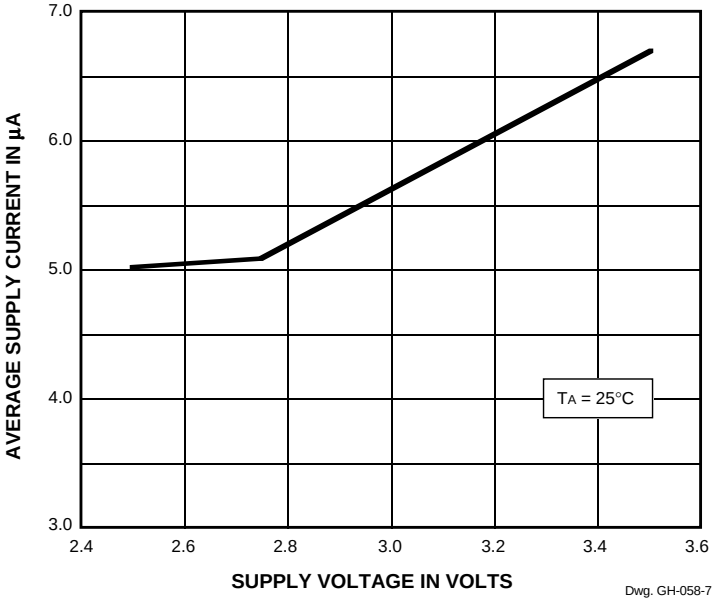



Dwg. GH-057-2

### SUPPLY CURRENT



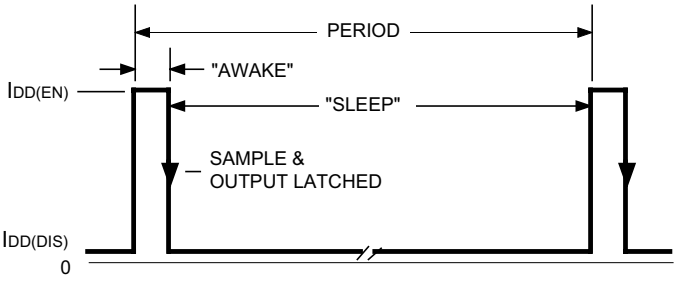

Dwg. GH-028-11




Dwg. GH-058-7

## FUNCTIONAL DESCRIPTION

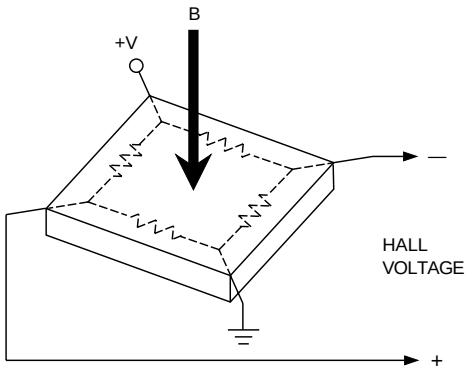
**Low Average Power.** Internal timing circuitry activates the sensor for 45 µs and deactivates it for the remainder of the period (45 ms). A short "awake" time allows for stabilization prior to the sensor sampling and data latching on the falling edge of the timing pulse. The output during the "sleep" time is latched in the last sampled state. The supply current is not affected by the output state.



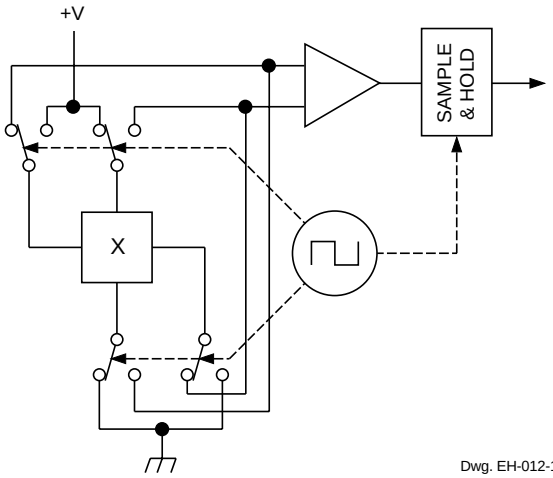

Dwg. WH-017-2

**Chopper-Stabilized Technique.** The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaing the Hall-voltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. A relatively high sampling frequency is used for faster signal processing capability can be processed.

More detailed descriptions of the circuit operation can be found in: Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensor Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.




Dwg. AH-011-2




Dwg. EH-012-1



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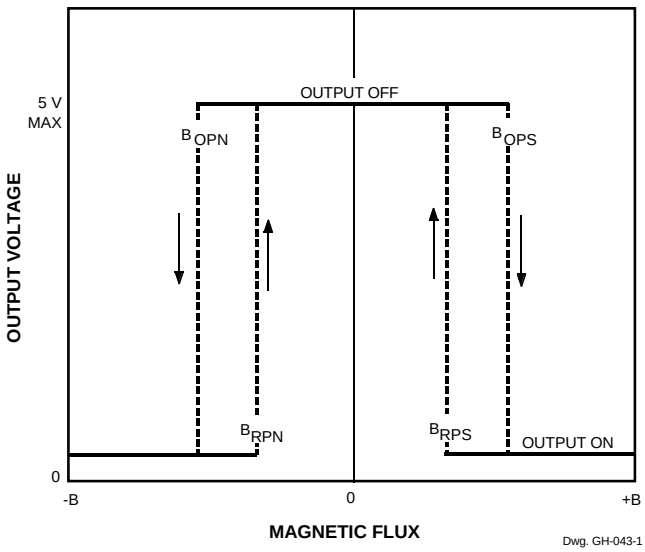
## FUNCTIONAL DESCRIPTION (cont'd)

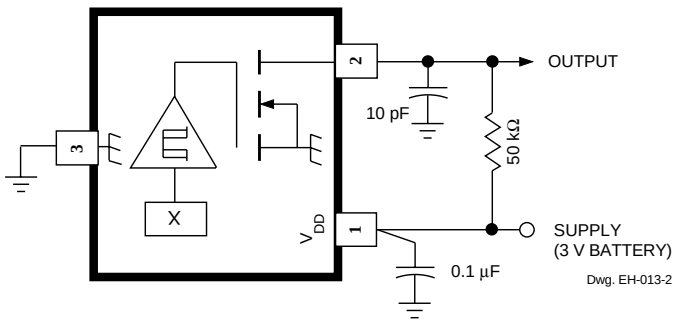
**Operation.** The output of this device switches low (turns on) when a magnetic field perpendicular to the Hall sensor exceeds the operate point $B_{OPS}$ (or is less than $B_{OPN}$). After turn-on, the output is capable of sinking up to 1 mA and the output voltage is $V_{OUT(ON)}$. When the magnetic field is reduced below the release point $B_{RPS}$ (or increased above $B_{RPN}$), the device output switches high (turns off). The difference in the magnetic operate and release points is the hysteresis ($B_{hys}$) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

As used here, negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.




**Applications.** Allegro's pole-independent sensing technique allows for operation with either a north pole or south pole magnet orientation, enhancing the manufacturability of the device. The state-of-the-art technology provides the same output polarity for either pole face.

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. This is especially true due to the relatively high impedance of battery supplies.




The simplest form of magnet that will operate these devices is a bar magnet with either pole near the branded surface of the device. Many other methods of operation are possible. Extensive applications information for Hall-effect sensors is available in:

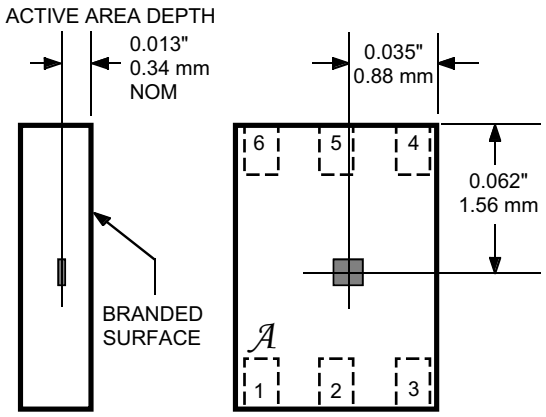
• *Hall-Effect IC Applications Guide*, Application Note 27701;
• *Hall-Effect Devices: Soldering, Gluing, Potting, Encapsulating, and Lead Forming*, Application Note 27703.1;
• *Soldering of Through-Hole Hall-Sensor Dervices*, Application Note 27703; and
• *Soldering of Surface-Mount Hall-Sensor Devices*, Application Note 27703.2.

All are provided at

www.allegromicro.com

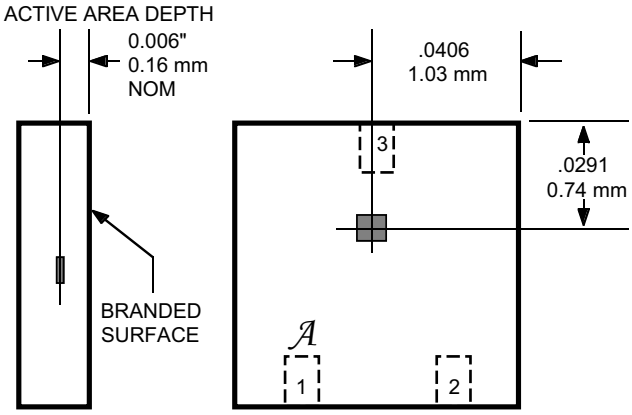
## SENSOR LOCATIONS

Package Designator 'EH'

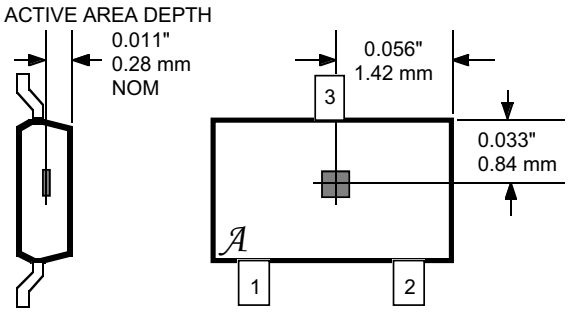



Dwg. MH-030

Package Designator 'EL'

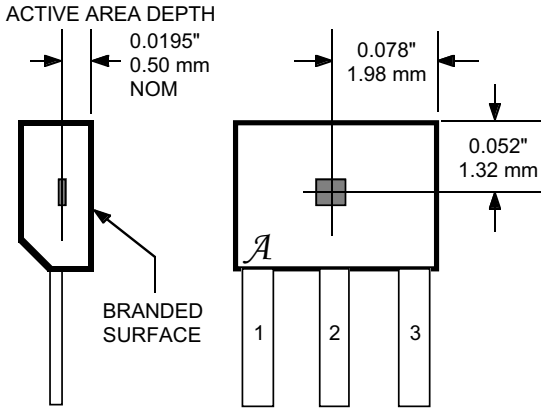



Package Designator 'LH'




Dwg. MH-025-2

Package Designator 'UA'




Dwg. MH-011-13



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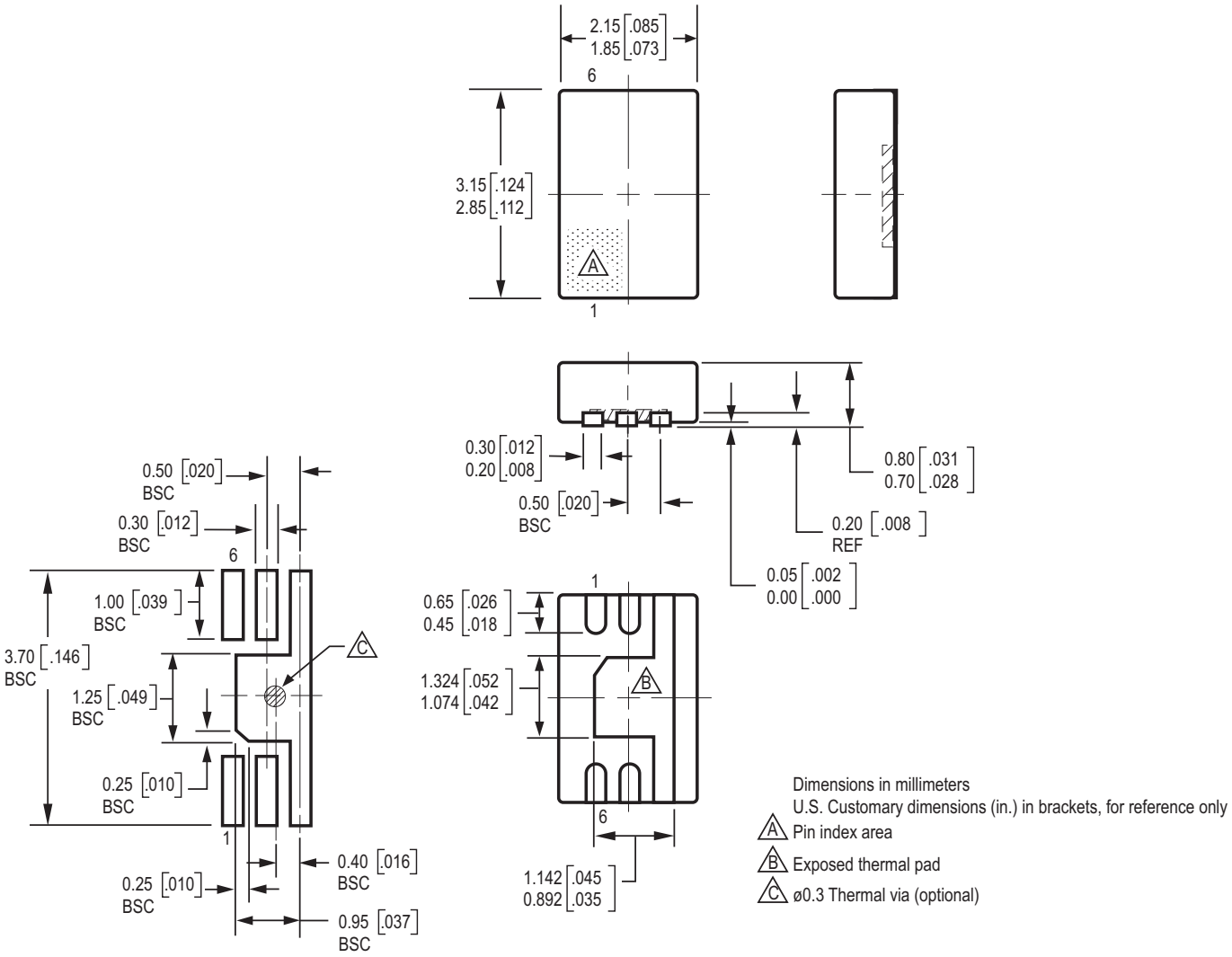
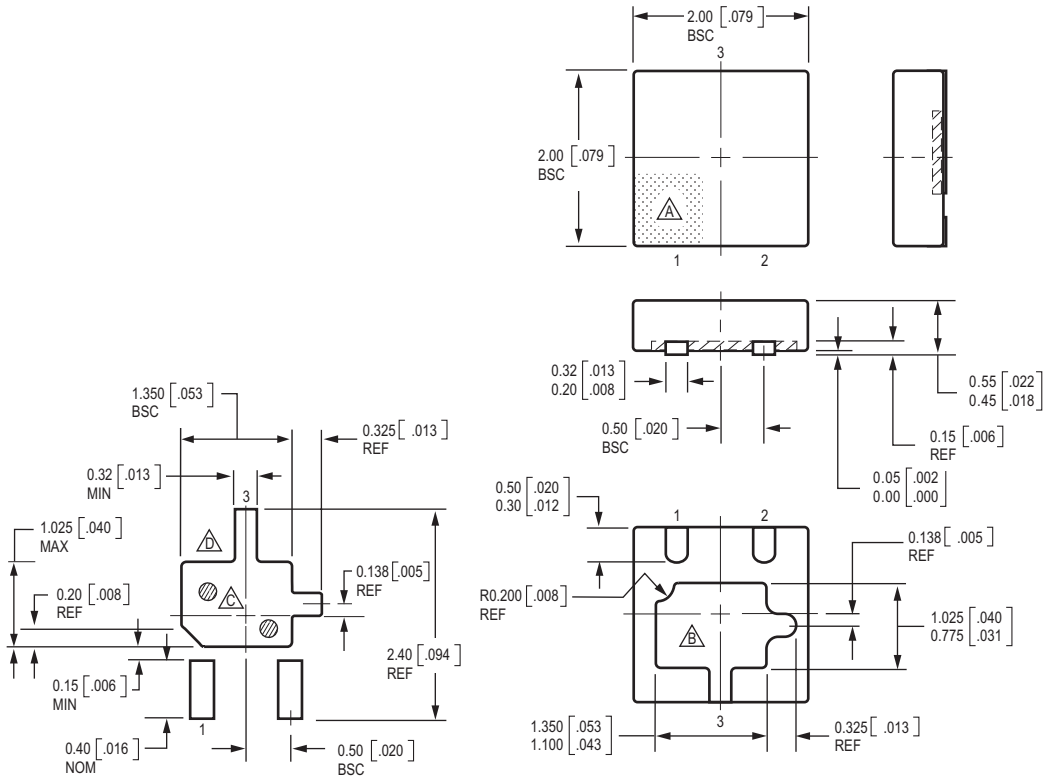
## PACKAGE DESIGNATOR 'EH'

(Reference MO-229C WCED-1)



## PACKAGE DESIGNATOR 'EL'

MLPD 3 Contact




Dimensions in millimeters
U.S. Customary dimensions (in.)
in brackets, for reference only

A Pin index area

B Exposed thermal pad

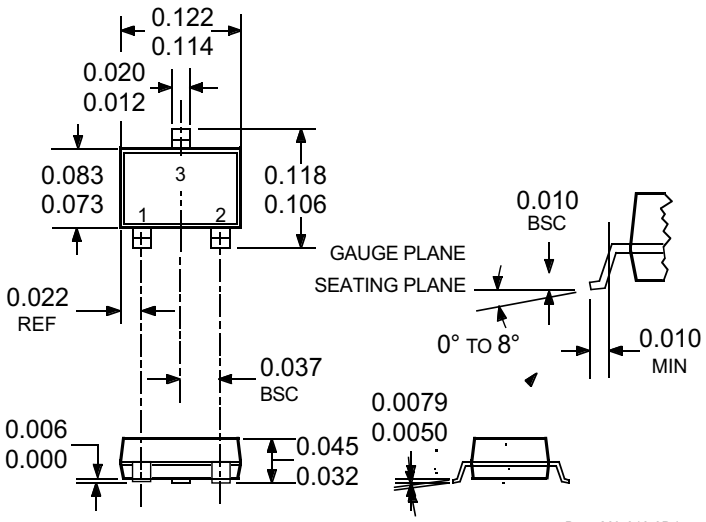
C Optional thermal vias, ∅0.30 [.012], pitch 1.2 [.047]

D Typical pad layout; adjust as necessary to meet application process requirements

## PACKAGE DESIGNATOR 'LH'

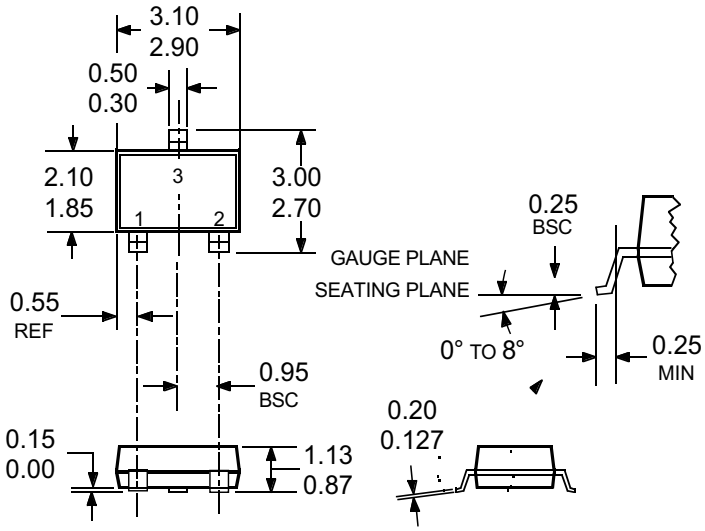
(SOT23W, fits SC-59A solder-pad layout)

Dimensions in Inches
(for reference only)

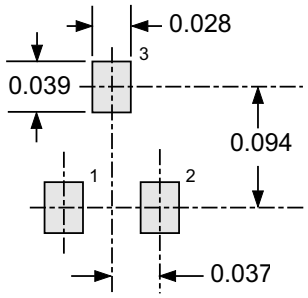



Dwg. MA-010-3D in

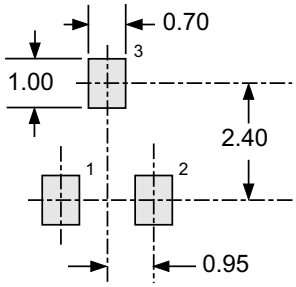
Dimensions in Millimeters
(controlling dimensions)




Dwg. MA-010-3D mm




Dwg. MA-011-3 in

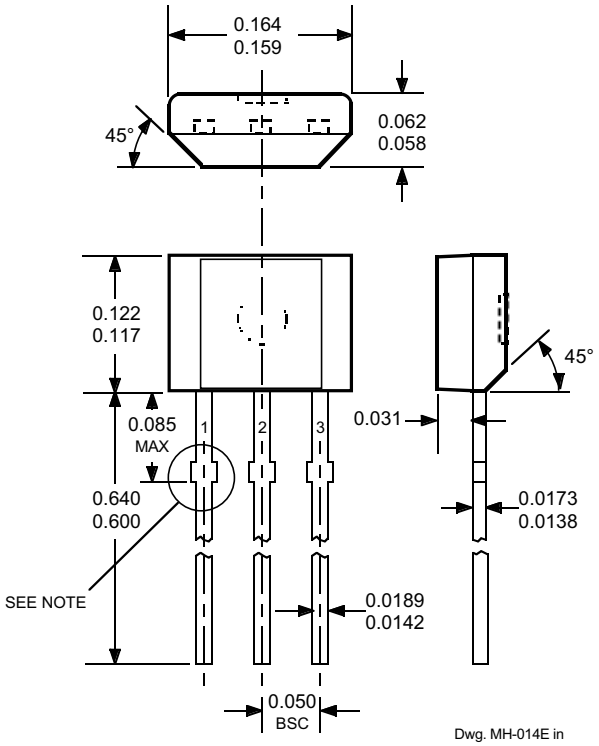



Dwg. MA-011-3 mm

NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Where no tolerance is specified, dimension is nominal.

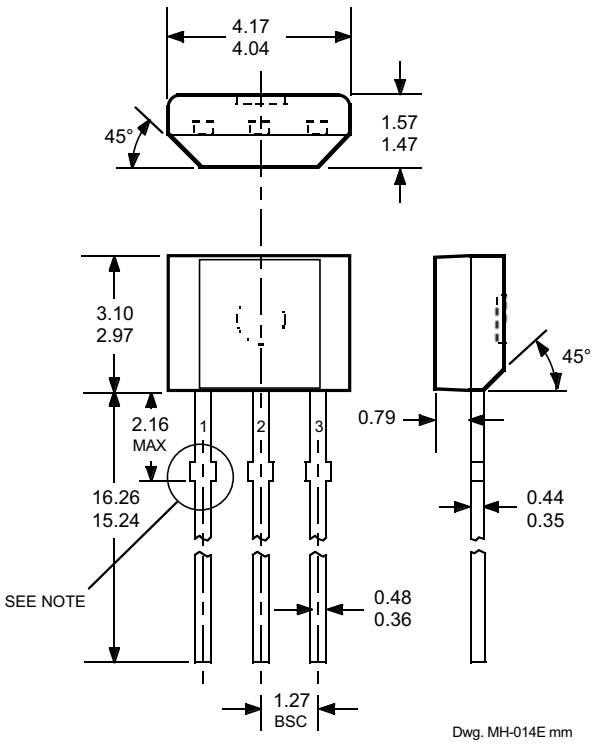
## PACKAGE DESIGNATOR 'UA'

Dimensions in Inches
(controlling dimensions)




Dwg. MH-014E in

Dimensions in Millimeters
(for reference only)




Dwg. MH-014E mm

NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.



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*The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.*

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