



RTS5450M

Type-C Power Delivery Controller

DATASHEET

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Revision History

Revision	Description	Page	Date
0.90	First release		2018/03/21
0.91	Modify 6.4		2018/03/26
0.92	<ol style="list-style-type: none">1. Correct the pin2 name in Figure 5-12. Remove DCI function description in the datasheet3. Remove DP/DM charger function in the datasheet4. Add the VCONN power switch input voltage range in section 6.2.5. Add VCONN power switch ON resistor and OFF leakage in section 6.36. Change the minimum value of 5V_IN power supply in section 6.27. Change the 5V digital IO maximum ratings in section 6.1.8. Change the 5V digital IO VIH VIL VOH VOL in section 6.3.9. Update the application block diagram in section 7.10. Add DC characteristic of combine IO in section 6.3.		2018/06/05

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1. General Description

RTS5450M is an advanced Type-C Power Delivery Controller, which integrates all Type-C Channel Configuration (CC) function, Power Delivery function (including BMC PHY, protocol, policy engine and device policy manager), 10Gbps high speed MUXs, low speed MUX, billboard device, AUX/HPD detection blocks and VCONN switches with over-current protection into a single chip. It also builds in a high speed switch to implement billboard device functions. The AUX and HPD detection blocks are used for detecting DP cable hot plug and HPD signals in order to support the DisplayPort Alt mode. That could apply to various applications and dramatically reduce the system BOM cost. Furthermore some new features in PD3.0 spec as Fast Role Swap, Extended Message transmission, PD FW update and so on are implemented in RTS5450M.

RTS5450M's Built-In 10Gbps 3:2 MUX can contribute to Type-C plug flipping as well as support for 4 lane alternate mode (e.g. DisplayPort) and USB3.X SS switching. That could apply to various applications and dramatically reduce the system BOM cost. It also builds in a low speed MUX switching for SBU1/2 polarity swap in alternate mode (e.g. AUX+/- of DisplayPort). These MUXs will simplify the design of the monitor or PCs systems including DisplayPort or other alternate modes.

The firmware inside the RTS5450M complies with the USB Type-C Specification Release 1.2 spec and Power Delivery spec R3.0 V1.0. All the configurations such as power roles, data roles and current modes of the type-c port can be configured by firmware flexibly. The MCU and firmware also implements the PD Protocols, including the Policy Engine (PE), Device Policy Management (DPM). RTS5450M has various interfaces to communicate with other components, such as GPIO, I2C, and SMBUS. It's flexible for extending varieties of applications by using these interfaces as well as be easier to add Type-C USB Power Delivery to any architecture. Benefit from RTS5450M's SMBUS/I2C slave interface, system can implement system control achieving all the Power Delivery related functions, such as Cable detection, Power Negotiation, Power Swap, Data Swap and VCONN Swap etc. Moreover, RTS5450M can be statically be configured via SMBUS to customize extra functions. With the I2C master interface, RTS5450M can control/configure other chip in the system, such as PMIC with I2C etc. See more details in section 8.

RTS5450M can update its firmware with an embedded SPI flash via flexible ISP channels. With the ISP function, it can configure lots of features and settings by the embedded SPI flash. The ISP function is easy to complete via USB/SMBUS/CCs download tools.

RTS5450M adopts an industry standard 46 pins QFN Green package and the size is 4.5mm*6.5mm.

2. Features

- Compliant with USB Type-C Specification Release 1.2 spec
 - Support being configured as DFP, UFP or DRP.
 - Attach and port power-role detection.
 - Cable Orientation Detection.
 - Type-C current mode detection/configuration as UFP/DFP after connection.
 - Audio Accessory mode detection.
- Compliant with USB Power Delivery Spec 3.0 V1.0
 - Integrated USB Power Delivery (PD BMC) PHY.
 - Support for Message Protocol.
 - Support for Policy Engine.
 - Support for Device Policy Manager.
 - Support Fast Role Swap.
 - Support Extended Message (both chunked and unchunked transmission).
- Support PD FW update via Firmware Update Extended Messages
- Built-In VCONN switches with over-current protection and support up to 300mA loading.
- Built-In low speed MUX for SBU1/2 switching in alternate mode (e.g. AUX+/- of DisplayPort).
- Built-In 10Gbps 3:2 MUX for 4 lane alternate mode (e.g. DisplayPort) and USB3.X SS switching ⁽¹⁾.
- Built-In configurable HS/FS billboard device.
- Built-In 10bit SAR ADC which can monitor VBUS voltage /current, battery voltage and so on.
- Digital auto-scan and comparator block of ADC which contributes to fast response to system alarm.
- Support presenting dead battery 'Rd' on CCs.
- Support SMBUS/I2C slave for customized configurations and system control.
- Support I2C master to configure other chips on the same platform.
- Integrated microprocessor.
- Support serial flash for ISP function which can upgrade Firmware or configurations via USB/SMBUS/CCs directly.
- Support Crystal-less mode.
- Integrated 3.3V and 1.2V LDO regulators.
- Ultra-low power consumption when the type-c is disconnected.

Note:

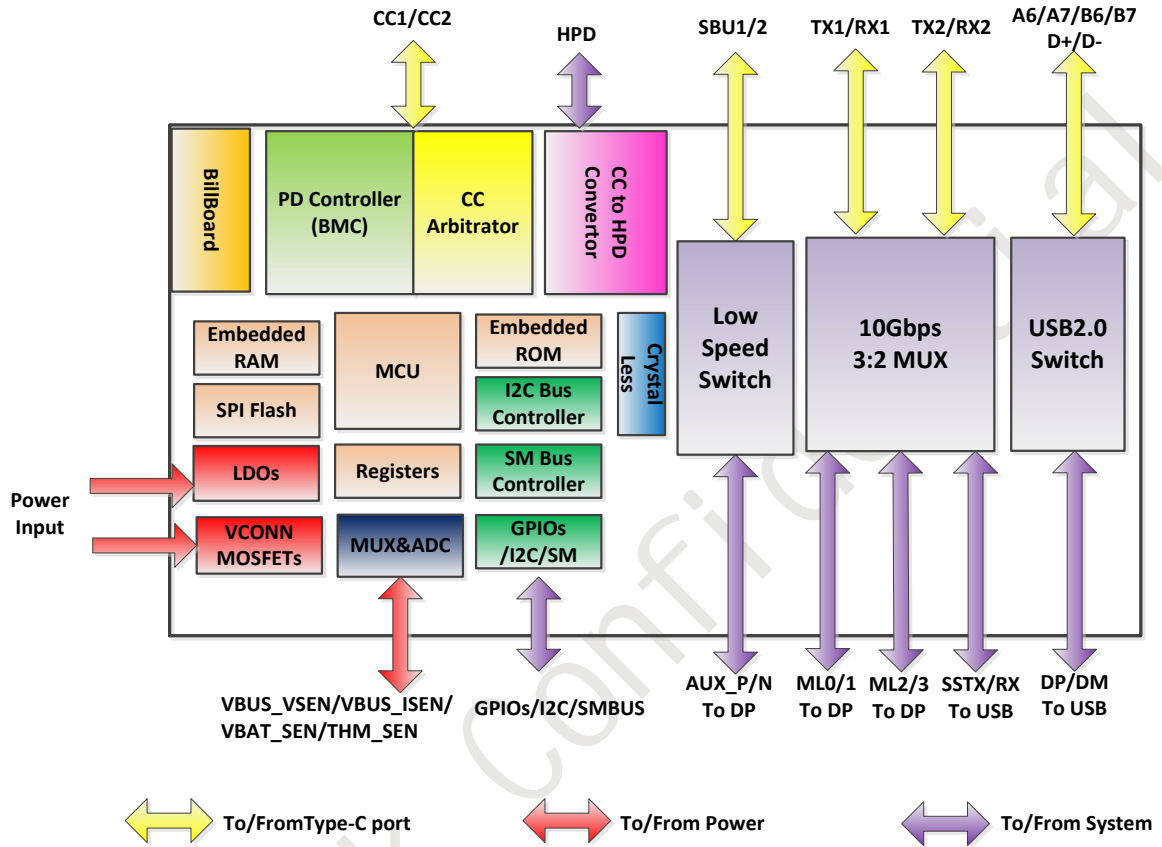
(1). In order to ensure the USB3.1 Gen2 10Gbps signal integrity, the external 10Gbps re-driver or re-timer chip is highly recommended to be used with RTS5450M for USB3.1 Gen2 applications. Please refer to the related reference schematics.

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3. Applications

- Cellphones
- Notebooks, Desktops
- Dockings
- Monitors
- AC Adaptors, Power Bank

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4. Block Diagram


5. Pin Information

5.1 Pin Assignment

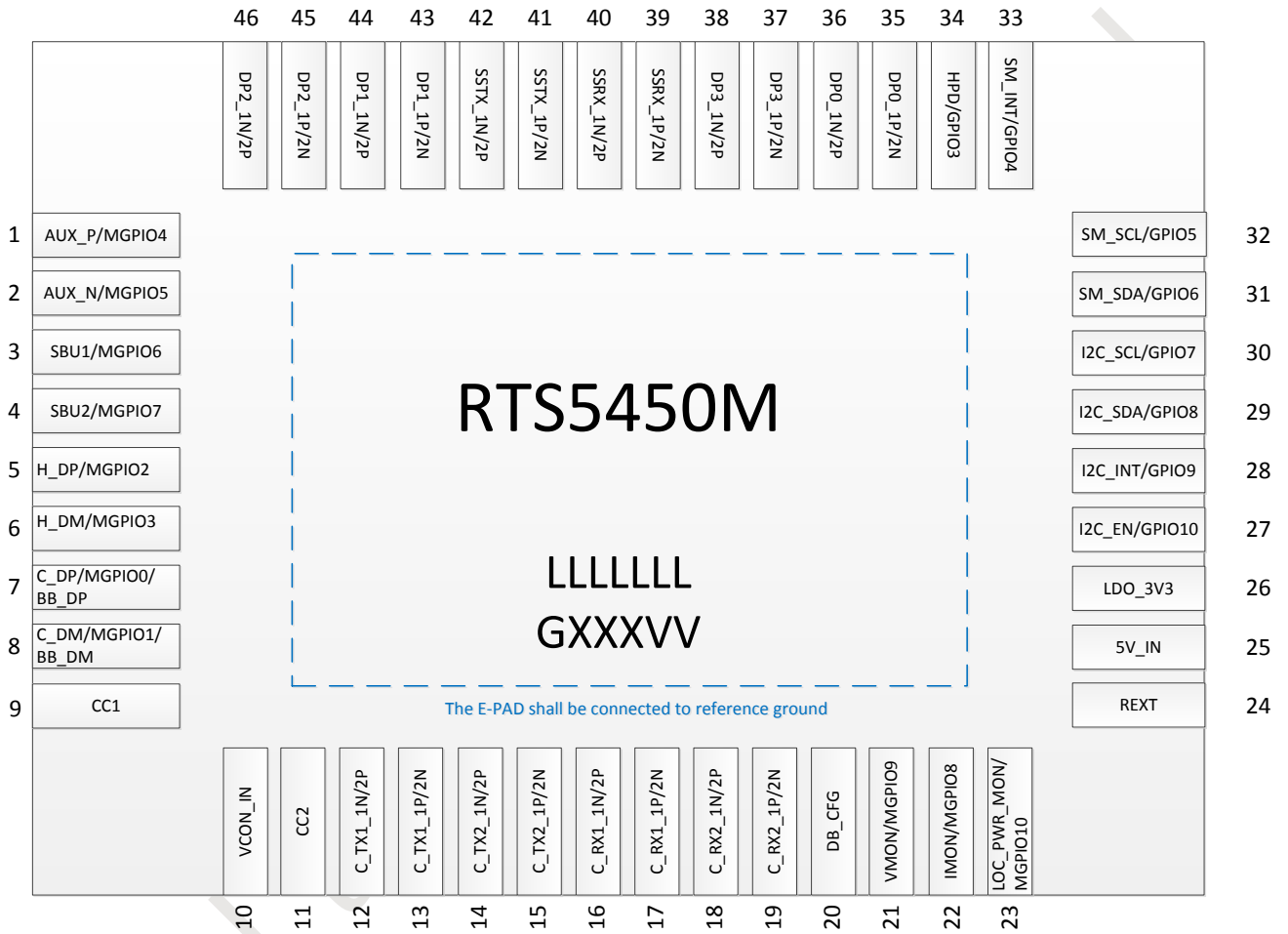


Figure 5-1 RTS5450M Pinout (Top View)

The version number is shown in the location marked 'VV' and G means Green Package

5.2 Pin Descriptions

Pin Name	Pin No.	I/O Type	Description
Power supply			
5V_IN	25	Power	Power input of internal 5V to 3.3V LDO. A MLCC with at least 10uF (X5R) value should be placed next to this pin.
VCON_IN	10	Power	Power input of internal VCONN switch. A MLCC with at least 10uF (X5R) value should be placed next to this pin.
LDO_3V3	26	Power	Power output of internal 5V to 3.3V LDO. A MLCC with at least 4.7uF (X5R) value should be placed next to this pin.
E-PAD	-	GND	The bottom of the package has a thermal pad. The pad shall be connected to the reference ground
Type-C Port Side Pins⁽¹⁾			
CC1 CC2	9, 11	Analog I/O	Type-C configuration channel
C_DP/MGPIO0/ BB_DP	7	Combined I/O	High speed MUX I/O connected to Type-C port D+/-. This pin can also be configured as digital GPIO via F/W in some applications. This pin can be configured as DP/DM of billboard device as well.
C_DM/MGPIO1/ BB_DM	8		
C_TX1_1P/2N C_TX1_1N/2P	13 12	Analog I/O	10Gbps MUX I/O connected to Type-C port TX1+/-
C_RX1_1P/2N C_RX1_1N/2P	17 16	Analog I/O	10Gbps MUX I/O connected to Type-C port RX1+/-
C_TX2_1P/2N C_TX2_1N/2P	15 14	Analog I/O	10Gbps MUX I/O connected to Type-C port TX2+/-
C_RX2_1P/2N C_RX2_1N/2P	19 18	Analog I/O	10Gbps MUX I/O connected to Type-C port RX2+/-
SBU1/MGPIO6 SBU2/MGPIO7	3 4	Combined I/O	Low speed MUX I/O connected to Type-C Port SBU1/2. This pin can also be configured as digital GPIO via F/W in some applications.

Pin Descriptions (continued)

Pin Name	Pin No.	I/O Type	Description
10Gbps MUX System Side Pins⁽¹⁾			
SSTX_1P/2N SSTX_1N/2P	41, 42	Analog I/O	10Gbps MUX I/O connected to system side USB3.X SSTX.
SSRX_1P/2N SSRX_1N/2P	39, 40	Analog I/O	10Gbps MUX I/O connected to system side USB3.X SSRX.
DP0_1P/2N DP0_1N/2P	35, 36	Analog I/O	10Gbps MUX I/O connected to system side one lane of alternate mode (e.g. DisplayPort).
DP1_1P/2N DP1_1N/2P	43, 44	Analog I/O	10Gbps MUX I/O connected to system side one lane of alternate mode (e.g. DisplayPort).
DP2_1P/2N DP2_1N/2P	45, 46	Analog I/O	10Gbps MUX I/O connected to system side one lane of alternate mode (e.g. DisplayPort).
DP3_1P/2N DP3_1N/2P	37, 38	Analog I/O	10Gbps MUX I/O connected to system side one lane of alternate mode (e.g. DisplayPort).
High Speed MUX System Side Pins			
H_DP/MGPIO2 H_DM/MGPIO3	5, 6	Combined I/O	High speed MUX I/O usually connected to USB2.0 host/device. These pins can also be configured as digital GPIOs via F/W in some applications.
Low Speed MUX System Side Pins			
AUX_P/MGPIO4 AUX_N/MGPIO5	1, 2	Combined I/O	Low Speed MUX I/O connected to system side DisplayPort AUX channel. These pins can also be configured as digital GPIOs via F/W in some applications.
I2C Master Interface			
I2C_SCL/GPIO7	30	5V Digital I/O	General Purpose I/O. Default configured as I2C master clock via F/W.
I2C_SDA/GPIO8	29	5V Digital I/O	General Purpose I/O. Default configured as I2C master data via F/W.
I2C_INT/GPIO9	28	5V Digital I/O	General Purpose I/O. Default configured as the INT pin to respond to the interrupt of the slave.
I2C_EN/GPIO10	27	5V Digital I/O	General Purpose I/O. Default configured as the enable pin to control the slave.
SMBUS/I2C Slave Interface			
SM_SCL/GPIO5	32	5V Digital I/O	General Purpose I/O. Default configured as SMBUS slave clock via F/W. Can also be configured as I2C master/slave clock.
SM_SDA/GPIO6	31	5V Digital I/O	General Purpose I/O. Default configured as SMBUS slave data via F/W. Can also be configured as I2C master/slave data.
SM_INT/GPIO4	33	5V Digital I/O	General Purpose I/O. Default configured as the INT pin to generate interrupt to the master.

Pin Descriptions (continued)

Pin Name	Pin No.	I/O Type	Description
ADC Input Channels			
VMON/MGPIO9	21	Combined I/O	Used to monitor VBUS voltage. Divide the VBUS voltage down to ADC full-scale input of 1.2V. Then connect the divided voltage to this pin. This pin can also be configured as digital GPIOs via F/W in some applications.
IMON/MGPIO8	22	Combined I/O	Used to monitor VBUS current. Usually use the current sense amplifier to amplify the voltage of the VBUS current sense resistor to the ADC full-scale input of 1.2V. This pin can also be configured as digital GPIOs via F/W in some applications.
LOC_PWR_MON/MGPIO10	23	Combined I/O	Used to monitor local power voltage. Divide the VBUS voltage down to ADC full-scale input of 1.2V. Then connect the divided voltage to this pin. This pin can also be configured as digital GPIOs via F/W in some applications.
Other MISC			
REXT	24	Analog Output	Connect an external resistor (6.2K \pm 1%) to the Reference GND
DB_CFG	20	Analog Input	Dead battery function configuration pin. Connect this pin to GND to disable dead battery 'Rd'. Leave this pin floating to enable dead battery 'Rd'
HPD/GPIO3	34	5V Digital I/O	DisplayPort HPD pin. This pin can also be configured as digital GPIO via F/W in some applications.

(1) The polarity of 10Gbps MUX I/Os can be swapped together depends on layout convenience.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Units
Power supply voltage ⁽¹⁾	V_{5V_IN}		-0.3 to 6	V
	V_{LDO_3V3}		-0.3 to 3.6	V
Input voltage ⁽¹⁾	V_I	5V Digital I/O	-0.3 to 3.6 ⁽⁴⁾	V
	V_{I_SW}	10Gbps MUX	-0.3 to 1.75	V
		High speed MUX	-0.3 to 3.6	V
		Low speed MUX	-0.3 to 3.6	V
		ADC analog input	-0.3 to 3.6	V
5V Digital IO Output current ⁽²⁾	I_O	4mA Type Buff ⁽³⁾	6	mA
		8mA Type Buff ⁽³⁾	12	mA
MUX ON-state switch current ⁽²⁾	I_{SW}	10Gbps MUX	10	mA
		High speed MUX	20	mA
		Low speed MUX	20	mA
Storage temperature	T_{stg}		-20 to +80	°C
Latch up Current			±400	mA
Electrostatic Discharge Voltage (HBM)			2	KV

- (1) This parameter indicates voltage exceeding which damage or reduced reliability will occur when power is applied to the IO.
- (2) This parameter indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.
- (3) The output driving strength of all output is 4mA by default, which can be configured as 8mA by firmware through executing external codes.
- (4) When IC is powered on, the DC tolerance of 5V Digital I/O can reach 6V.

6.2 Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Power supply voltage	$V_{5V_IN}^{(1)}$		4.0	5	5.5	V
	$V_{LDO_3V3}^{(2)}$		3.14	3.3	3.46	V
Available current of 3.3V power supply for external circuits ⁽³⁾		$V_{5V_IN}=5V$			20	mA
VCONN switch input voltage range	V_{VCONN_IN}		4.95		5.5	V
10Gbps MUX common-mode voltage	V_{CM_SS}		0		1.4	V
10Gbps MUX differential voltage	V_{DF_SS}		0		1.4	Vpp
High speed MUX I/O voltage range	V_{L_HS}		0		3.6	V
Low speed MUX I/O voltage range	V_{L_LS}		0		3.6	V
Operating ambient temperature	T_A		0		+70	°C
Absolute maximum junction temperature	T_J		0		+125	°C

- (1) 5V_IN power pin should be supplied with the power of voltage range in the table when using on-chip LDO.
- (2) 5V_IN and LDO_3V3 power pin should be shorted together and supplied with the power of the voltage range in the table without using on-chip LDO.
- (3) Load current of external circuits shouldn't exceed the max value when using on-chip LDO. It is recommended that the external circuits are limited to LEDs.

6.3 DC Characteristics

The following specifications apply when power supply voltages are within the recommended operating ranges in section 6.2.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
5V Digital I/O						
Input leakage current ⁽¹⁾	I_I	$V_I = V_{5V_IN}$ or GND	-2.5		2.5	μA
Input High Voltage ⁽²⁾	V_{IH}	Input 3.3V mode	2.0			V
		Input 1.8V mode	1.2			V
Input Low Voltage ⁽²⁾	V_{IL}	Input 3.3V mode			0.8	V
		Input 1.8V mode			0.6	V
Output High Voltage ⁽³⁾	V_{OH}	IO source current = 4mA	2.4			V
Output Low Voltage ⁽³⁾	V_{OL}	IO sink current = 4mA			0.4	V
Input pin Capacitance	C_{in}			5		pF
Combined I/O⁽⁴⁾						
Input leakage current ⁽¹⁾	I_I	$V_I = V_{LDO_3V3}$ or GND	-4		4	μA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	IO source current = 4mA	2.7			V
Output Low Voltage	V_{OL}	IO sink current = 4mA			0.3	V
ADC Analog Input						
ENOB				9.5		Bits
Full-scale input span			0		1.2	V
Input capacitance				5		pF
MUX resistance				50		Ω
No missing codes			10			Bits
Integral linearity			-1.4		1.2	LSBs
Differential linearity			-0.6		0.7	LSBs
Offset error			-0.5		+0.5	LSBs
Gain error			-0.5		+0.5	%

DC Characteristics (continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
10Gbps MUX						
Switch ON resistance	R_{on}	$V_{5V_IN}=5V$, $V_{CM} = 0-1.4V$, $I_o=-8mA$		8	9	Ω
Switch ON resistance flatness	$R_{on(Flat)}$	$R_{ON_SS(max)}$. $R_{ON_SS(min)}$ value over $V_{CM_SS}= 0-1.4V$ range			1.5	Ω
High speed MUX						
Switch ON resistance	R_{on}	$V_{LHS}= 2V$, $I_o=-8mA$		12		Ω
Switch ON resistance flatness	$R_{on(Flat)}$	$R_{ON_HS(max)}$. $R_{ON_HS(min)}$ value over $V_{LHS}=0-3.3V$ range		11		Ω
SBU Low Speed MUX						
Switch ON resistance	R_{on}	$V_{LLS}=1.6V$, $I_o=-8mA$		10		Ω
Switch ON resistance flatness	$R_{on(Flat)}$	$R_{ON_LS (max)}$. $R_{ON_LS(min)}$ value over $V_{LLS}=0-3.3V$ range		4.8		Ω
VCONN Power Switch						
Switch ON resistance	R_{on_vcon}	$V_{IN_VCONN}=5 - 5.5V$. Switch on without over current condition.		0.4		Ω
Switch OFF leakage	I_{off_vcon}	$V_{IN_VCONN}=5 - 5.5V$. Switch off. V_{out} short GND.			10	nA

- (1) This parameter indicates the current that flows through the I/O which output Hi-z when power supply voltage is supplied to it.
- (2) 5V digital IO except HPD default input high/low voltage level is 1.8V mode, but can be configured as 3.3V mode via F/W. HPD is input high/low voltage level is 3.3V mode
- (3) Default IO driving strength is 4mA, but can be configured as 8mA via F/W.
- (4) DC characteristic of combined I/O when used as GPIO.

6.4 AC Characteristics

6.4.1 10Gbps MUX Dynamic Characteristics

Under recommended operating conditions, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
differential insertion loss	DIL	@100MHz		-1.2		dB
		@2.5GHz		-2.0		
		@5GHz		-3.0		
differential return loss	DRL	@100MHz		-17		dB
		@2.5GHz		-14		
		@5GHz		-11		
differential near-end crosstalk	XTALK	@100MHz		-60		dB
		@2.5GHz		-37		
		@5GHz		-43		
Differential off isolation	DOI	@100MHz		-77		dB
		@2.5GHz		-53		
		@5GHz		-43		
-3dB bandwidth	BW			5		GHz
on-state input/output capacitance	$C_{io(on)}$			1.2		pF
propagation delay	t_{PD}				TBD	ns
intra-pair skew	$t_{sk(dif)}$				TBD	ns
inter-pair skew	t_{sk}				TBD	ns

Note:

In order to ensure the USB3.1 Gen2 10Gbps signal integrity, the external 10Gbps redriver or retimer chip is highly recommended to be used with RTS5450M for USB3.1 Gen2 applications. Please refer to the related reference schematics.

6.4.2 High speed MUX Dynamic Characteristics

Under recommended operating conditions, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crosstalk	XTALK	RL = 50 Ω , f = 240 MHz		-40		dB
off isolation	OIS	RL = 50 Ω , f = 240 MHz		-40		dB
-3dB bandwidth	BW	RL = 50 Ω , CL = 5 pF		1		GHz
on-state input/output capacitance	C _{io(on)}	Switch on		5		pF
off-state input/output capacitance	C _{io(off)}	Switch off		5		pF
propagation delay	t _{PD}	RL = 50 Ω , CL = 5 pF		0.2		ns
intra-pair skew	t _{sk(dif)}	RL = 50 Ω , CL = 5 pF		2.2		ps

6.4.3 SBU Low Speed MUX Dynamic Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crosstalk	XTALK			-40		dB
off isolation	OIS			-40		dB
-3dB bandwidth	BW			0.5		GHz
on-state input/output capacitance	C _{io(on)}			5		pF
off-state input/output capacitance	C _{io(off)}			5		pF
propagation delay	t _{PD}			0.4		ns
intra-pair skew	t _{sk(dif)}			1.7		ps

6.5 Power Consumption

The following consumption value applies upon the typical condition in 5V or 3.3V mode.

TA= 25°C.

Parameter		Conditions	Min.	Typ.	Max.	Units
5V or	Sleep	Type-C is disconnected		0.5		mA
3.3V	Normal	Power consumption mean value when Type-C is connected.		3.5		mA
total	Operation					
	Full Operation	Peak power consumption when Type-C is connected. Full Speed billboard is enabled.		27		mA
		Peak power consumption when Type-C is connected. Billboard is disabled.		21		mA

7. System Level Block Diagram

7.1 Docking/Monitor Application

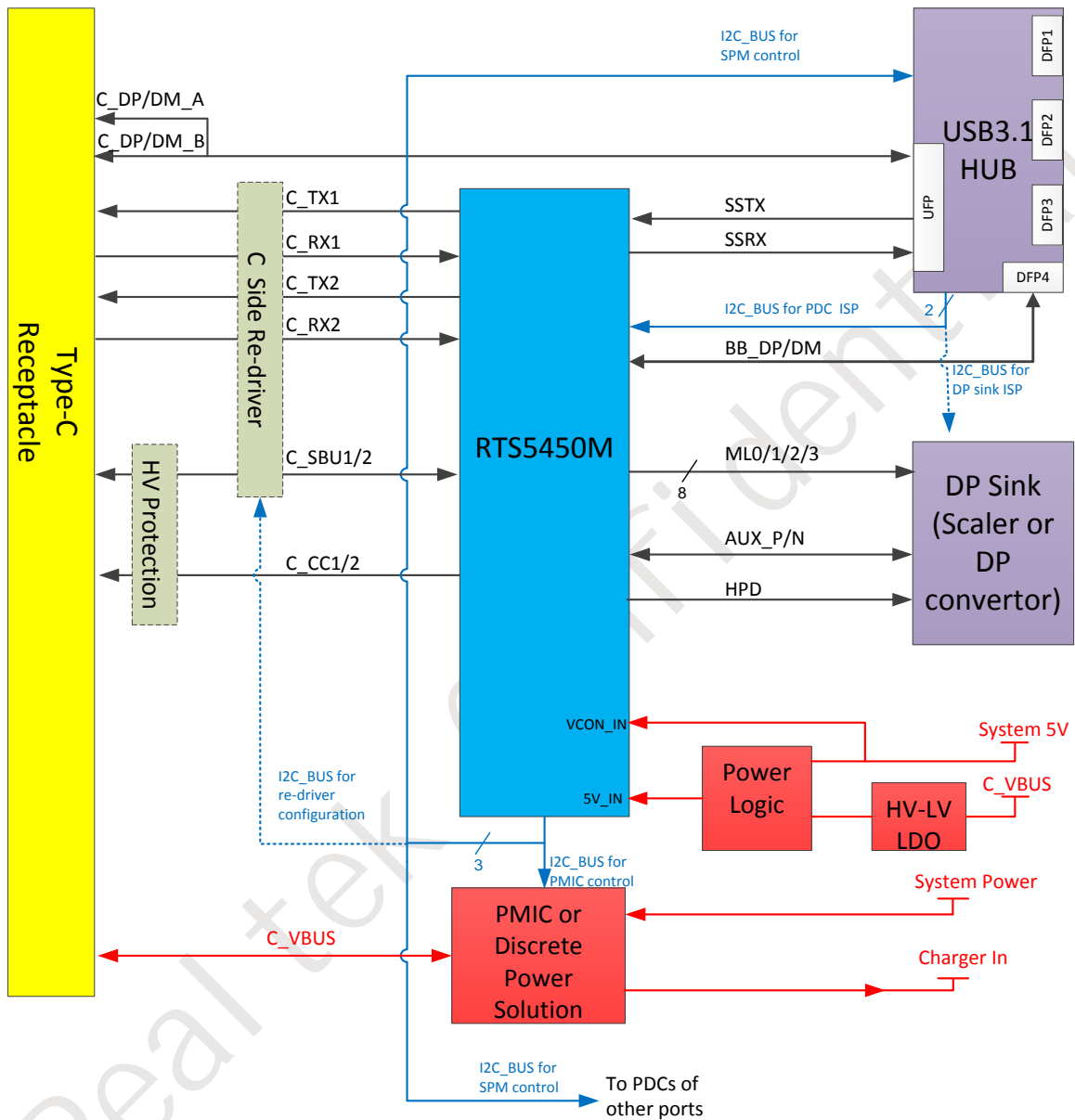


Figure 7-2 Docking/Monitor Application Block Diagram

Note:

1. Some discrete components as ac couple capacitors, pull resistors, etc. are not painted on this diagram. Please refer to the reference schematic for detail information.
2. The component or net with dotted line is not mandatory. Refer to related design documents as layout guide, application note, etc. for more information.
3. In some monitor application, I2C/SMBUS interconnection is more complicated for DisplayPort 2lane/4lane switch policy. Please refer to the turnkey solution reference schematic for detail information

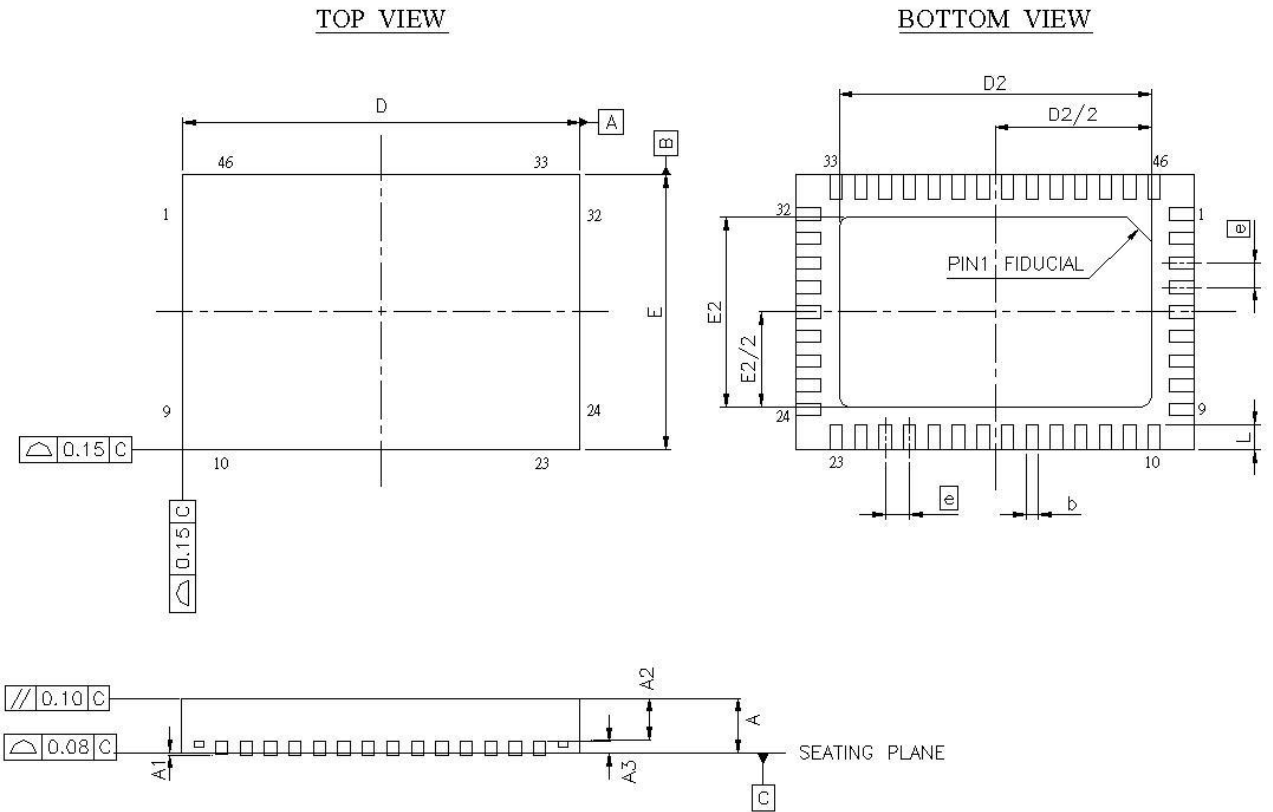
8. I2C/SMBUS interface

8.1 Overview

RTS5450M has integrated SMBUS/I2C slave and I2C Master to implement various functions. This contributes to flexibility and simplicity of adding Type-C USB Power Delivery to any architecture. See more details in the table below.

Role	Function Support	Description
Slave	Vendor Setting	RTS5450M can be configured via SMBUS/I2C before the any function work. Most of the functions can be customized, such as Type-C/Power delivery/Alt mode/USB billboard device.
Salve	Power Delivery System Control	RTS5450M can be controlled via SMBUS/I2C, to achieve all the Power Delivery related functions, such as Cable detection/Power Negotiation/Power Swap/Data Swap/VCONN Swap.
Salve	Type-C Alt Mode system control	The detail VDM flow (including SOP and SOP' packet) can be controlled via SMBUS/I2C to achieve various Type-C Alternate Mode.
Slave	Firmware ISP	RTS5450M has MCU inside and supports external SPI flash mode, in which firmware can be updated via F/W. This function can benefit to the flexibility of various applications.
Master	According to Application	RTS5450M supports I2C master mode for various application.

9. QFN-46 Package Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A ₁	0.00	0.035	0.05	0.000	0.001	0.002
A ₂	0.55	0.65	0.80	0.022	0.026	0.032
A ₃	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.50BSC			0.256BSC		
D2	4.85	5.1	5.35	0.191	0.201	0.211
E	4.5BSC			0.177BSC		
E2	2.85	3.1	3.35	0.112	0.122	0.132
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.

10. Ordering Information

Part Number	Package	Status
RTS5450M-GR	QFN-46 Green package	

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