High Efficiency 8A Synchronous Boost Convertor

General Description

The LP6253H is a synchronous current mode boost DC-DC converter. Its PWM circuitry with built-in 8A current power MOSFET makes this converter highly efficient. Selectable high switching frequency allows faster loop response and easy filtering with a low noise output. The non-inverting input its error amplifier is connected to an internal 1.21V precision reference voltage. Current mode control and internal compensation network make it easy and flexible to stabilize the system.

Features

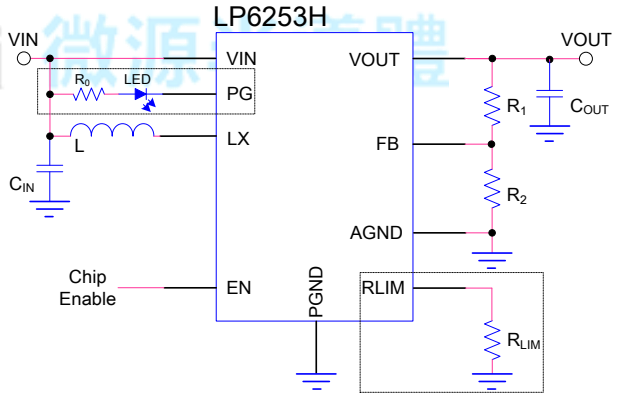
- Up to 96% high efficiency
- Output to Input Disconnect at Shutdown Mode
- High switch on current: 8A
- Output Voltage Up to 5.0V/2.1A with V_{IN}=3V
- Only use small inductor: 1uH
- Programmable output current limit: 0.1A~2.5A
- Power good indication function(open drain)
- Internal Compensation
- 650KHz fixed frequency switching
- Shutdown current:<1uA
- Available in ESOP8 & TDFN-10 Package

Order Information

LP6252H □ □ □ – □ □

- Output type
  - Default: Adjustable
  - 51: 5.1V
- F: Pb-Free
- Package Type
  - SP: ESOP8
  - QV: TDFN-10

Typical Application Circuit



Note: C_{OUT} must be as close as possible to the PGND and VOUT pins.

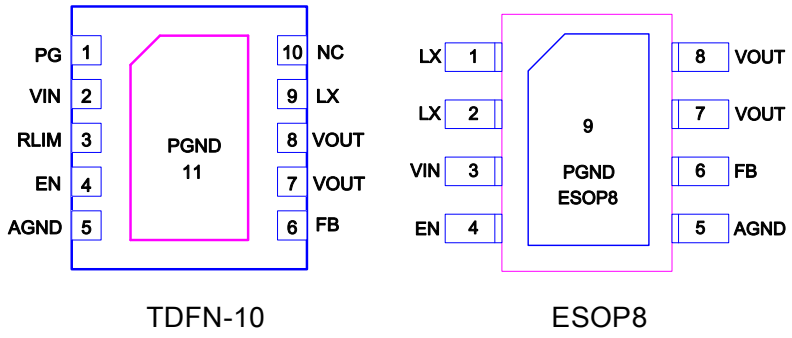
Applications

- Battery products
- Host Products
- Panel

Marking Information

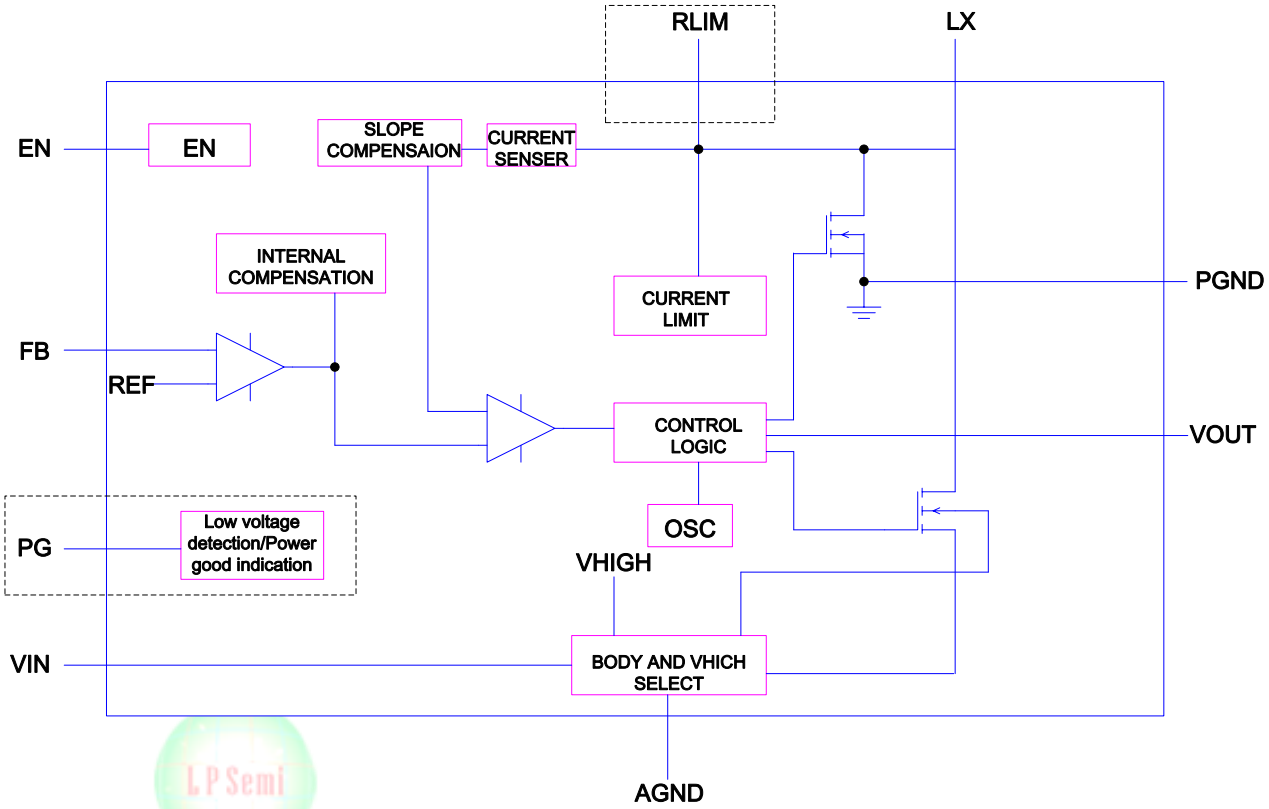
Device	Marking	Package	Shipping
LP6253HSPF	LPS LP6253H YWX	ESOP8	2.5K/REEL
LP6253HQVF		TDFN-10	3K/REEL
Y:Production year W:Production period X:Production batch			

Functional Pin Description

Package Type	Pin Configurations
TDFN-10 / ESOP8	 TDFN-10 ESOP8

Pin		Name	Description
TDFN-10	ESOP8		
1		PG	Power good indication.
2	3	VIN	Voltage input pin.
3		RLIM	Connect a resistor to GND for limiting the output current.
4	4	EN	Chip enable pin.
5	5	AGND	Internal Analog Ground pin. Connect this pin to PGND.
6	6	FB	Feedback pin. The reference voltage is 1.21V.
7,8	7,8	VOUT	Output pin.
9	1,2	LX	Switching pin.
10		NC	No connection.
11	9	PGND	Power Ground pin.

Function Diagram



Absolute Maximum Ratings Note 1

- ✧ Input and VOUT to GND ---------- 6V
- ✧ Other Pin to GND (FB,EN,LX) ---------- 6V
- ✧ Maximum Junction Temperature ---------- 150℃
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
- ✧ Operating Ambient Temperature Range ---------- -40℃ to 85℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (ESOP8, PD,T_A=25℃) ---------- 2W
- ✧ Thermal Resistance (ESOP8, J_A) ---------- 46℃/W
- ✧ Maximum Power Dissipation (TDFN-10, PD,T_A=25℃) ---------- 1.5W
- ✧ Thermal Resistance (TDFN-10, J_A) ---------- 68℃/W

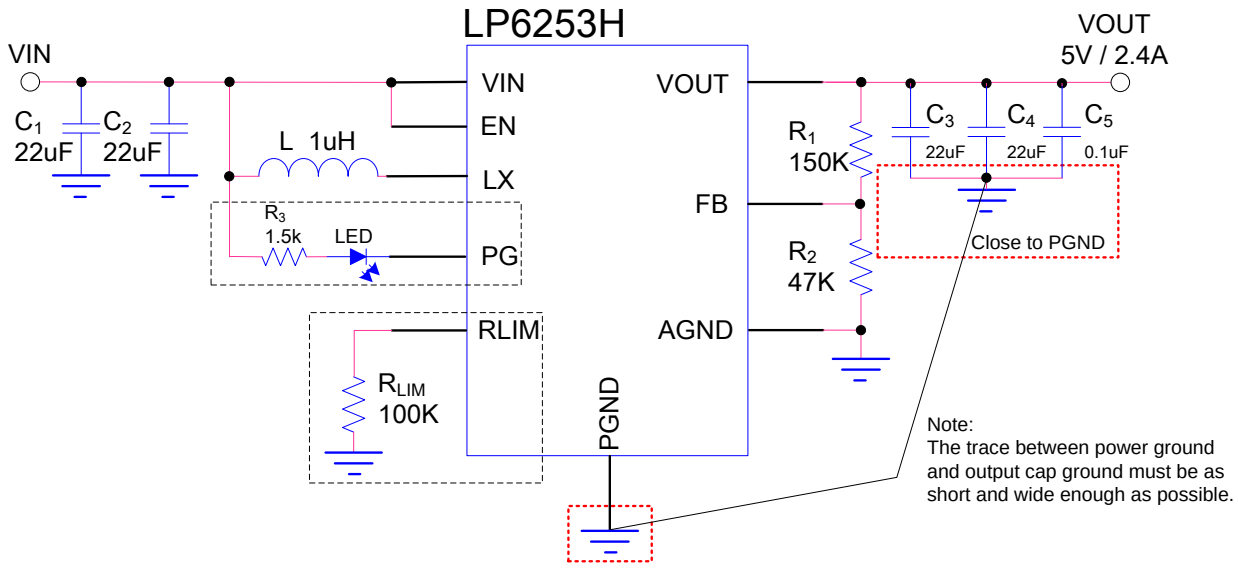
ESD Susceptibility

- ✧ HBM(Human Body Mode) ---------- 2KV
- ✧ MM(Machine Mode) ---------- 200V

Electrical Characteristics

(V_{IN}=3.5V, V_{OUT}=5V, C_{IN}=22uF×2, C_{OUT}=22uF×2, L=1uH)

Parameter	Condition	Min	Typ.	Max	Units
Supply Voltage		2.5		5.5	V
Output Voltage Range		2.8		5.5	V
Under voltage lockout	V_{IN} rising	1.8	2	2.2	V
Supply Current(Shutdown)	V_{EN}= 0V		0.5	1	μA
Supply Current	V_{EN}= 3V		200		μA
Feedback Voltage		1.186	1.21	1.234	V
Feedback Input Current	V_{FB}=1.21V		0.1	1	μA
Switching Frequency			650		KHz
EN Input Low Voltage				0.4	V
EN Input High Voltage		1.4			V
High-side On Resistance	V_{OUT}=5V		55		mΩ
Low-side On Resistance	V_{OUT}=5V		55		mΩ
Switch Current Limit			8		A
Line regulation				0.6	%
Over temperature protection			150		℃
Over temperature hysteresis			20		℃



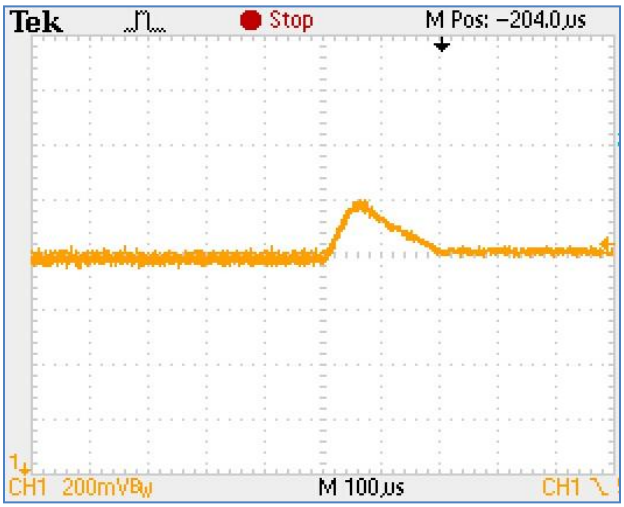
Typical Operating Characteristics

V_{IN}=3V, V_{OUT}=5V, I_{OUT}=2A

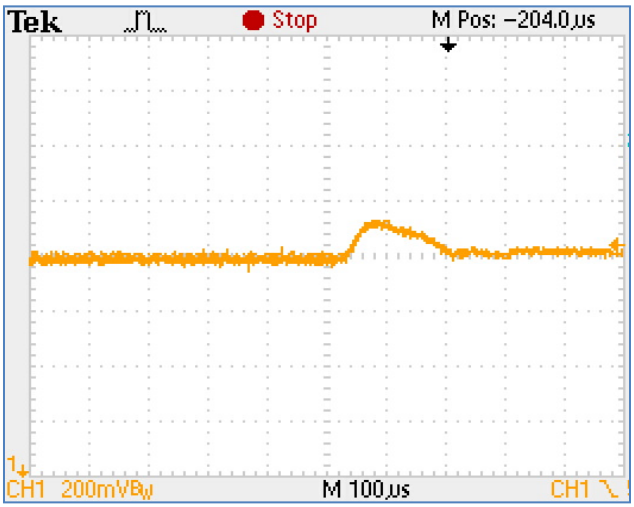
V_{IN}=3.7V, V_{OUT}=5V, I_{OUT}=2A

V_{IN}=3V, V_{OUT}=5V, I_{OUT}=1A

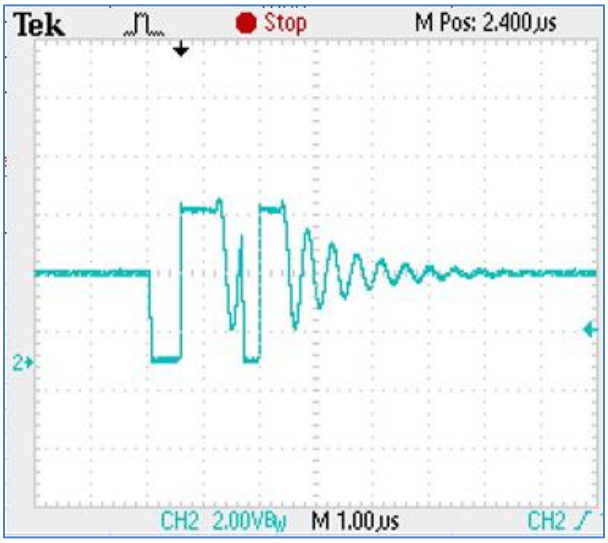
V_{IN}=3.7V, V_{OUT}=5V, I_{OUT}=1A



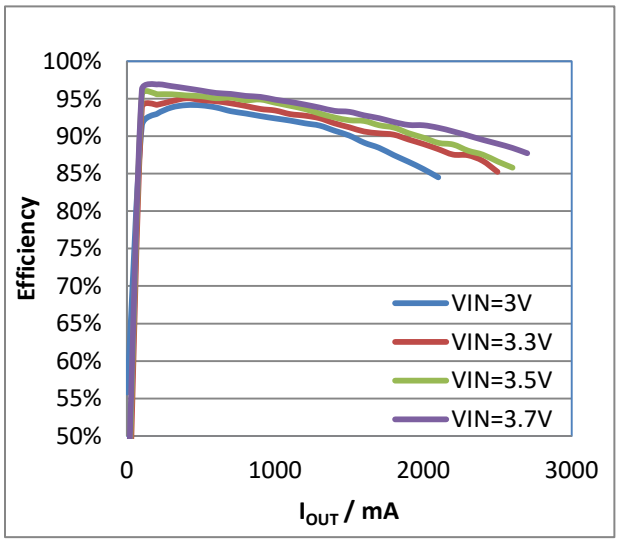
Output Unloading @ V_{IN}=3V, I_{OUT}=2A→0A



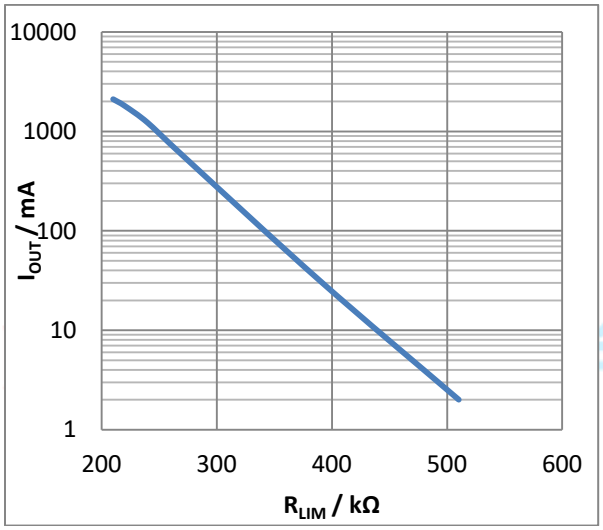
Output Unloading @ V_{IN}=3.7V, I_{OUT}=2A→0A



V_{IN}=3V, V_{OUT}=5V, I_{OUT}=0A



Efficiency VS. I_{OUT}



I_{OUT_Limit} VS. R_{LIM} for LP6253HQVF

Operation Information

The LP6253H uses a synchronous 650KHz fixed frequency, current-mode regulation architecture to regulate the output voltage. The LP6253H measures the output voltage through an external resistive voltage divider and compares that to the internal 1.21V reference to generate the error voltage to the inductor current to regulate the output voltage. The use of current-mode regulation improves transient response and control loop stability. The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 8A. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

The device integrates a high side N-channel and a low side N-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low $R_{DS(ON)}$ NMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to GND. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the back gate diode of the high-side NMOS is forward biased in shutdown and allows current flowing from the VIN to the VOUT. This device however uses a special circuit which takes the cathode of the back gate diode of the high-side NMOS and disconnects it from the source when the regulator is not enabled (EN=low). The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

Undervoltage Lockout

An under voltage lockout function prevents device start-up if the supply voltage on VIN is lower than approximately 2V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VIN drops below approximately 1.8V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 1.21V feedback voltage. Use a 10K resistor for R_2 of the voltage divider. Determine the high-side resistor R_1 by the equation:

$$V_{OUT} = (R_1 / R_2 + 1) \times V_{FB}$$

Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the LX node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the LX pin is induced. The integrated antiringing switch clamps this voltage to VIN and therefore dampens ringing.

Pre-Boost Current and Short Circuit Protect

Initially output voltage is lower than battery voltage, and the LP6253H enters pre-boost phase. During pre-boost phase, the internal NMOSFET turned OFF/ON and a constant current is provided from battery to output until the output voltage close to the battery voltage. The constant current is limited by internal controller. If the output short to ground, the LP6253H also limits the output current to avoid damage condition.

Inductor Selection

For a better efficiency in high switching frequency converter, the inductor selection has to use a proper core material such as ferrite core to reduce the core loss and choose low ESR wire to reduce copper loss. The most important point is to prevent the core saturated when handling the maximum peak current. Using a shielded inductor can minimize radiated noise in sensitive applications. The maximum peak inductor current is the maximum input current plus the half of inductor ripple current. The calculated peak current has to be smaller than the current limitation in the electrical characteristics. A typical setting of the inductor ripple current is 20% to 40% of the maximum input current. If the selection is 40%, the maximum peak inductor current is

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} I_{RIPPLE} = 1.2 \times I_{IN(MAX)}$$
$$= 1.2 \times \left[\frac{I_{OUT(MAX)} \times V_{OUT}}{\eta \times V_{IN(MIN)}} \right]$$

The minimum inductance value is derived from the following equation :

$$L = \frac{\eta \times V_{IN(MIN)}^2 \times [V_{OUT} - V_{IN(MIN)}]}{0.4 \times I_{OUT(MAX)} \times V_{OUT}^2 \times f_{OSC}}$$

Depending on the application, the recommended inductor value is between 1μH to 4.7μH.

Input Capacitor Selection

For better input bypassing, low-ESR ceramic capacitors are recommended for performance. A 10μF input capacitor is sufficient for most applications. A ceramic capacitor or a tantalum capacitor with a 100nF ceramic capacitor in parallel, placed close to the IC, is recommended. For a lower output power requirement application, this value can be decreased.

Output Capacitor Selection

For lower output voltage ripple, low-ESR ceramic capacitors are recommended. The output capacitor must be close to the VOUT and PGND pins. The tantalum capacitors can be used as well, but the ESR is bigger than ceramic capacitor. The output voltage ripple consists of two components: one is the pulsating output ripple current flows through the ESR, and the other is the capacitive ripple caused by charging and discharging. The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation:

$$V_{RIPPLE} = V_{RIPPLE\_ESR} + V_{RIPPLE\_C}$$
$$\cong I_{PEAK} \times R_{ESR} + \frac{I_{PEAK}}{C_{OUT}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} \times f_{OSC}} \right)$$

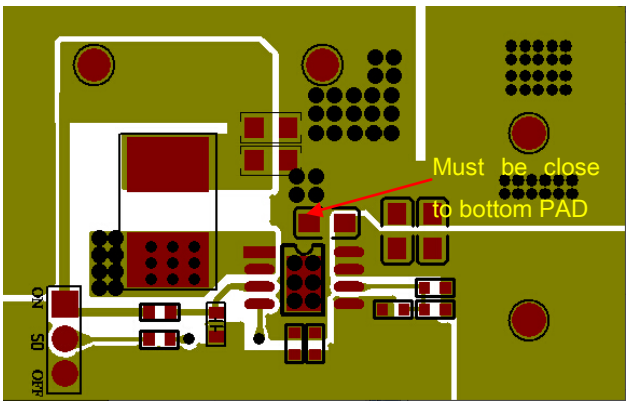
Layout Guideline

For high frequency switching power supplies, the PCB layout is important step in system application design. In order to let IC achieve good regulation, high efficiency and stability, it is strongly recommended the power components should be placed as close as possible. The set races should be wide and short. The feedback pin and then works of feedback and compensation should keep away from the power loops, and be shielded with a ground trace or plane to prevent noise coupling.

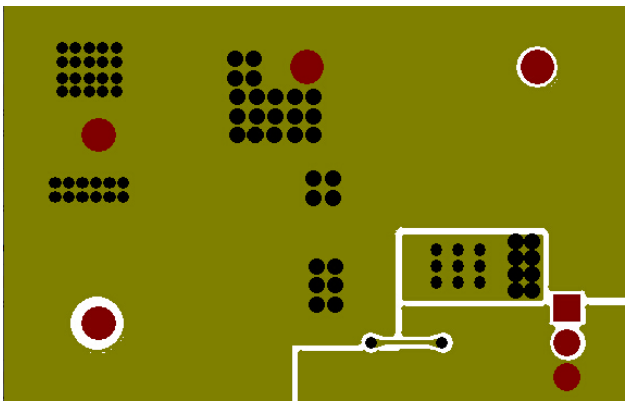
Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component. Three basic approaches for enhancing thermal performance are listed below:

1. Improving the power dissipation capability of the PCB design;
2. Improving the thermal coupling of the component to the PCB;
3. Introducing airflow in the system.

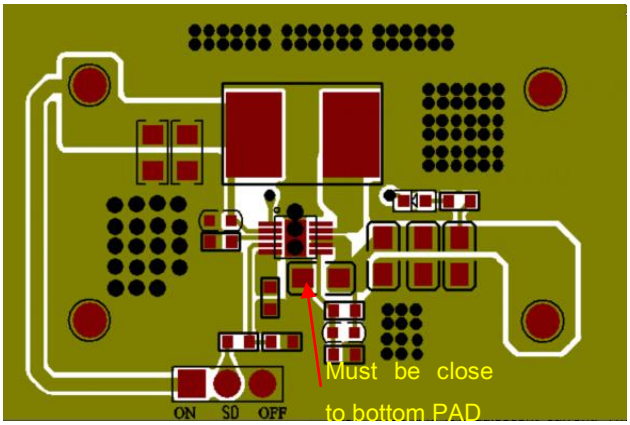
PCB Layout



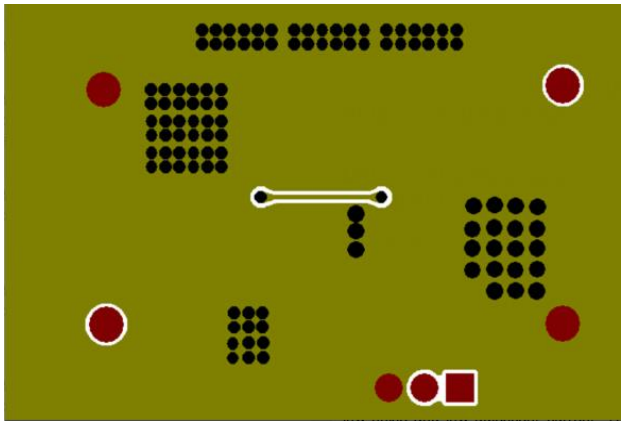
Top layer for LP6253HSPF Demo PCB Layout



Bottom layer for LP6253HSPF Demo PCB Layout



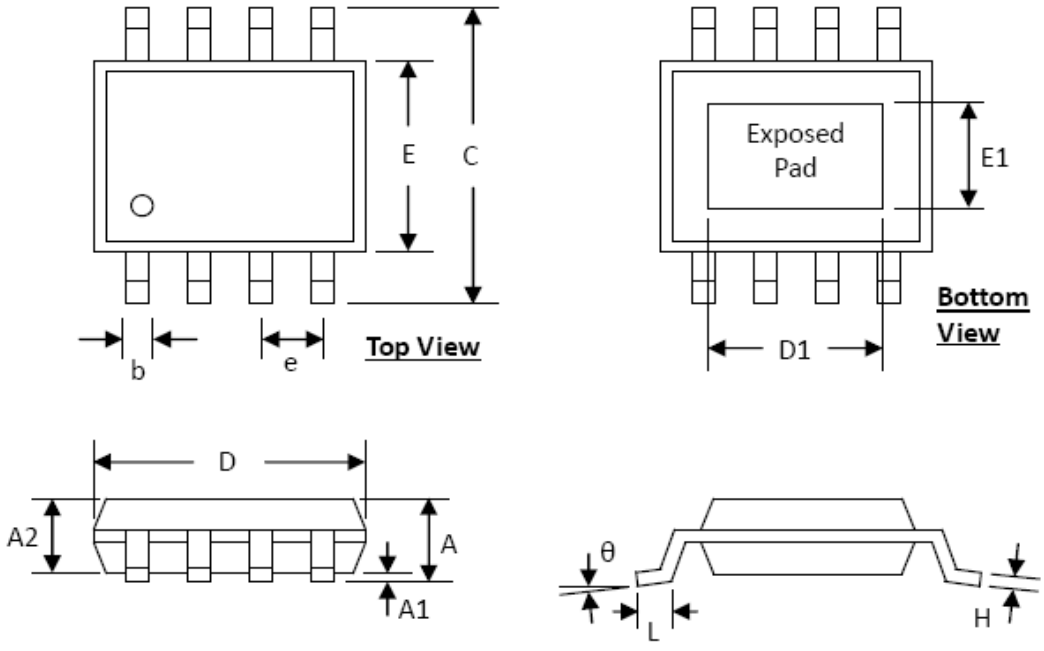
Top layer for LP6253HQVF Demo PCB Layout



Bottom layer for LP6253HQVF Demo PCB Layout

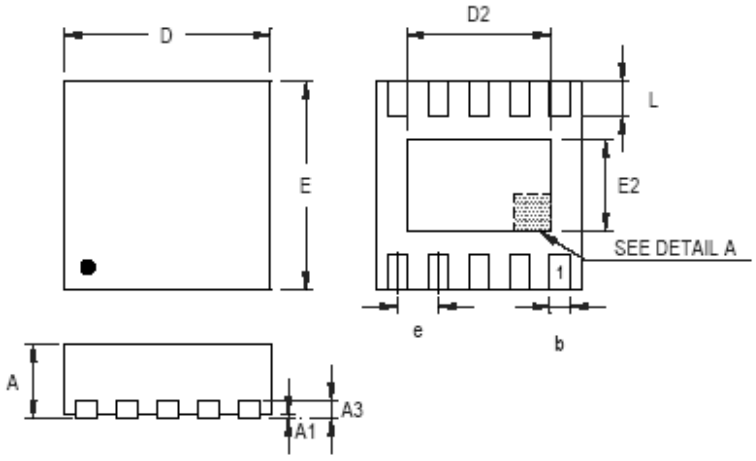
Packaging Information

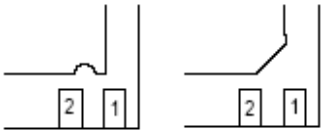
ESOP8



SYMBOLS	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A	1.30	1.70	0.051	0.067
A1	0.00	0.15	0.000	0.006
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
C	5.80	6.20	0.228	0.244
D	4.80	5.00	0.189	0.197
D1	3.15	3.45	0.124	0.136
E	3.80	4.00	0.150	0.157
E1	2.26	2.56	0.089	0.101
e	1.27 BSC		0.050 BSC	
H	0.19	0.25	0.0075	0.0098
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°

TDFN-10





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package