LITE-ON SEMICONDUCTOR CORP.

LSP5502

2A Synchronous Step Down DC/DC Converter

■ FEATURES

- 2A Output Current
- Wide 4.5V to 27V Operating Input Range
- Integrated 120mΩ Power MOSFET Switches
- Output Adjustable from 0.925V to 24V
- Up to 96% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 400KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- 8-Pin SOP Package

■ GENERAL DESCRIPTION

The LSP5502 is a monolithic synchronous buck regulator. The device integrates 120mΩ MOSFETS that provide 2A continuous load current over a wide operating input voltage of 4.5V to 27V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn on. In shutdown mode, the supply current drops below 1μA.

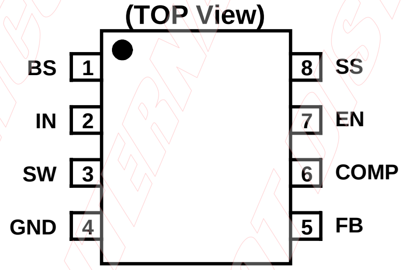
This device, available in an 8-pin SOP package, provides a very compact system solution with minimal reliance on external components.

■ TYPICAL APPLICATION

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

■ PIN ASSIGNMENT

SOP-8L
(TOP View)



■ PIN DESCRIPTION

Name	No.	Description
BS	1	Bootstrap. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 0.01uF capacitor between BS and SW.
IN	2	Input Supply. Bypass this pin to G with a low ESR capacitor. See Input Capacitor in the Application Information section.
SW	3	Switch Output. Connect this pin to the switching end of the inductor.
GND	4	Ground.
FB	5	Feedback Input. The voltage at this pin is regulated to 0.925V. Connect to the resistor divider between output and ground to set output voltage.
COMP	6	Compensation Pin. See Stability Compensation in the Application Information section.
EN	7	Enable Input. When higher than 2.5V, this pin turns the IC on. When lower than 1.3V, this pin turns the IC off. Output voltage is discharged when the IC is off. This pin should not be left open.
SS	8	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
IN Supply Voltage	-0.3 to 30	V
SW Voltage	-1 to V_{IN} + 0.3	V
BS Voltage	V_{SW} – 0.3 to V_{SW} + 6	V
EN, FB, COMP Voltage	-0.3 to 6	V
Continuous SW Current	Internally limited	A
Junction to Ambient Thermal Resistance (θ_{JA}) (Test on Approximately 3 in^2 Copper Area 1OZ copper FR4 board)	70	°C/W
Junction to Ambient Case Resistance (θ_{JC})	20	°C/W
Maximum Power Dissipation	0.76	W
Operating Temperature	-20 to 85	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	4.5	27	V
T_J	Operating Junction Temperature Range	-20	125	°C

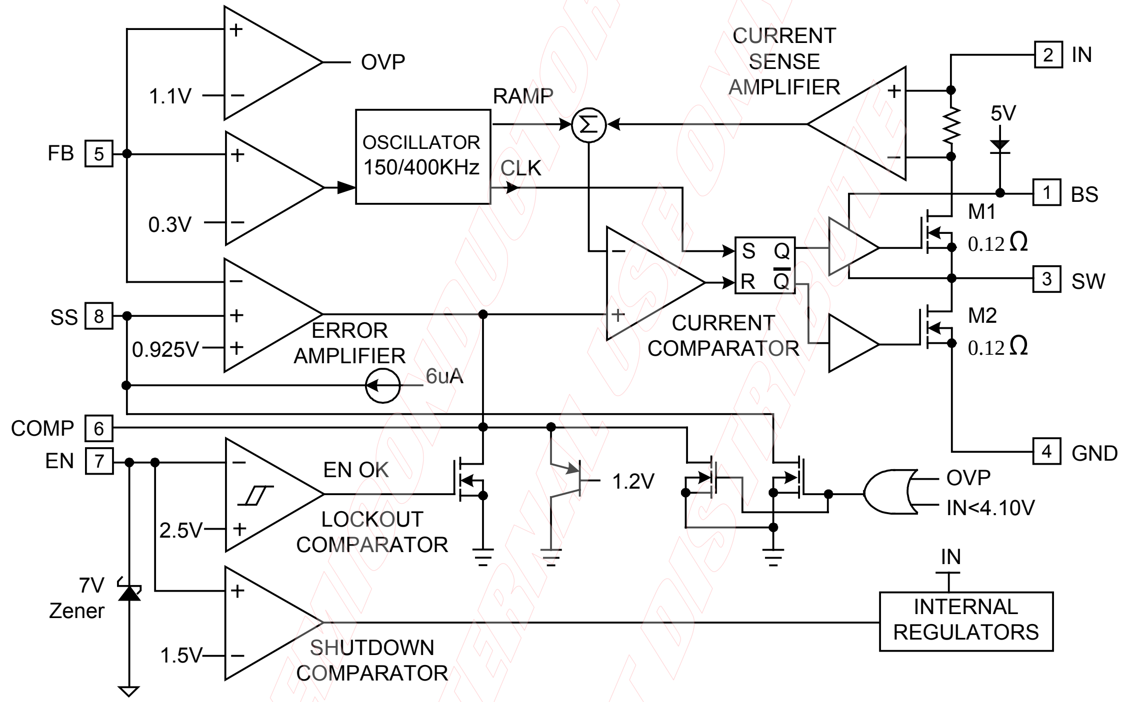
■ ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, TA= 25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Operating Voltage	V_{IN}	V_{OUT} = 1.0V, I_{LOAD} = 0A to 2A	4.5		27	V
Input Holdup Voltage		V_{OUT} = 1.0V, I_{LOAD} = 0A to 2A		4.5		V
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 20V	0.900	0.925	0.950	V
Feedback Overvoltage Threshold				1.1		V
High-Side Switch-On Resistance				120		mΩ
Low-Side Switch-On Resistance				120		mΩ
High-Side Switch Leakage		VEN = 0V, VSW = 0V		9	10	μA
Upper Switch Current Limit				3.5	4.0	A
Lower Switch Current Limit				0.9		A
COMP to Current Limit Transconductance	G_{COMP}			5.2		A/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ±10μA		800		μA/V
Error Amplifier DC Gain	A_{VEA}			480		V/V
Switching Frequency	f_{SW}		350	400	470	kHz
Short Circuit Switching Frequency		V_{FB} = 0		150		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.8V		90		%
Minimum On Time				220		nS
EN Shutdown Threshold Voltage		VEN Rising	1.1	1.3	1.5	V
EN Shutdown Threshold Voltage Hysterisis				200		mV
EN Lockout Threshold Voltage			2.2	2.5	2.7	V
EN Lockout Hysterisis				210		mV

Supply Current in Shutdown		V_{EN} = 0		0.3	3.0	μA
IC Supply Current in Operation		V_{EN} = 3V, V_{FB} = 1.0V		1.4	1.5	mA
Input UVLO Threshold Rising	UVLO	VEN Rising	3.80	4.05	4.40	V
Input UVLO Threshold Hysteresis				210		mV
Soft-start Current		VSS = 0V		6		μA
Soft-start Period		CSS = 0.1μF		15		mS
Thermal Shutdown Temperature		Hysteresis = 10°C		160		°C

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

The LSP5502 is a synchronous rectified, cur-rent-mode, step-down regulator. It regulates in-put voltages from 4.5V to 23V down to an out-put voltage as low as 0.925V, and supplies up to 2A of load current.

The LSP5502 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal trans-conductance error amplifier. The voltage at the COMP pin is compared to the switch current

measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the LSP5502 FB pin exceeds 20% of the nominal regulation voltage of 0.925V, the over volt-age comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

APPLICATION INFORMATION

Output Voltage Setting

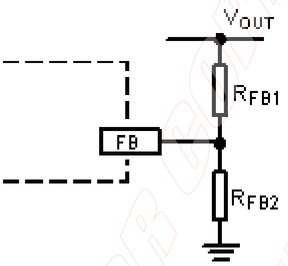


Figure1. Output Voltage Setting

Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors RFB1 and RFB2 based on the output voltage. Typically, use RFB2 ≈ 10kΩ and determine RFB1 from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.925V} - 1\right) \quad (1)$$

Table 1-Recommended Resistance Values

VOUT	RFB1	RFB2
1.0V	1.0kΩ	12kΩ
1.2V	3.0kΩ	10kΩ
1.8V	9.53kΩ	10kΩ
2.5V	16.9kΩ	10kΩ
3.3V	26.1kΩ	10kΩ
5V	44.2kΩ	10kΩ
12V	121kΩ	10kΩ

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on the ripple current requirement:

$$L = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUTMAX} K_{RIPPLE}} \quad (2)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{OUTMAX} is the maximum output current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum output current.

With this inductor value, the peak inductor current is $I_{OUT} \bullet (1 + K_{RIPPLE} / 2)$. Make sure that this peak inductor current is less that the 3A current limit. Finally, select the inductor core size so that it does not saturate at 3A. Typical inductor values for various output voltages are shown in Table 1.

V_{OUT}	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
L	4.7uH	4.7uH	6.8μH	6.8μH	10μH	10μH	15μH

Table 1. Typical Inductor Values

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.
The input capacitance needs to be higher than 10μF. The best choice is the ceramic type; however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1μF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{8 \cdot f_{SW}{}^{2} L C_{OUT}} \quad (3)$$

where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic capacitors. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

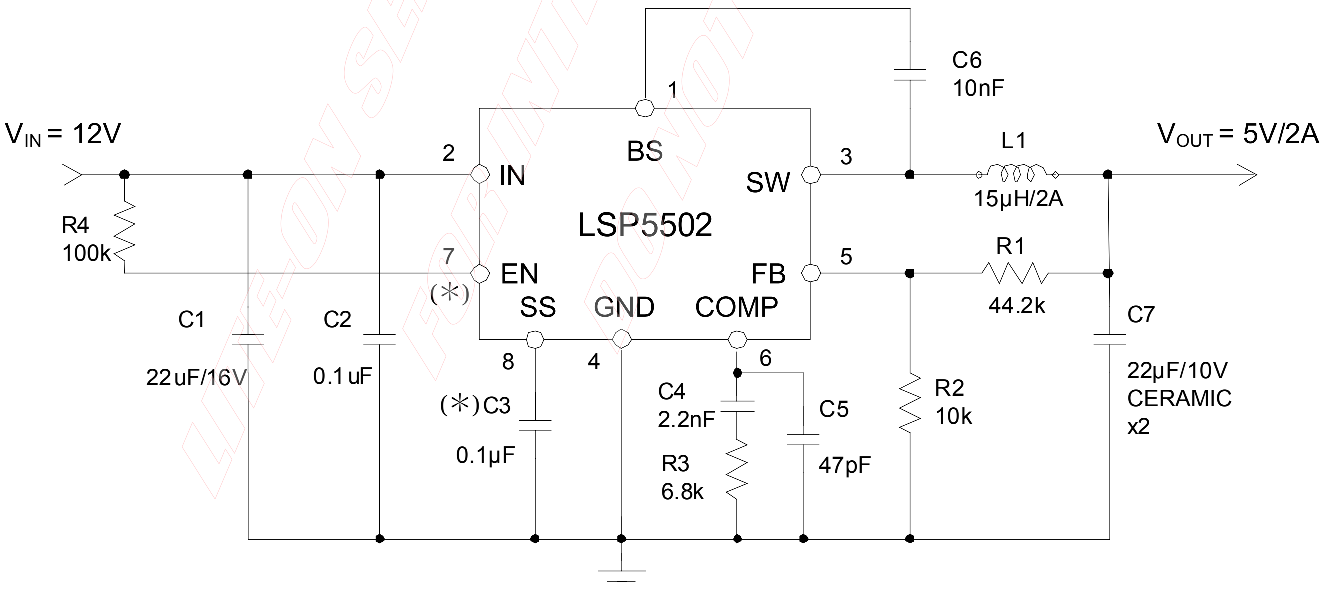
For ceramic output capacitors, typically choose a capacitance of about 22μF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Optional Schottky Diode

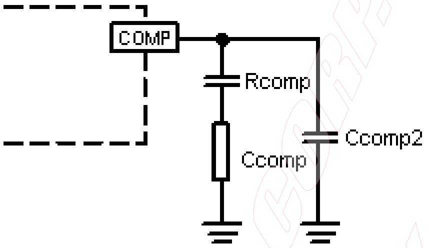
During the transition between high-side switch and low-side switch, the body diode of the low side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2-Diode Selection Guide

Part Number	Voltage/Current Rating	Vendor
B130	30V,1A	Lite-on Semiconductor Corp.
MBRS130	30V,1A	International Rectifier



Stability Compensation



C_{COMP2} is needed only for high ESR output capacitor

Figure 2. Stability Compensation

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 2. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.925V}{I_{OUT}} A_{VEA} G_{COMP} \quad (4)$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}} \quad (5)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \quad (6)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}} \quad (7)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \quad (8)$$

The following steps should be used to compensate the IC:

STEP1. Set the crossover frequency at 1/10 of the switching frequency via RCOMP:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \bullet 0.925V} \quad (9)$$

but limit RCOMP to 10kΩ maximum.

STEP2. Set the zero fZ1 at 1/4 of the crossover frequency. If RCOMP is less than 10kΩ, the equation for CCOMP is:

$$C_{COMP} = \frac{1.8 \times 10^{-5}}{R_{COMP}} \quad (F) \quad (10)$$

If RCOMP is limited to 10kΩ, then the actual crossover frequency is 10/ (VOUTCOUT). Therefore:

$$C_{COMP} = 1.2 \times 10^{-5} V_{OUT} C_{OUT} \quad (F) \quad (11)$$

STEP3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the crossover frequency, an additional compensation capacitor CCOMP2 is required. The condition for using CCOMP2 is:

$$R_{ESRCOUT} \geq Min\left(\frac{1.1 \times 10^{-6}}{C_{OUT}}, 0.012 \bullet V_{OUT}\right) \quad (\Omega) \quad (12)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}} \qquad (13)$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.
Table 3 shows some calculated results based on the compensation method above.

VOUT	COUT	RCOMP	CCOMP	CCOMP2
1.0V	22µF Ceramic	1.5kΩ	10nF	100pF
1.2V	22µF Ceramic	1.7kΩ	10nF	100pF
1.8V	22µF Ceramic	2.2kΩ	6.8nF	100pF
2.5V	22µF Ceramic	3.6kΩ	4.7nF	100pF
3.3V	22µF Ceramic	4.7kΩ	3.3nF	47pF
5V	22µF Ceramic	6.8kΩ	2.2nF	47pF
1.0V	47µF SP Cap	3.0kΩ	6.8nF	470pF
1.2V	47µF SP Cap	3.6kΩ	4.7nF	330pF
1.8V	47µF SP Cap	5.6kΩ	3.3nF	220pF
2.5V	47µF SP Cap	6.8kΩ	2.2nF	200pF
3.3V	47µF SP Cap	10kΩ	2.0nF	150pF
5V	47µF SP Cap	10kΩ	2.2nF	150pF
1.0V	470µF/6.3V/30mΩ	10kΩ	2.2nF	1nF
1.2V	470µF/6.3V/30mΩ	10kΩ	3.3nF	1nF
1.8V	470µF/6.3V/30mΩ	10kΩ	4.7nF	1nF
2.5V	470µF/6.3V/30mΩ	10kΩ	6.8nF	1nF
3.3V	470µF/6.3V/30mΩ	10kΩ	8.2nF	1nF
5V	470µF/10V/30mΩ	10kΩ	10nF	1nF

Table3. Typical Compensation for Different Output Voltages and Output Capacitors

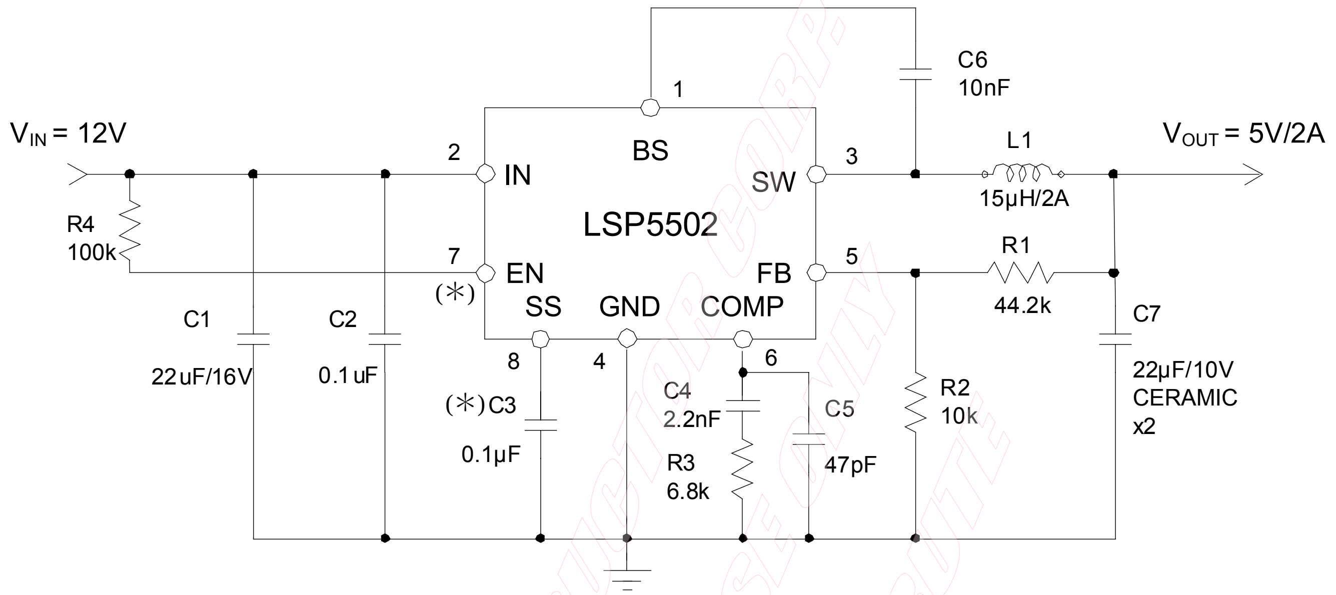


Figure 3 shows a sample LSP5502 application circuit generating 5V/2A output.

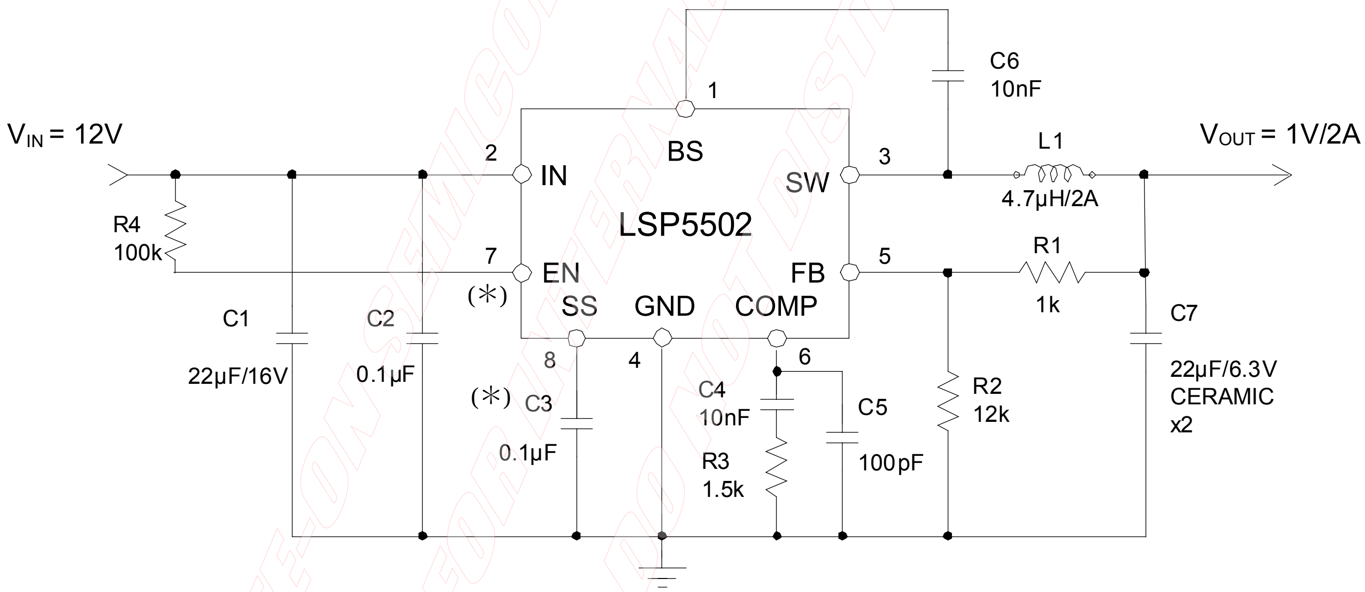
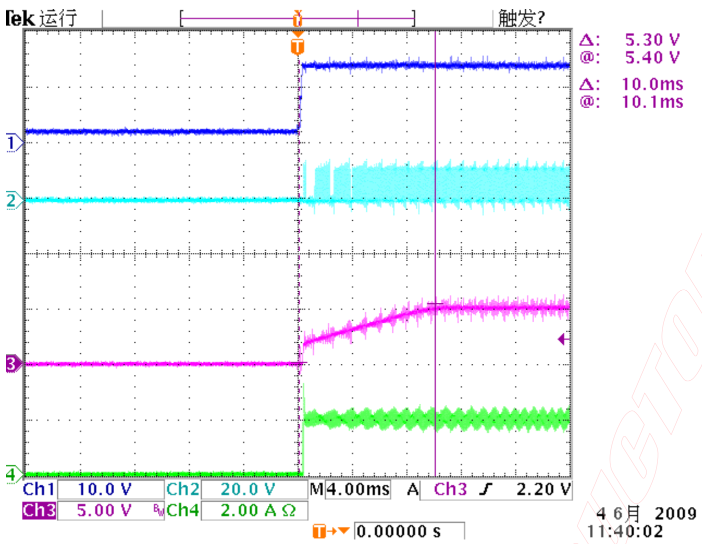


Figure 4 shows a sample LSP5502 application circuit generating 1.0V/2A output.

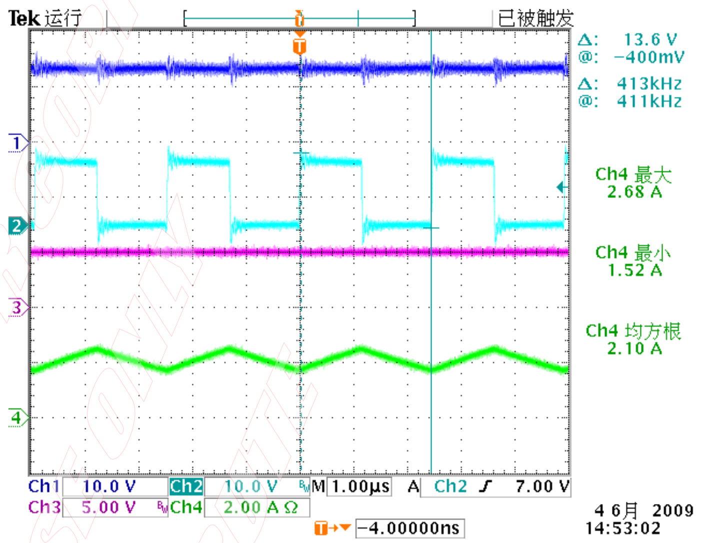
(*) To improve quality, it is recommended to choose a capacitance of about 1uF for C3.
For system security, it is recommended to place a 0.1uF capacitor from EN Pin to ground.

■ TYPICAL CHARACTERISTICS

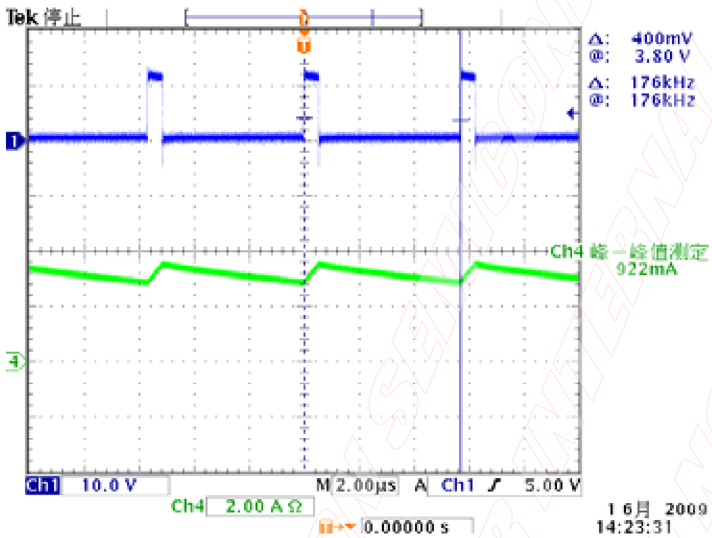
Start up soft start Vin=12V, Vout=5V Iout=2A



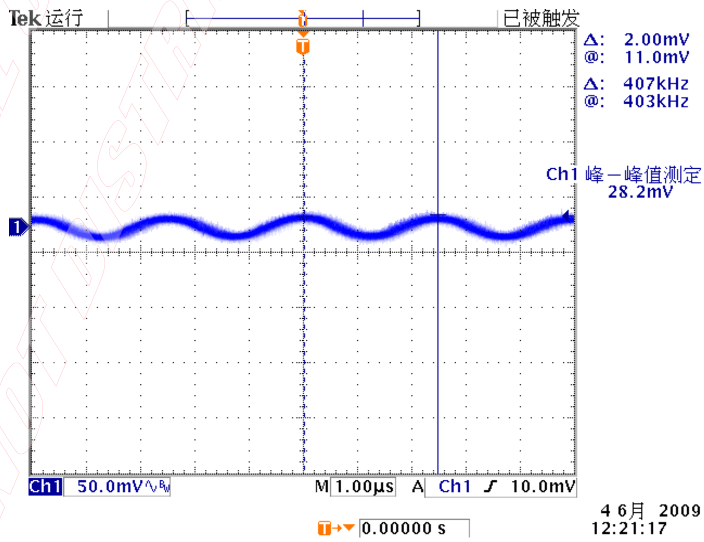
Operating status Vin=12V, Vout=5V Iout=2A



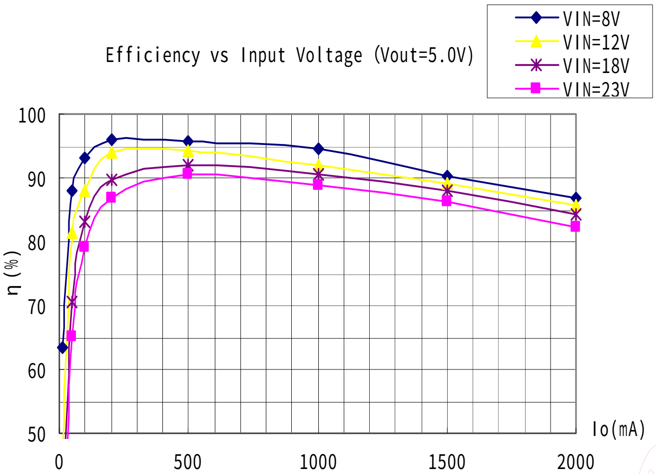
ripple of Vout Vin=12V, Vout=5V Iout=3A



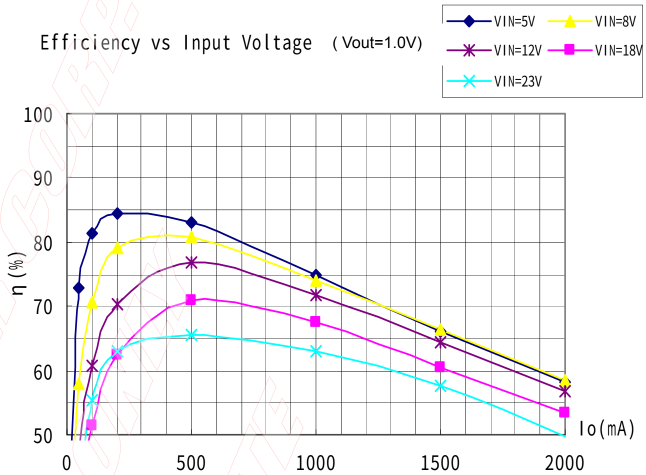
SCP



12Vin 5.0Vout Efficiency curve



12Vin 1.0Vout Efficiency curve



■ ORDERING INFORMATION

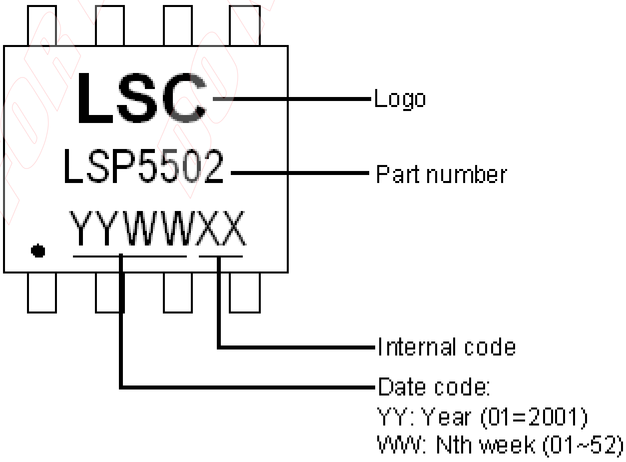
LSP5502 X X X

Package :
S: SOP8

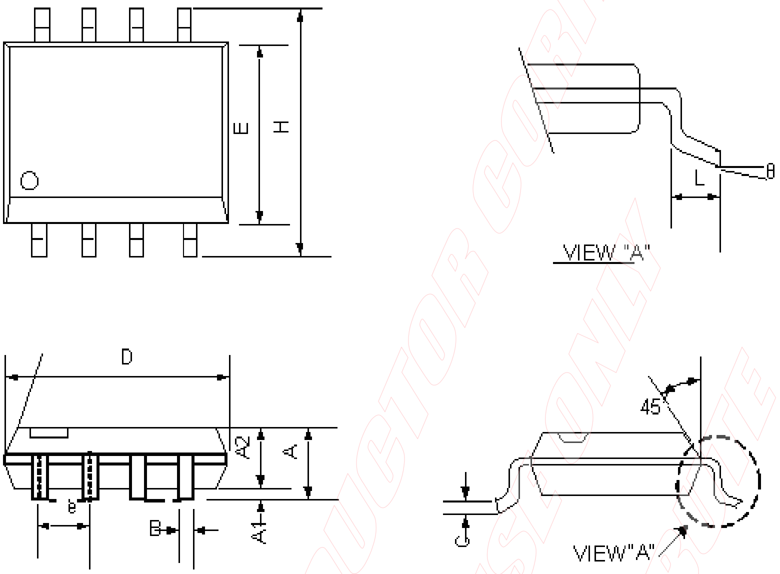
Packing :
Blank : Tube or Bulk
A : Tape & Reel

Temperature :
C : -20 ~ 85℃

■ MARKING INFORMATION



■ PACKAGE INFORMATION



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.35	1.6	1.75	0.053	0.063	0.069
A1	0.1		0.25	0.004		0.01
A2	1.25	1.45	1.55	0.049	0.057	0.061
B	0.31	0.41	0.51	0.012	0.016	0.02
C	0.1	0.2	0.25	0.0039	0.008	0.01
D	4.8	4.9	5	0.192	0.196	0.2
E	3.8	3.9	4	0.148	0.154	0.16
e		1.27 BSC		0.050 BSC		
H	5.7	6	6.3	0.224	0.236	0.248
L	0.4	0.71	1.27	0.015	0.028	0.05
θ	0^{o}		8^{o}	0^{o}		8^{o}

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