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[BT136S-600D,118](#)

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Cette fiche technique est
présentée par le fabricant



BT136S-600D

4Q Triac

30 September 2013

Product data sheet

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT428 (DPAK) surface-mountable plastic package intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants. This very sensitive gate "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Low holding current for low current loads and lowest EMI at commutation
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose motor control
- General purpose switching

4. Quick reference data

Table 1. Quick reference data

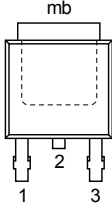
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{J}(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	25	A
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{mb}} \leq 107\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	4	A
Static characteristics						
I_{GT}	gate trigger current	$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T_2+ G+; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	2	5	mA
		$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T_2+ G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	2.5	5	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	2.5	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	5	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	1.2	10	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 DPAK (SOT428)	 sym051
2	T2	main terminal 2 [1]		
3	G	gate		
mb	T2	mounting base; connected to main terminal 2		

[1] it is not possible to make a connection to pin 2 of the SOT428 (DPAK) package

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT136S-600D	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{mb}} \leq 107\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3		-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5		-	25	A
		full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 16.7\text{ ms}$; Fig. 4 ; Fig. 5		-	27	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$; SIN		-	3.1	A^2s
dl_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 6\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $dl_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$; T2+ G+		-	50	$\text{A}/\mu\text{s}$
		$I_{\text{T}} = 6\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $dl_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$; T2+ G-		-	50	$\text{A}/\mu\text{s}$
		$I_{\text{T}} = 6\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $dl_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$; T2- G-		-	50	$\text{A}/\mu\text{s}$
		$I_{\text{T}} = 6\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $dl_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$; T2- G+		-	10	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	$^{\circ}\text{C}$
T_{j}	junction temperature			-	125	$^{\circ}\text{C}$

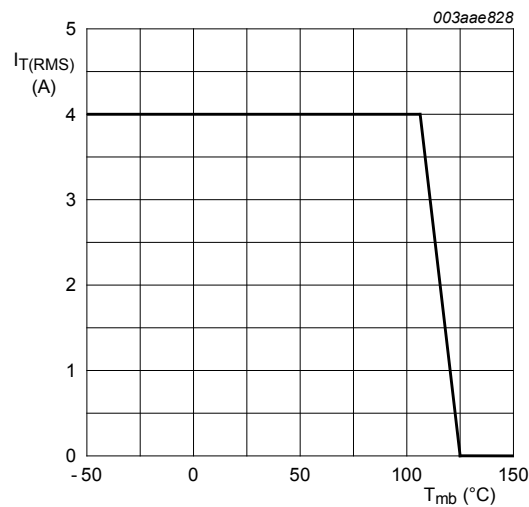
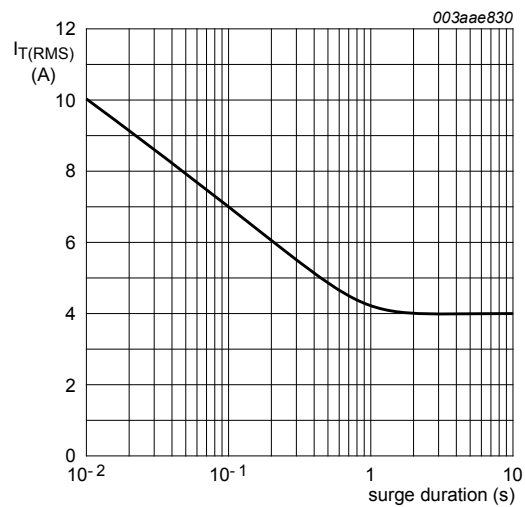
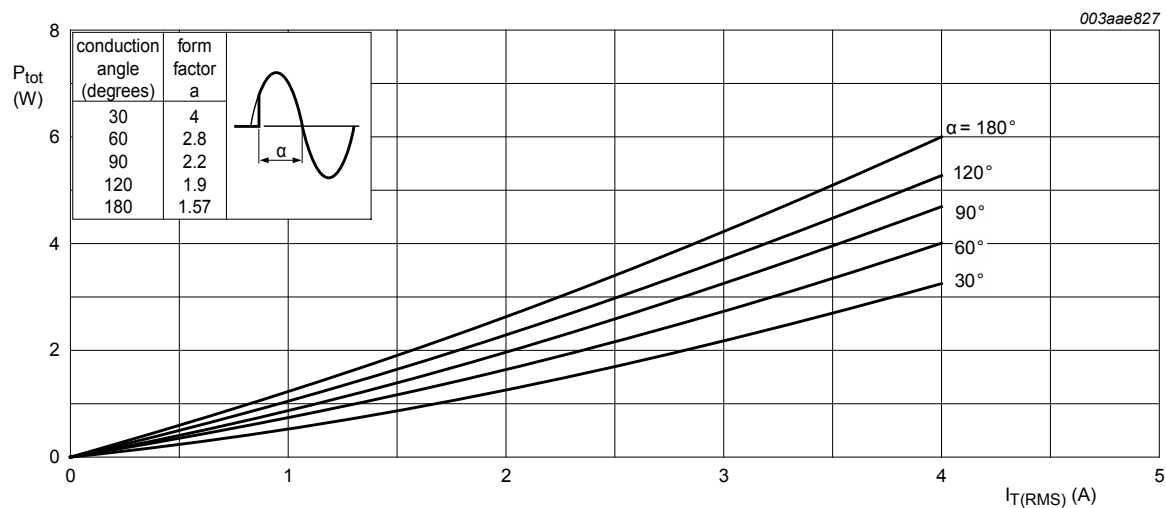


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz
T_{mb} ≤ 107 °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle
a = form factor = I_{T(RMS)} / I_{T(AV)}

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

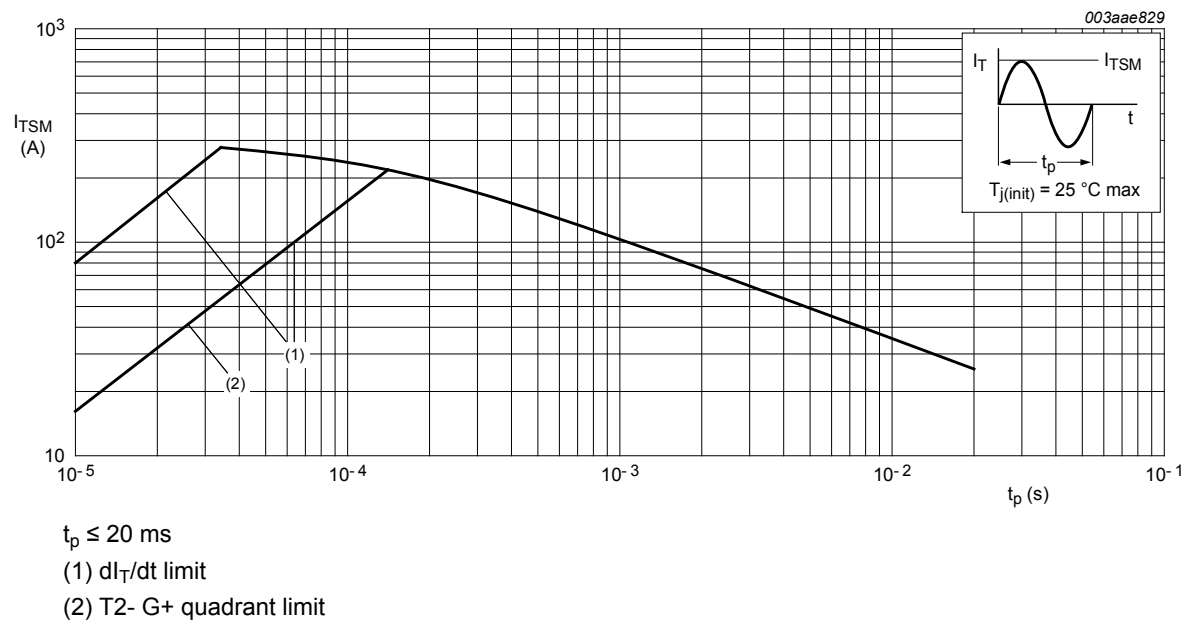


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

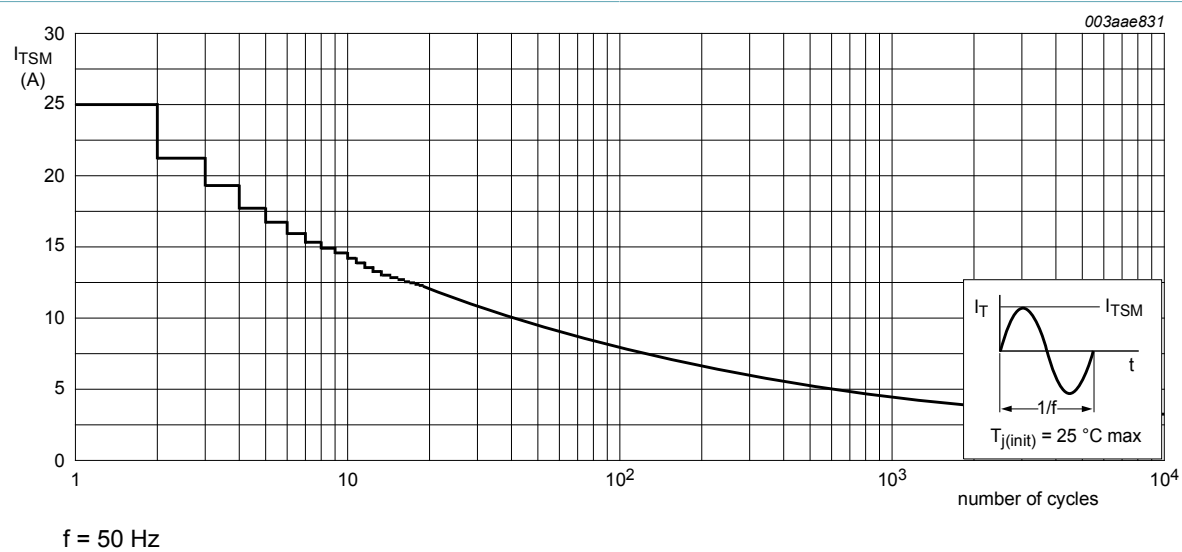


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 6		-	-	3	K/W
		half cycle; Fig. 6		-	-	3.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	75	-	K/W

[1] printed circuit board (FR4) mounted; standard footprint, single-sided copper, tin-plated

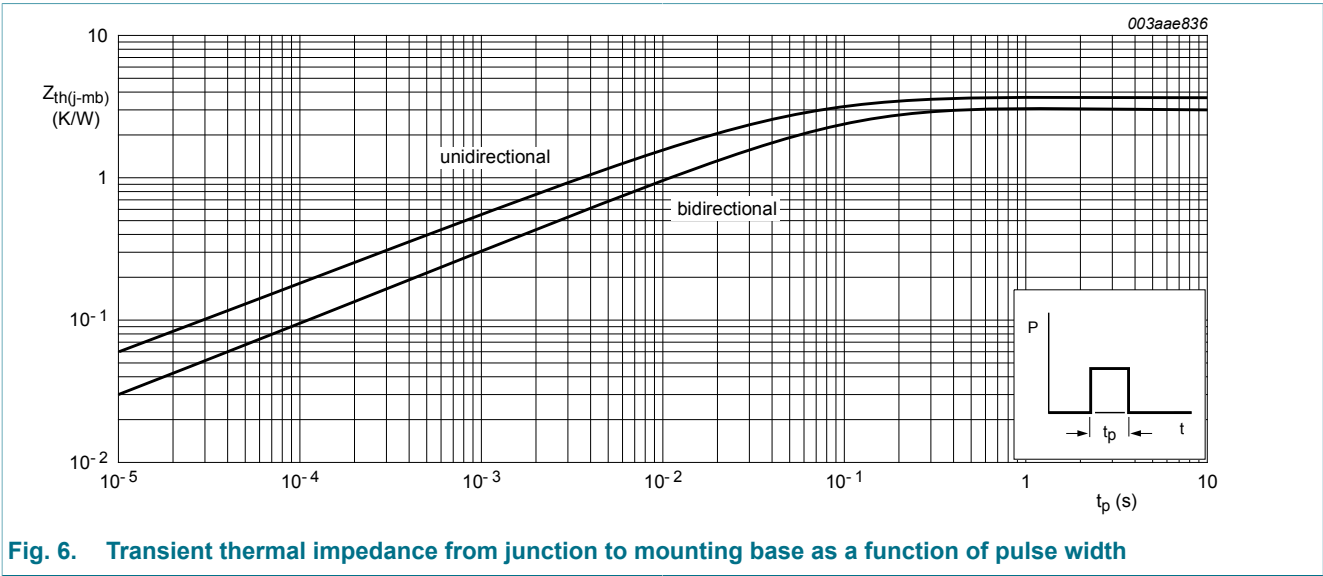
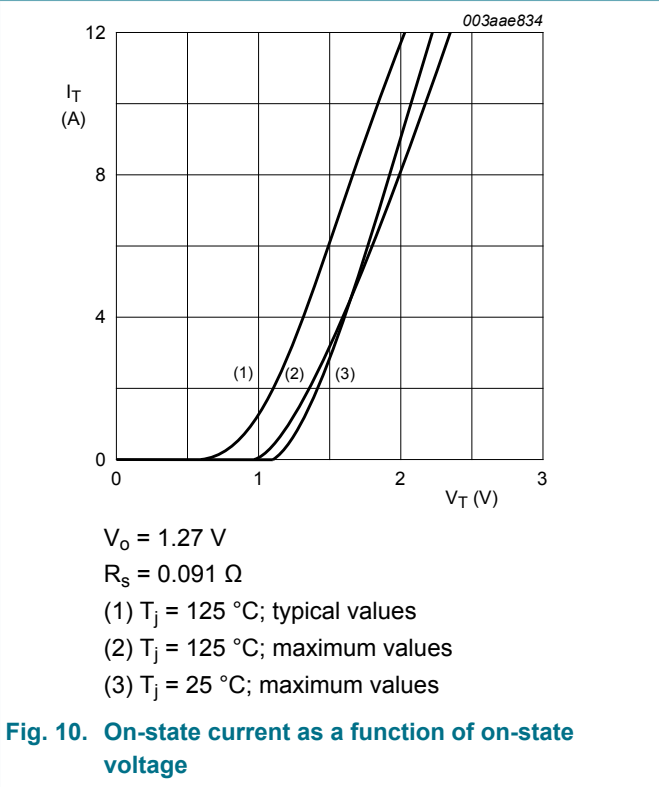
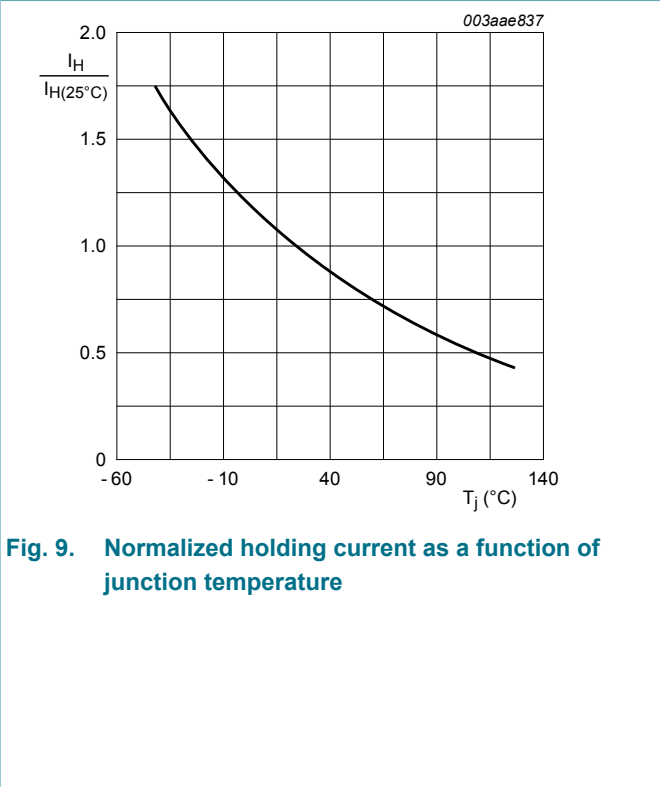
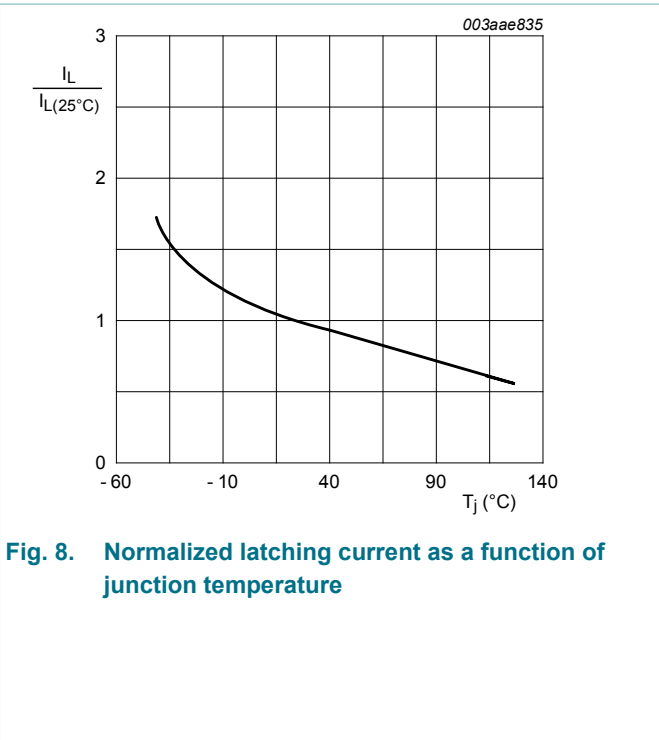
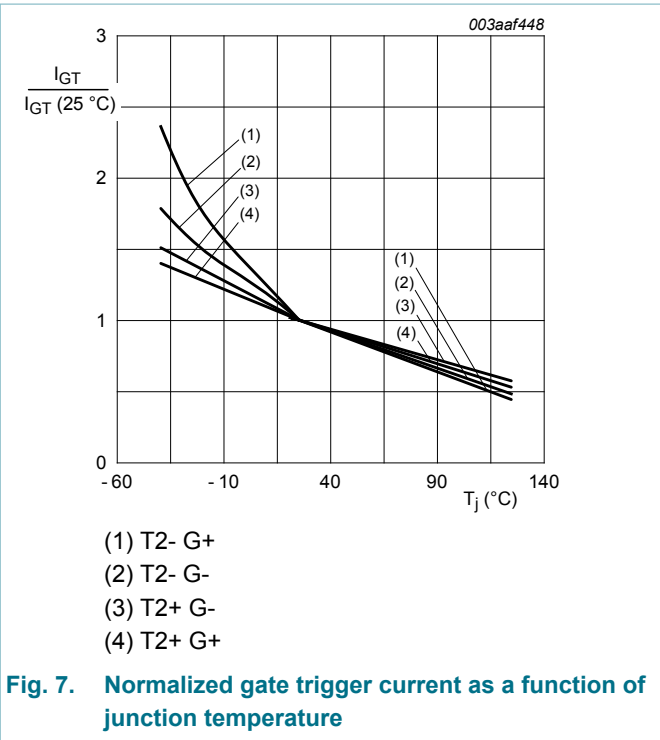


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	2	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	2.5	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	2.5	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	5	10	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	1.6	10	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	4.5	15	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	1.2	10	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	2.2	15	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	1.2	10	mA
V_T	on-state voltage	$I_T = 5\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.4	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	0.7	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11	0.25	0.4	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	-	5	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 6\text{ A}$; $V_D = 600\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μs



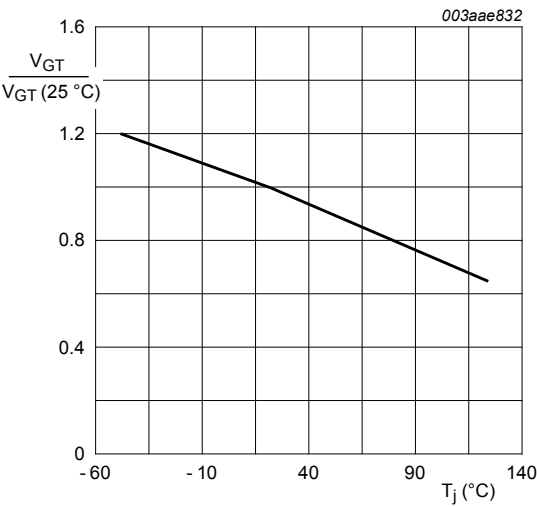


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

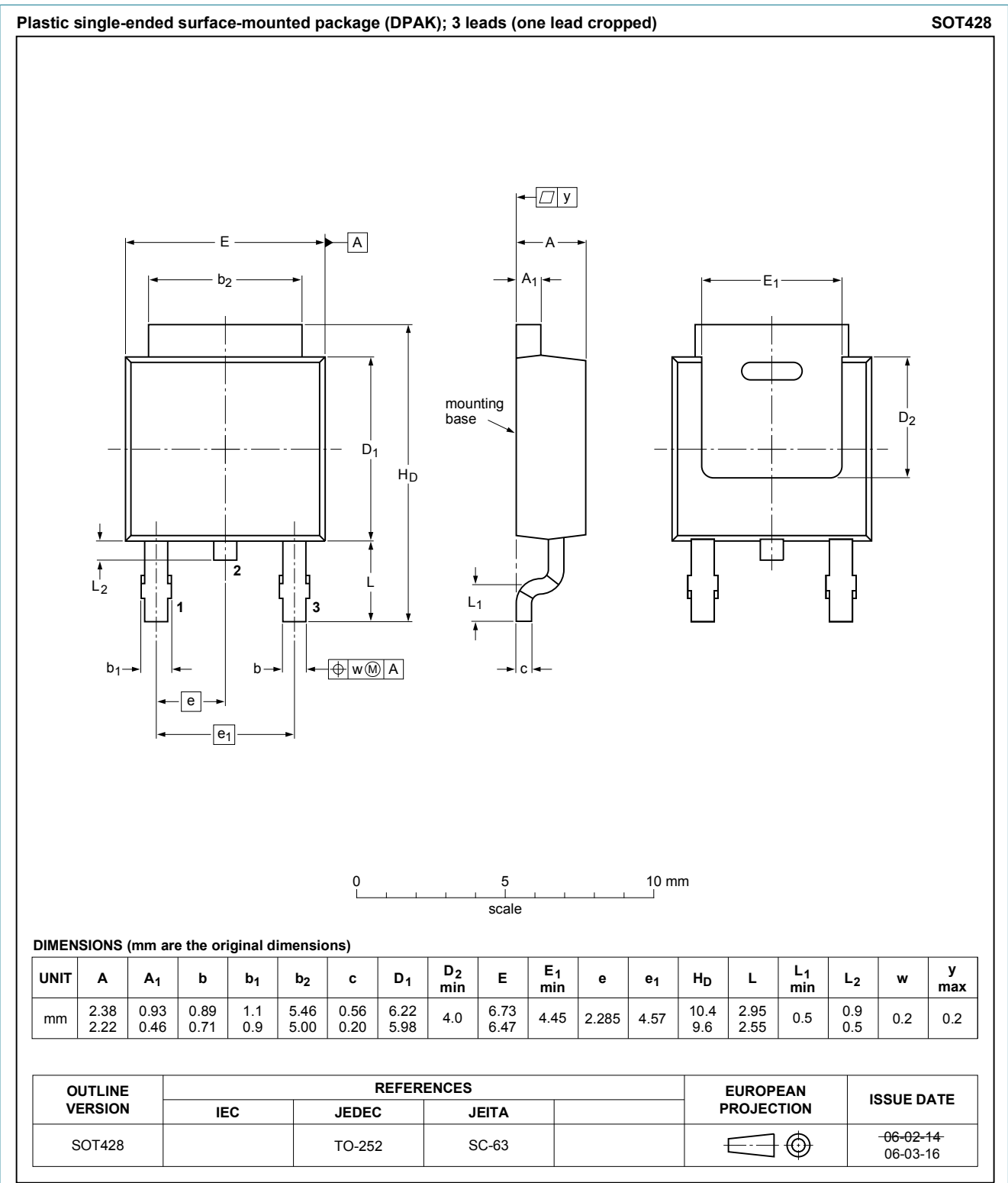
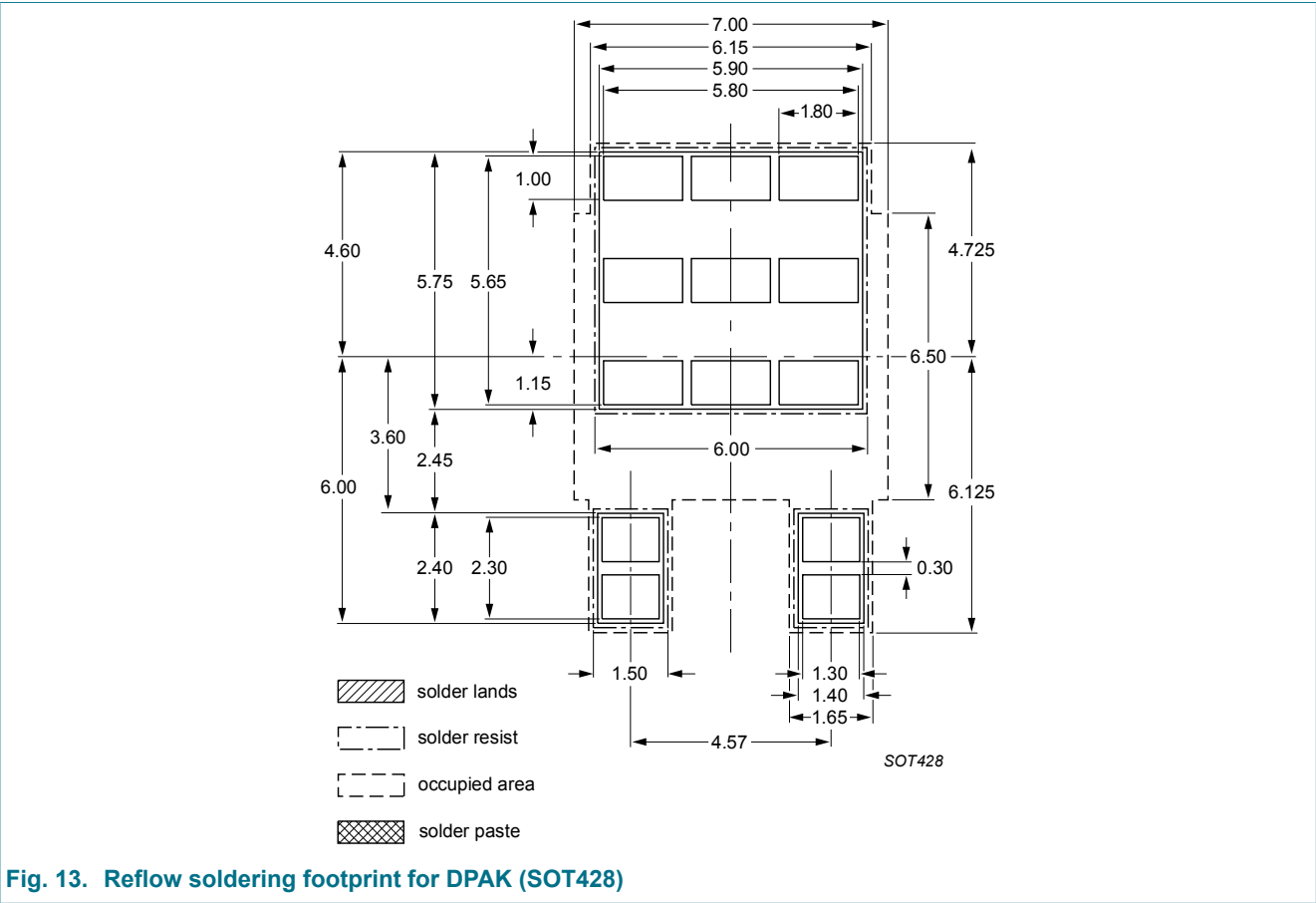


Fig. 12. Package outline DPAK (SOT428)

11. Soldering



12. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 30 September 2013

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