SLG3NB145

Notebook Clock

General Description

The SLG3NB145 uses a 25MHz quartz crystal to provide two 25MHz clock outputs and two 32.768kHz clock outputs and supports non-rechargeable CR coin cell batteries.

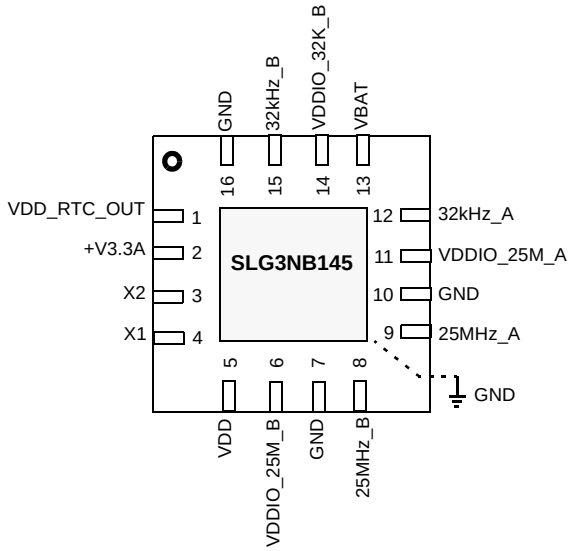
Features

- 32.768kHz GreenCLK technology
- 3.3V Swing 25MHz_A for LAN REFCLK
- Scalable VDD I/O for 25MHz_B
- Improved performance over temperature
- No 32.768kHz tuning fork crystal
- Smaller package
- Removes up to 12 components from a standard note-book/netbook design
- Integrated battery supply switch
- Pb-Free / RoHS compliant
- Halogen-Free
- Pb-Free 16-Pin TQFN package: 3mm x 3mm x 0.75mm, 0.5mm pitch

Applications

- Notebooks
- Netbooks

Pin Configuration



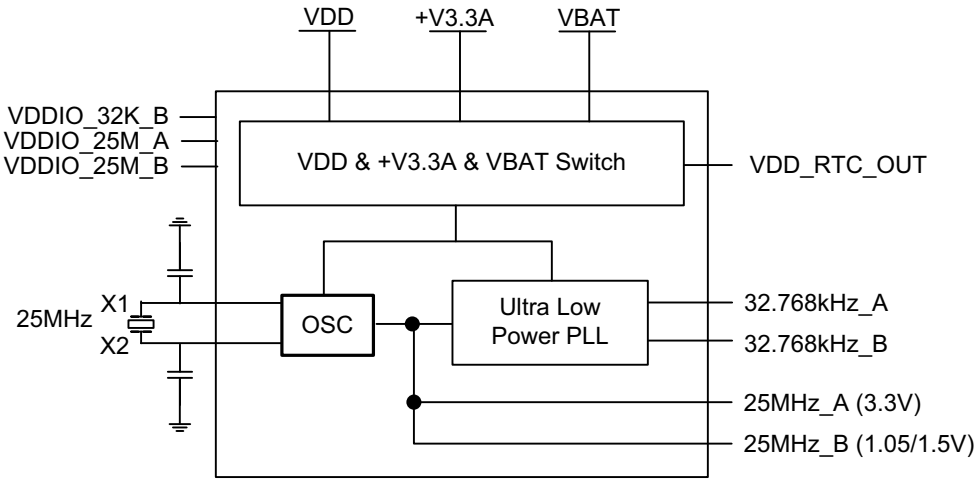
16-pin TQFN

(Top View)

Output Summary

- 2 - 32.768kHz clock outputs (2µA typ)
- 1 - 25MHz_A clock output (2mA typ) @ 3.3V Swing
- 1 - 25MHz_B clock output (1.5mA typ) @ 1.05V to 1.5V Swing

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD_RTC_OUT	PWR	Power Output
2	+V3.3A	PWR	+V3.3A Power Supply
3	X2	O, SE	25MHz crystal output
4	X1	I	25MHz crystal input
5	VDD	PWR	3.3V Power Supply, (S0 Power Rail)
6	VDDIO_25M_B	PWR	Power for 25MHz_B output (1.05V to 1.5V Typical)
7	GND	GND	Ground
8	25MHz_B	O, SE	25MHz Output (Stop by VDDIO_25M_B, pin 6) 1.05V to 1.5V Typical Swing
9	25MHz_A	O, SE	25MHz Output (Stop by VDDIO_25M_A, pin 11) 3.3V Typical Swing
10	GND	GND	Ground
11	VDDIO_25M_A	PWR	Power for 25MHz_A output (3.3V Typical)
12	32kHz_A	O, SE	32.768kHz clock output. (Free Running)
13	VBAT	PWR	Power for 32kHz_A output. Connect to coin cell battery. Clock will draw power from this pin when +V3.3A (Pin 2) = 0V.
14	VDDIO_32K_B	PWR	Power for 32kHz_B output
15	32kHz_B	O, SE	32.768kHz clock output. (Stop by VDDIO_32K_B, pin 14)
16	GND	GND	Ground
Exposed Bottom Pad	GND	GND	Ground

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DDMAX}	Absolute Max V_{DD}	V_{DDMAX}-GND	--	4.2	V
V_{BAT}	Absolute Max V_{BAT}	V_{BAT}-GND	--	4.2	V
T_O	Operational Temperature		-40	85	°C
T_S	Storage Temperature	Non-Functional	-65	150	°C
MSL	Moisture Sensitivity Level	16-Pin TQFN	1		

Recommended 25MHz Quartz Crystal Specifications

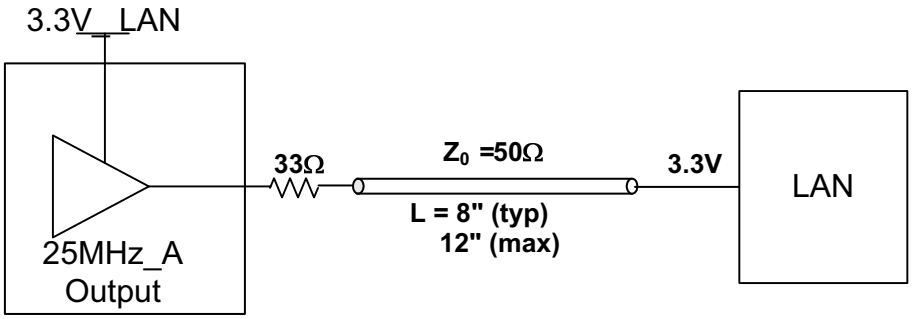
Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{INI}	Initial Frequency		--	25	--	MHz
F_{ERRI}	Frequency Accuracy	@ 25°C	--	--	±10	ppm
F_{ERRT}	Frequency Error over Temperature	@ -10°C to 70°C	--	--	±10	ppm
F_{AGE}	Frequency Aging	per year	--	--	±1	ppm
DL	Drive Level		--	--	100	µW
C_L	Crystal Load Capacitance	Parallel Resonance		8		pF
AT	AT Cut Crystal		--	--	--	
Mode	Fundamental		--	--	--	

25MHz_A REF Clock Output Characteristics

TA = 25°C, V_{DD} = 3.3V (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{INI}	Initial Frequency		--	25	--	MHz
F_{ERRI}	Initial Frequency Error	@ 25°C	--	--	±10	ppm
F_{ERRT}	Frequency Error over Temperature Range	-10°C to 70°C	--	--	±10	ppm
DC	Duty Cycle	$V_{DD}/2$	45	50	55	%
V_{OH}	Output Voltage HIGH	4 pF, I_{OH} = 1mA	$0.8V_{DD\_IO}$	--	--	V
V_{OL}	Output Voltage LOW	4 pF, I_{OL} = -1mA	--	--	$0.2V_{DD\_IO}$	V
SR_{OUT}	Slew Rate	measured at V_{OH} and V_{OL} level	0.5	--	2	V/ns
V_{DDIO_25A}	Voltage Supply Range		3.0	--	3.6	V

25MHz_A Output

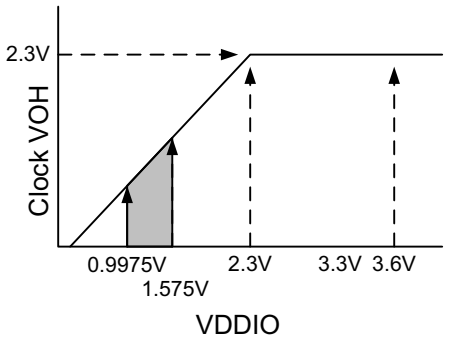


25MHz_B REF Clock Output Characteristics

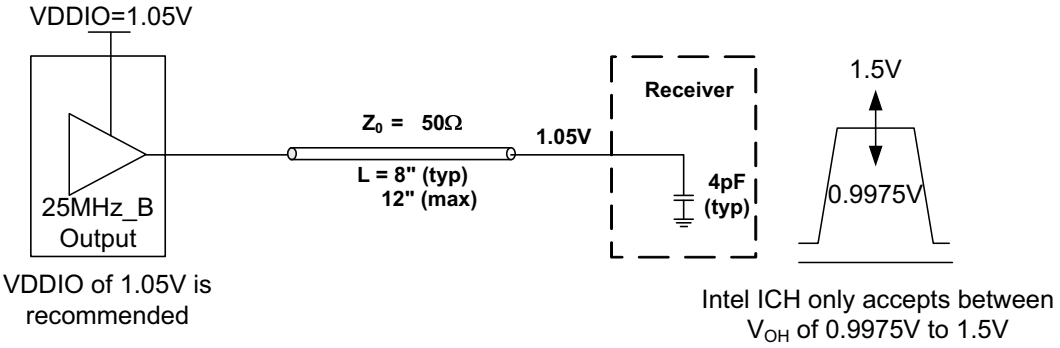
TA = 25°C, V_{DD} = 3.3V (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{INI}	Initial Frequency		--	25	--	MHz
F_{ERRI}	Initial Frequency Error	@ 25°C	--	--	±10	ppm
F_{ERRT}	Frequency Error over Temperature Range	-10°C to 70°C	--	--	±10	ppm
DC	Duty Cycle	V_{DD}/2	45	50	55	%
V_{OH}	Output Voltage HIGH	4 pF, I_{OH} = 1mA	$0.8V_{DDIO}$	--	--	V
V_{OL}	Output Voltage LOW	4 pF, I_{OL} = -1mA	--	--	$0.2V_{DDIO}$	V
SR_{OUT}	Slew Rate	measured at V_{OH} and V_{OL} level	0.5	--	2	V/ns
V_{DDIO_25B}	Voltage Supply Range		0.9975	--	1.575	V

25MHz_B VDDIO Power Supply Operating Range



25MHz_B Output



VDDIO of 1.05V is recommended

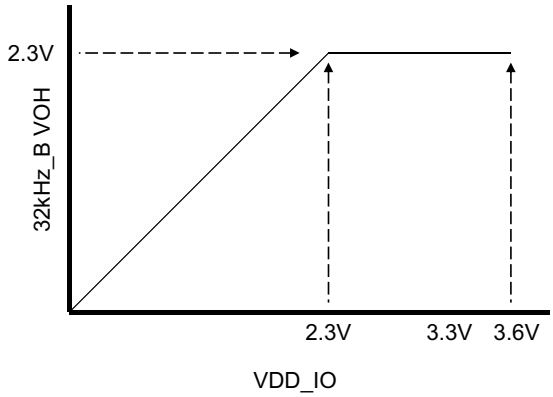
Intel ICH only accepts between V_{OH} of 0.9975V to 1.5V

32.768kHz_A & 32.768kHz_B Output Characteristics

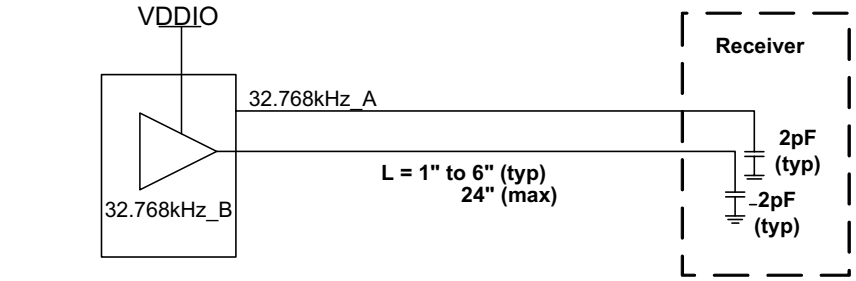
TA = 25°C, V_{DD} = 3.3V (unless otherwise stated)

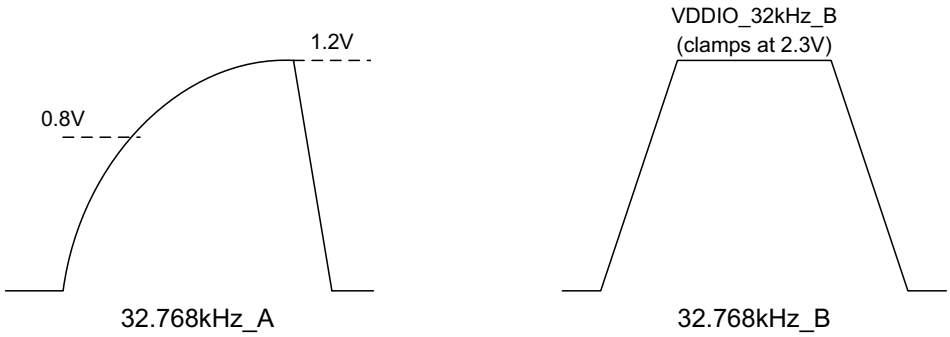
Symbol	Description	Conditions	Min	Typ	Max	Unit
Freq	Frequency		--	32.768	--	kHz
$32F_{ERRI}$	Initial Frequency Error See Application Note SLG3AN001 - GreenCLK Technology Calibration Methods	Basic Time Keeping Mode (BTK)	--	±17	±32	ppm
			--	--	3	sec/day
		One Time Adjusted Keeping Mode (OTA)	--	--	±6	ppm
			--	--	0.5	sec/day
		Dynamic Adjusted Time Keeping Mode (DAT)	--	--	±3	ppm
			--	--	0.25	sec/day
$32F_{ERRT}$	Frequency Error over Temperature Range See Application Note SLG3AN001 - GreenCLK Technology Calibration Methods	-10°C to 40°C, in BTK Mode	--	±20	±34.5	ppm
			--	--	3	sec/day
		-10°C to 40°C, in OTA Mode	--	--	±9	ppm
			--	--	0.75	sec/day
		-10°C to 40°C, in DAT Mode	--	--	±3	ppm
			--	--	0.25	sec/day
DC	Duty Cycle	V_{BAT}/2	40	50	60	%
V_{OH}	Output Voltage HIGH	32kHz_A	0.8	1.0	1.2	V
V_{OL}	Output Voltage LOW	32kHz_A	--	--	0.3	V
V_{OH}	Output Voltage HIGH	32kHz_B	See Graph B	--	--	V
V_{OL}	Output Voltage LOW	32kHz_B	--	--	$0.2V_{DD\_IO}$	V
SR_{OUT}	Slew Rate		--	0.03	--	V/ns

Graph B



Output Buffer





GreenCLK 32.768 kHz Error Explained in Basic Time Keeping Mode with NO software calibration

32.768 kHz Clock output error is made up of many components. The error sources are:

- 25 MHz crystal initial ppm error
- 25 MHz crystal over temperature error
- 25 MHz crystal aging error
- GreenCLK random error
- GreenCLK offset error

Random Error Sources add by the Square Root (Error Source A^2 + Error Source B^2). Deterministic Error Sources add directly Error Source C + Error Source D

Error Source	Random	Value in ppm	DPMO 1 sigma	DPMO 2 sigma (Typical Spec)	DPMO 3 sigma (Max Spec)
			31% of parts	69% of parts	93.3% of parts
			LT C_{pk} 0.33	LT C_{pk} 0.67	LT C_{pk} 1.00
25 MHz crystal initial offset error	Yes	±10	±3	±7	±9.5
25 MHz crystal temperature error	Has both Random and Deterministic Error	±10	±1.5 R ±2.5 D	±3.5 R ±2.5 D	±5 R ±2.5 D
25 MHz crystal aging error	Has both Random and Deterministic Error	±1 per year	±0.5	±0.5	±1
GreenCLK additional random error	Yes	±28	±5.5	±13	±28
GreenCLK additional offset error	No	+2	+2	+2	+2
Total GreenCLK ERROR @ 25°C			±8	±17	±32
Total GreenCLK Error @ -10°C to +40°C			±11	±20	±34.5
Total GreenCLK Error @ +10°C to +70°C			±8	±15	±30

+V3.3A and VBAT Electrical Specification

T_A = 25°C, V_{DD} = 3.3V (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
+V3.3A	Operating Voltage	Normal operating mode	3.0	3.3	3.6	V
V_{DD}	Operating Voltage	Normal operating mode	3.0	3.3	3.6	V
$V_{BAT\_CR/BR}$	Coin Battery Voltage	Normal operating mode	2.3	2.9	3.6	V
$V_{SWITCH1}$	V_{DD} Voltage trigger level to enter battery mode	V_{BAT} Mode	--	--	1.80	V
$V_{SWITCH2}$	Voltage trigger level to enter V_{DD} mode	V_{DD}Mode	1.95	--	--	V
V_{TRIP-L}	V_{BAT} Mode Low Threshold		1.7	1.8	1.9	V
V_{TRIP-H}	V_{BAT} Mode High Threshold		1.8	1.9	2.0	V
I_{VBAT}	V_{BAT} Current Consumption when 32.768 kHz draws power from V_{BAT}	V_{DD} = 0V, V_{BAT} = 3.3V	--	2	--	µA
I_{VDD}	Current Consumption, all outputs active	V_{DD} = 3.3V, V_{BAT} = 3.3V	--	2.5	3	mA
I_{VBAT_SWI}	V_{BAT} Current Consumption when device switches from $V_{DD}$to V_{BAT} or +V3.3A	V_{DD} = 0V, V_{BAT} = 3.3V, 0 < switch time < 10sec	--	35	40	µA
$GPOUT_{VDD}$	VDD_RTC_OUT Output Voltage Level	VDD Mode	3.15	3.3	3.45	V
$GPOUT_{VDD}$	VDD_RTC_OUT Output Voltage Level	Battery Mode	1.8	3.0	3.3	V
$GPOUT_{ICC}$	VDD_RTC_OUT Current Output		--	6	10	µA

Power Supply State Table

Power Supply (V)			V_{DDIO} Control			Outputs					Current Consumption		
V_{BAT} (Pin 13)	$+V_{3.3A}$ (Pin 2)	V_{DD} (Pin 5)	V_{DDIO} 32k_B	V_{DDIO} 25M_A	V_{DDIO} 25M_B	32kHz_A	32kHz_B	25MHz_A	25MHz_B	Voltage at $V_{BAT\_RTC\_OUT}$	V_{BAT} (µA) typ	$+V_{3.3A}$ (µA) typ	V_{DD_25MHz} (mA) typ
2.3 to 3.0	0	0	1	N/A	N/A	ON	OFF	OFF	OFF	V_{BAT}	2.5	0	0
2.3 to 3.0	0	0	0	N/A	N/A	ON	OFF	OFF	OFF	V_{BAT}	2.5	0	0
2.3 to 3.0	3.3	0	1	N/A	N/A	ON	ON	OFF	OFF	$+V_{3.3A}$	0	4	0
2.3 to 3.0	3.3	0	0	N/A	N/A	ON	OFF	OFF	OFF	$+V_{3.3A}$	0	4	0
2.3 to 3.0	3.3	3.3	o	0	o	ON	OFF	OFF	OFF	$+V_{3.3A}$	0	4	2.5
2.3 to 3.0	3.3	3.3	0	0	1	ON	OFF	OFF	ON	$+V_{3.3A}$	0	4	2.5
2.3 to 3.0	3.3	3.3	0	1	0	ON	OFF	ON	OFF	$+V_{3.3A}$	0	4	2.5
2.3 to 3.0	3.3	3.3	0	1	1	ON	OFF	ON	ON	$+V_{3.3A}$	0	4	2.5
2.3 to 3.0	3.3	3.3	1	0	0	ON	ON	OFF	OFF	$+V_{3.3A}$	0	4	2.5
2.3 to 3.0	3.3	3.3	1	0	1	ON	ON	OFF	ON	$+V_{3.3A}$	0	4	2.5
2.3 to 3.0	3.3	3.3	1	1	0	ON	ON	ON	OFF	$+V_{3.3A}$	0	4	2.5
2.3 to 3.0	3.3	3.3	1	1	1	ON	ON	ON	ON	$+V_{3.3A}$	0	4	2.5

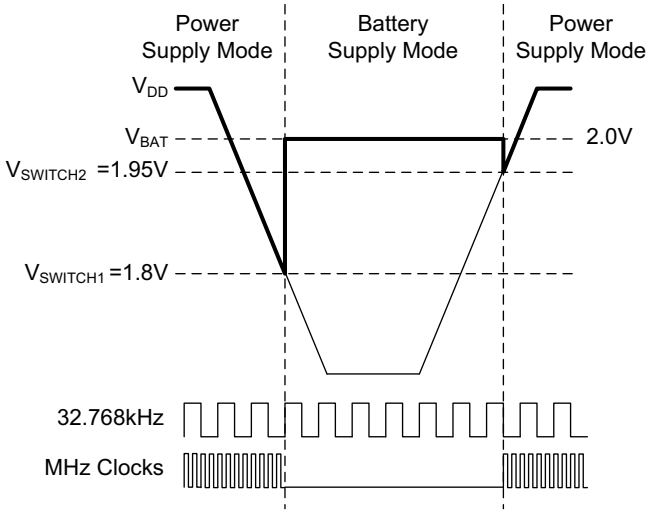


Figure 1. Power Modes Voltage Trigger.

VBAT Battery Recommendations

Coin Battery

Part Number	SLG3NB145 32.768kHz Lifetime	Capacity (mAH)	Voltage Range(V)			Max Discharge Current (mA)		Cycles @ 20% Discharge Depth		Dimensions (mm)		Charge Voltage continous
			95%	50%	5%	Constant	Peak	5%	20%	Dia.	Height	
CR2032[1]	10 years	220 to 235	3	2.9	2.3	4	20			20	3.2	

Notes:

[1] Lithium Manganese Dioxide Battery

Reference Design Comparison
SLG3NB145 Clock Reference design using Non-Rechargeable CR or BR Coin cell battery

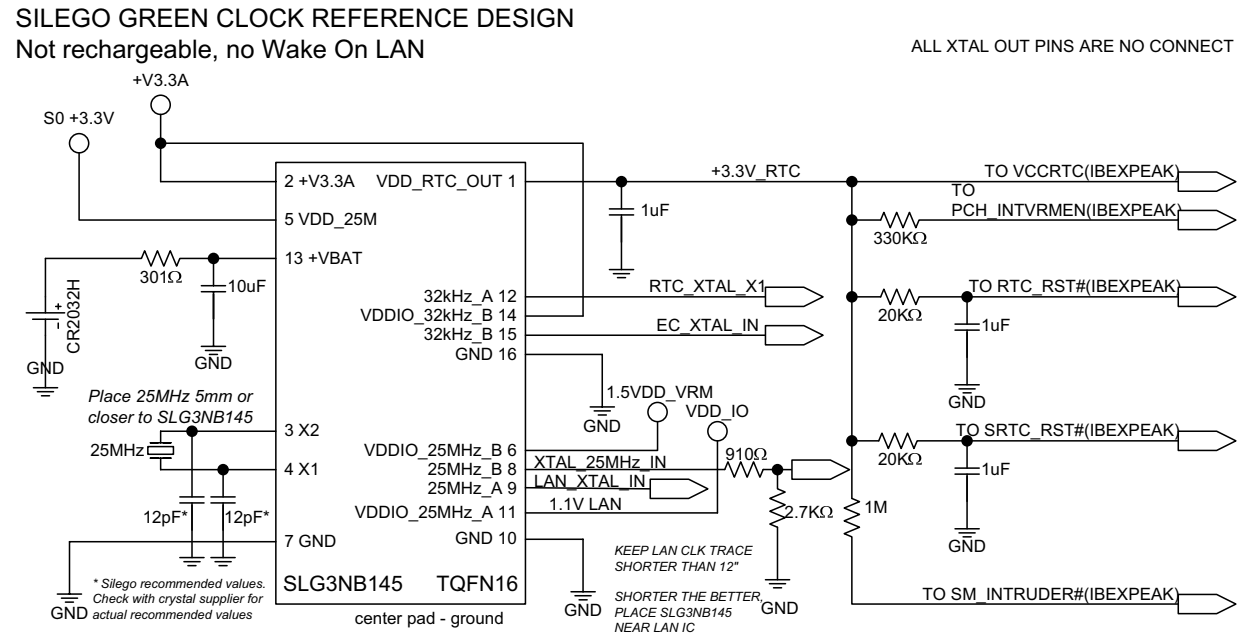


Figure 2. Silego Reference Design - Non-rechargeable.

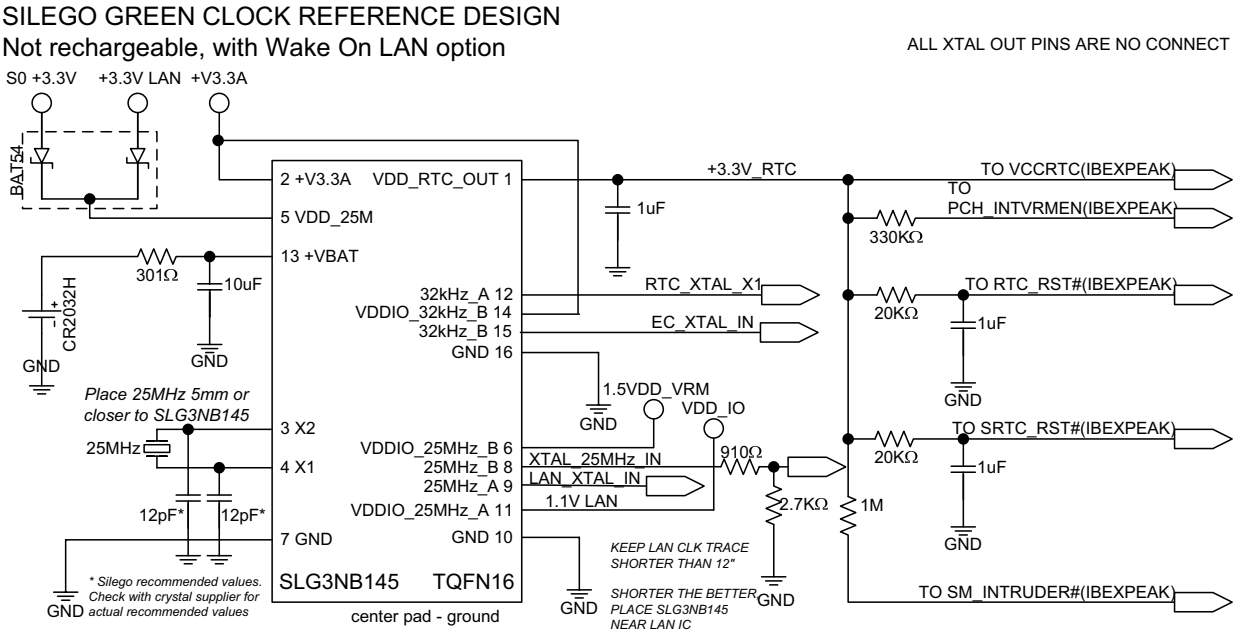


Figure 3. Silego Reference Design - Non-rechargeable with WOL option.

Differences between Intel Design Guidelines for RTC with external crystal and SLG3NB145

RTC

The Intel ICH contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The Intel ICH RTC module requires an external oscillating source of 32.768 kHz connected on RTCX1 and RTCX2 balls. The SLG3NB145 removes the requirement for RTCX2 to be connected. RTCX2 is left disconnected; however do NOT tie RTCX2 to ground.

RTC Signals

Group	Signals	Description
Crystal Input 1	RTCX1	Crystal Input 1
Crystal Input 2	RTCX2	The Intel guidelines refer to this as in input, actually it is an output and maybe left unconnected

The Input ICH uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal via the RTCX2 signal. The SLG3NB145 does not require this feedback. Internal to the Intel ICH the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for the system to use. This output ball of the Intel ICH is called SUSCLK.

RTC Layout Considerations

The Intel design RTC circuit is very sensitive and requires highly accurate oscillation. However, the Silego RTC generation circuit is much more insensitive (1000x less sensitive) to noise to achieve the same high performance. There is no need to reduce trace capacitance or place the SLG3NB145 near the Intel RTC as is required for the 32.768 crystal. The SLG3NB145 is a driven clock with low impedance and therefore can be placed a long distance from the embedded controller or RTC circuit.

Using a ground guard plane, 50 ohm matched traces, microstrip lines may be used but are not required and will not give any better performance.

The oscillator VCC should be clean however an RC low-pass or a ferrite inductor is NOT required. It is recommended that an RC low-pass or ferrite inductor be laid out for risk mitigation in case the oscillator VCC is very dirty.

RTC Routing Guidelines

Signal Name	Impedance	Width (W)	Layer	Length	Figure	Notes
RTCX1	50Ω ±15%	4 mils	Microstrip	0-24”		
RTCX2	No Connect					

External Capacitors

The SLG3NB145 does not require the 32.768 kHz crystal and as such capacitor trimming is NOT required.

In the Intel design guideline a best case condition of ppm error is given. The example does not evaluate ppm beyond +0°C to +50°C, does not address again 3 ppm/year, does not address temperature rollover variation ±5°C, does not address the ppm variation with capacitor value tolerance, does not address the ppm variation with capacitor value vs. temperature. Intel recommends that the crystal be “tuned” with perfect capacitors that are not available for purchase anywhere in this universe to run +23 ppm high which is an error of about 8 seconds per month at room temperature.

Temperature can change the frequency of the 32.768 kHz crystal dramatically and permanently so it is important to place the 32.768 kHz a long distance 2-3” from significant heat sources.

GreenCLK Technology Calibration Methods

See Application Note SLG3AN001 - GreenCLK Technology Calibration Methods document.

RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and it's RAM while the Intel ICH is not powered by the system.

Example batteries are: Duracell 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 6 µA, the battery life will be at least:

170,000 µAh / 6 µA = 28,333 hours = 3.2 years

There are three significant changes to the battery circuitry that need to be discussed when comparing the Silego and Intel solutions.

First, the average current consumption on the battery is increased from 6µA to 8.5µA. Next, the Intel reference solution is based on the non-rechargeable CR or BR type coin cell battery technology. A more modern, smaller, longer-lasting option is to switch to the rechargeable ML type rechargeable coin cell battery (The SLG3NB145 does not support this option). Finally, a 10µF ceramic capacitor needs to be added in parallel to the battery to limit the effect of current spikes from the Silego chip on the long term performance of the battery.
In the Intel reference design solution the voltage of the battery as it decays influences the RTC accuracy. However, because the Silego solution is internally regulated the battery voltage will have very little influence on the accuracy of the 32.768 kHz reference clock.

The battery must be connect to the Intel ICH chip via an isolation Schottky diode circuit. The "Schottky" diode circuit is included in the Silego SLG3NB145. However, the series resistor for the CR/BR type batteries should be changed from 1K to 300 ohms, and 100Ω for ML batteries (not supported by the SLG3NB145) must be present external to the SLG3NB145 to meet the UL safety current limit specifications should the "Schottky" diode circuit stop functioning. The Schottky diode circuit allows the ICH RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this function, the diodes are set to be reversed biased when the system is not available. Do not include the "Schottky" diodes shown in the Intel Design Guide when using the SLG3NB145 IC because the Silego IC already includes the equivalent of these diodes internally in the chip. The 1.0µF capacitor called for in the Intel spec should be placed on the output of the SLG3NB145 at VDD_RTC_OUT. The VDD_RTC_OUT is specified to provide all the current required for the Intel ICH RTC and reset circuits.

RTC External RTCRST# Circuit

The use of the SLG3NB145 does not impact the Intel design requirements for the RTCRST# circuit.

RTC External SRTCRST# Circuit

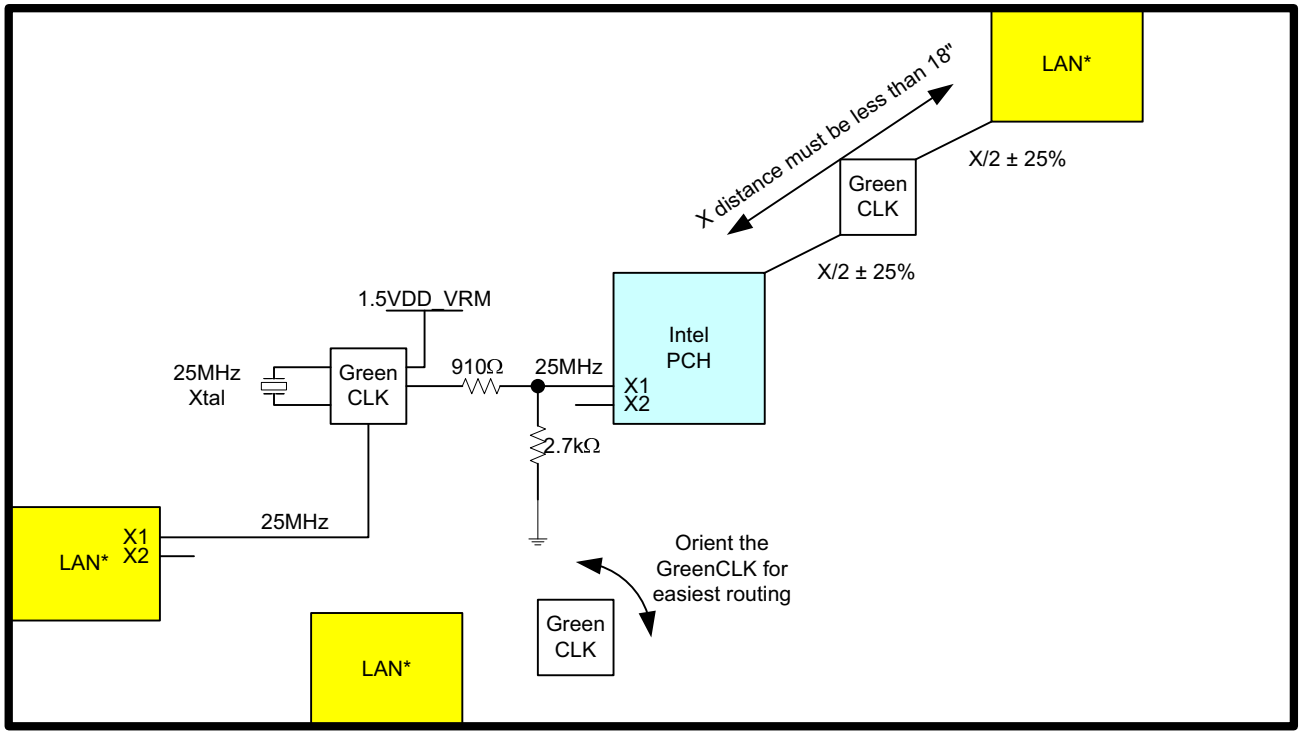
The use of the SLG3NB145 does not impact the Intel design requirements for the SRTCRST# circuit.

RTC-Well Input Strap Requirements

The use of the SLG3NB145 does not impact the Intel design requirements for the RTC-Well Input strap requirements.

Recommended GreenCLK Placement

The MHz crystals determine where the GreenCLK is to be placed as the 32.768 kHz clocks are not as jitter sensitive and do not have as many issues with EMI and signal integrity If LAN 25 MHz frequency comes from GreenCLK: place GreenCLK ~1/2 the distance between LAN and Intel PCH. The LAN and PCH Xtal inputs are NOT 50Ω terminated.

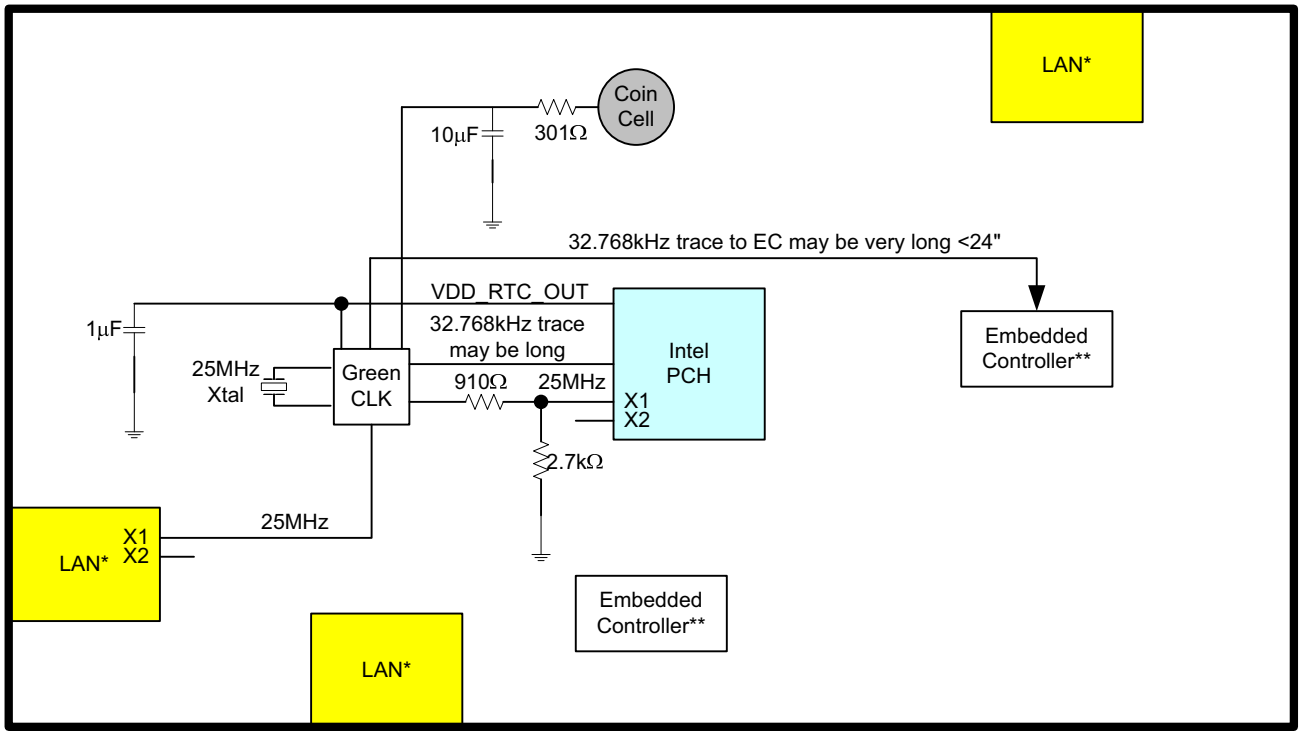


* Possible LAN locations

Figure 4. GreenCLK Placement Reference.

Performance: The 25 MHz GreenCLK for both the PCH and LAN will be better than 3 ps rms phase jitter from 12 kHz to 20 MHz. The 25 MHz LAN clock is NOT derived from a PLL and as such the performance will be very good.

Recommended GreenCLK Placement (cont.)



* Possible LAN locations
** Possible Embedded Controller locations

Figure 5. GreenCLK Placement Reference.

The 32.768 kHz clocks are not as sensitive to layout issues like EMI, interference, and jitter issues because a 32.768 kHz xtal has ~50kΩ of impedance, a 32.768 kHz clock is just a few hundred ohms. The CR coin cell safety resistors must be reduced from 1kΩ to ~300Ω. A 10µF capacitor needs be placed after the safety resistor. The BAT54 diode should be removed.

GreenCLK Layout

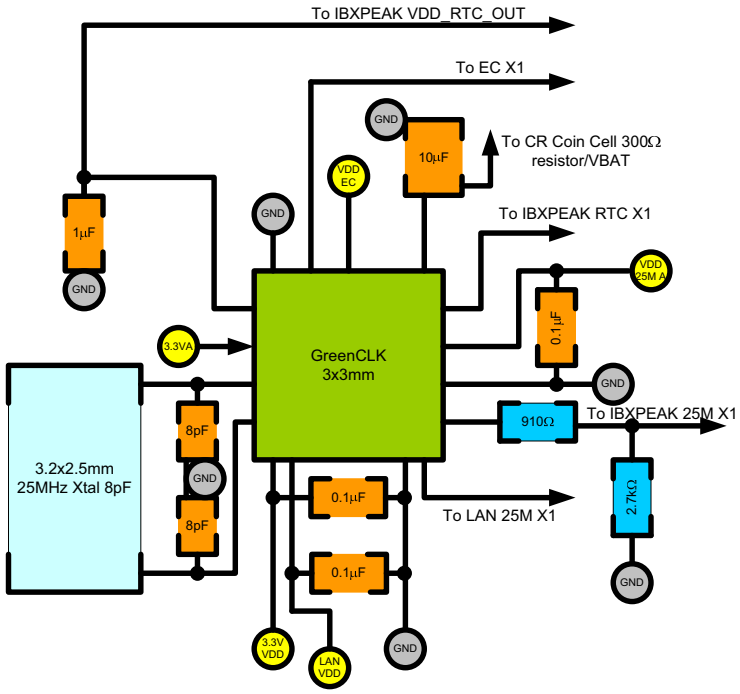


Figure 6. GreenCLK Layout Reference.

GreenCLK Tuning

The GreenCLK is a highly accurate device. However board layout and error tolerance the crystal load capacitors can change the ppm accuracy of the system. Be assured that this error tolerance is LESS in magnitude and easier to control as compared to traditional 32.768 kHz crystals.

The GreenCLK gives the lowest over power consumption when a 25MHz crystal is specified with low pF load capacitors like 8 pF or 12 pF. Experimentally Silego has found that up to 10 or 20 ppm error can be introduced due to variations in the amount of capacitance. Typically 1 pF of change in load capacitance can effect the 32.768 kHz frequency by up to 10 ppm.

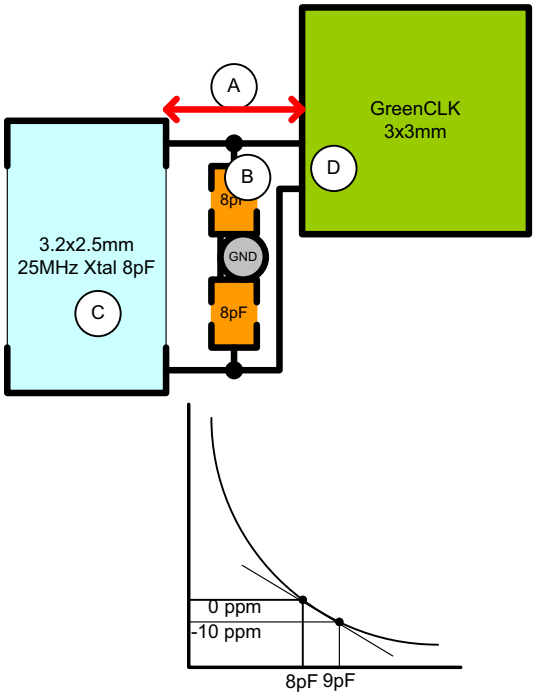
As pictured to the right, capacitor error sources are:

A: Trace length

B: Capacitor tolerance

C: Quartz manufacturing sensitivity to load capacitance

D: The amount of capacitance internally on the X1 and X2 pin of the GreenCLK.



The ONLY way to ensure high accuracy is after the system is completed and then tuning the final load capacitors. The easiest way to do this is to first build your notebook. Then start the RTC and record the exact time to the second with a high accuracy clock. Then record the time and error one day later, then two days, and continually do this for up to 1 week. One second of error per day is ~10 ppm. Therefore, to speed the clock up decrease the load capacitors by 1 pF, to slow the clock down increase the load capacitors by 1 pF.

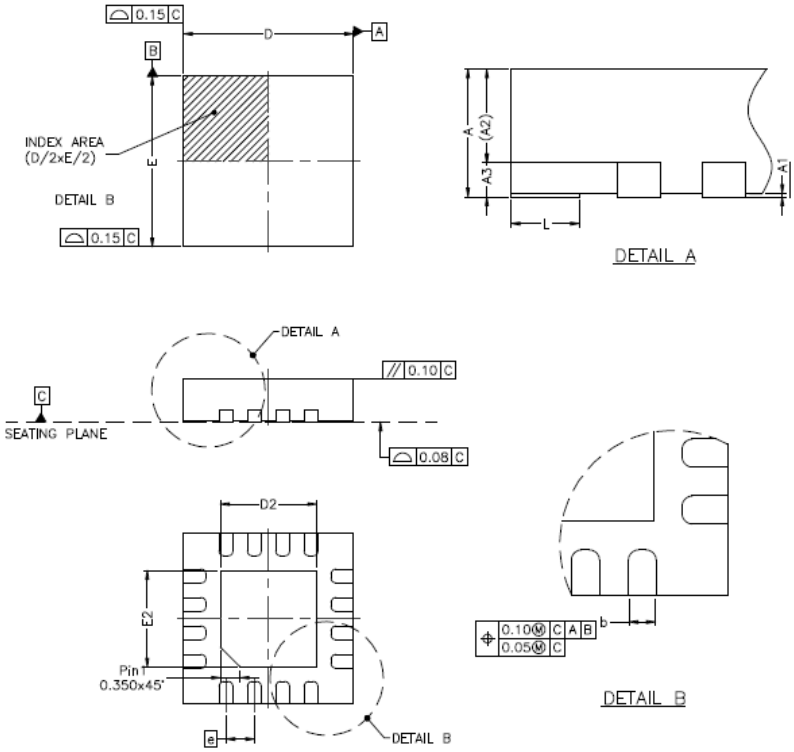
Once tuned, the GreenCLK has been shown to hold the frequency to typically better than 2-3 ppm while aging less than comparable 32.768 kHz crystals

Ordering Information

Part Number	Type	Production Flow
SLG3NB145V	16-pin TQFN	Extended Commercial, -10°C to 70°C
SLG3NB145VTR	16-pin TQFN - Tape and Reel	Extended Commercial, -10°C to 70°C

Package Drawing and Dimensions

16 Lead TQFN Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	2.90	3.00	3.10	114	118	122
D1		–			–	
D2	1.60	1.70	1.80	63	67	71
E	2.90	3.00	3.10	114	118	122
E1		–			–	
E2	1.60	1.70	1.80	63	67	71
e	0.50 BSC			20 BSC		
L	0.35	0.40	0.45	14	16	18

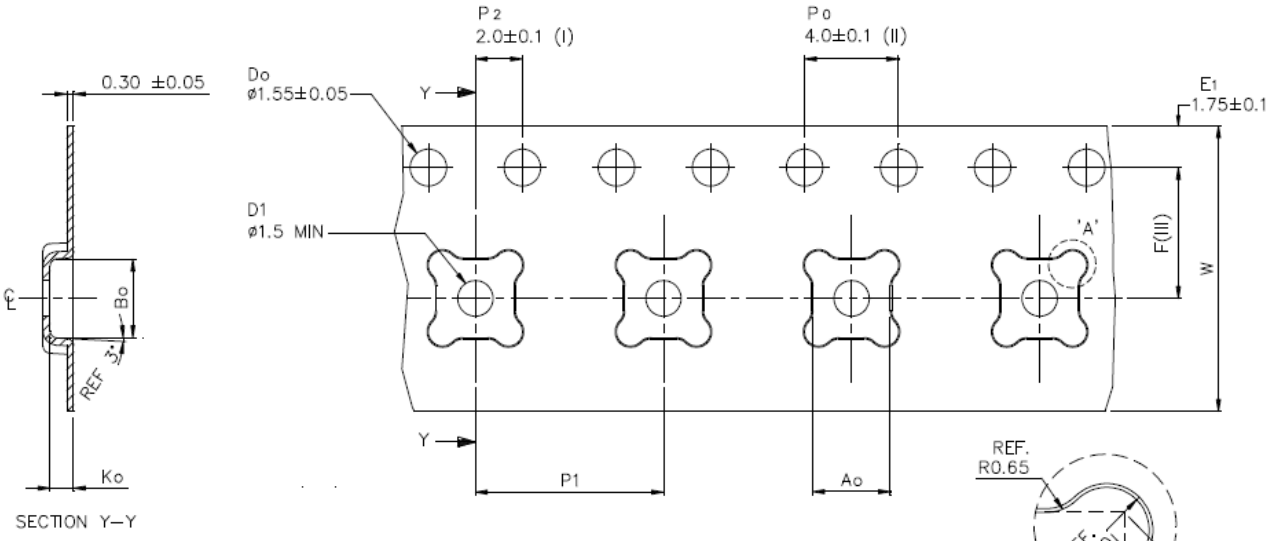
NOTE :

1. REFER TO JEDEC STD: MO-220.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size	Units per Reel	Max Units per Box	Reel & Hub Size (inches)	Trailer A		Leader B		Pocket Tape(mm)	
						Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
16TQFN	16	3x3x0.75mm	5,000	10,000	13/4	42	336	42	336	12	8

16 Lead TQFN Tape and Reel Package



Ao	3.30 + 0.10/−0.15
Bo	3.30 + 0.10/−0.15
Ko	1.00 + 0.25/−0.20
F	5.50 +/−0.10
P1	8.00 +/−0.10
W	12.00 +/−0.30

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Soldering Profile

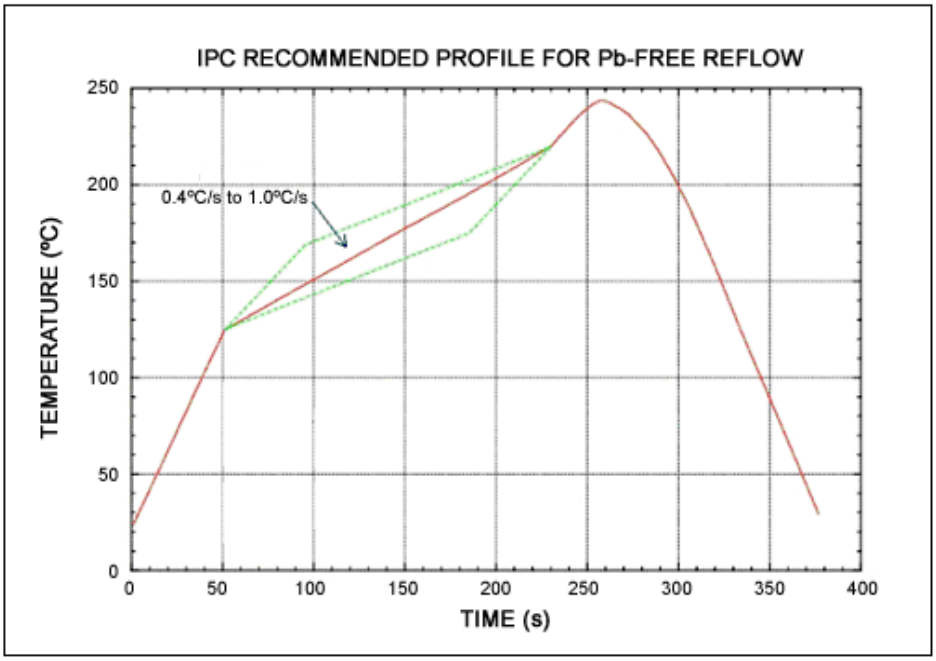


Figure 7. Soldering Profile.

Revision History

Date	Version	Change
10/18/2010	0.16	Updated 32kHz ppm spec
10/13/2010	0.15	Adjusted GreenCLK Error Explained ppm table
9/13/2010	0.13	Added LAN REFCLK to 25MHz_A Swing Feature Modified 25MHz_A Output Diagram
9/10/2010	0.12	25MHz_B voltage swing change