

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

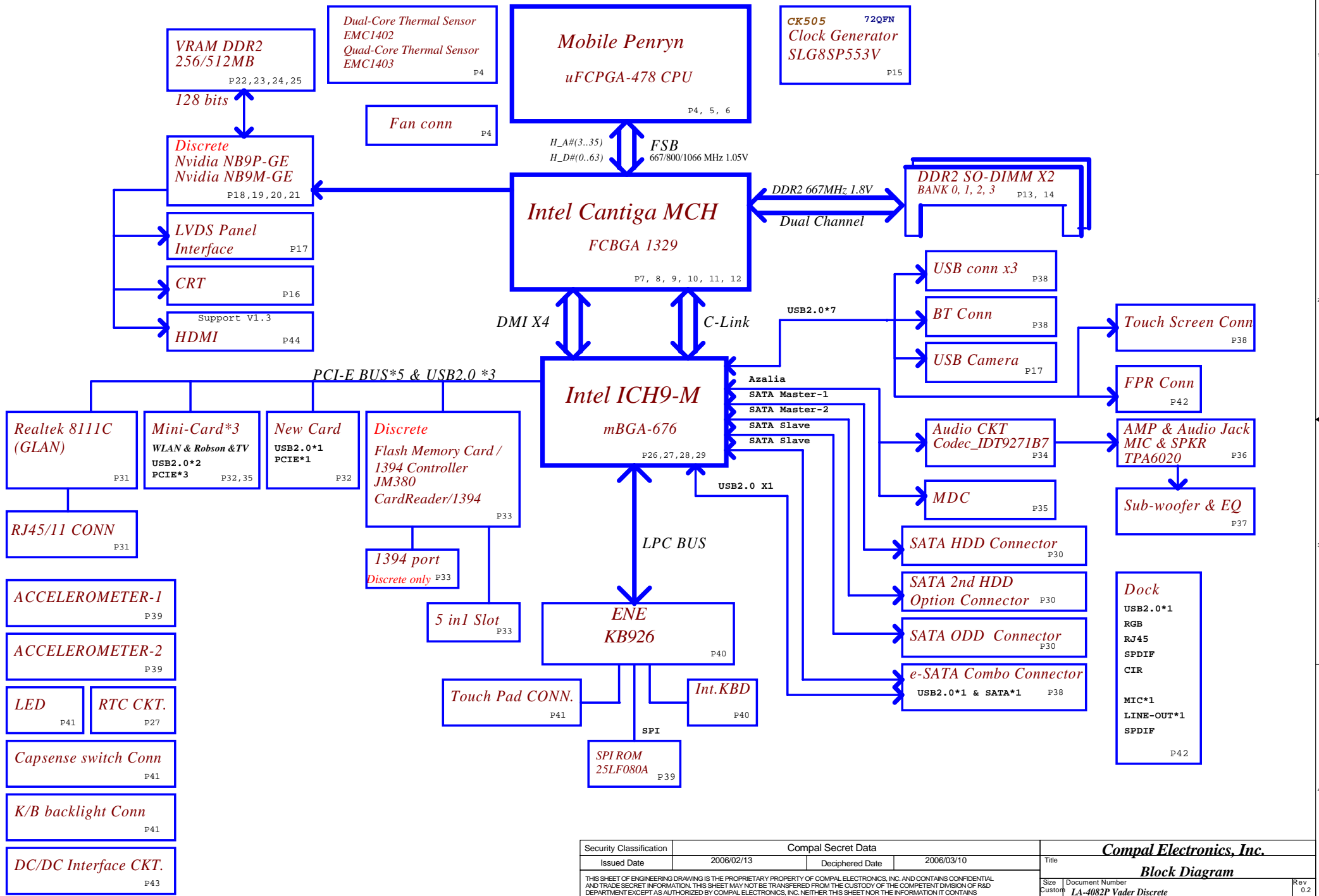
LA-4082P Vader Discrete (NB9P-GS, NB9M-GE)

2007-12-26 Rev 0.4



Security Classification	Compal Secret Data			Title Compal Electronics, Inc.		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Cover Sheet		
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				Custom	LA-4082P Vader Discrete	0.2
Date: Wednesday, December 26, 2007				Sheet	1	of 58

Montevina Consumer Discrete



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Size	Document Number	Date		Rev	
Custom	LA-4082P Vader Discrete	Wednesday, December 26, 2007		0.2	
Date				Sheet 2 of 58	

Voltage Rails O MEANS ON X MEANS OFF

power plane	+B	+5VALW	+1.8V	+5VS
				+3VS
State		+3VALW		+1.5VS
				+0.9V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBus Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Sensor board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
DDC2_CLK DDC2_DATA	NB9M	X	X	X	X	X	X	X	V	X

USB

assignment:

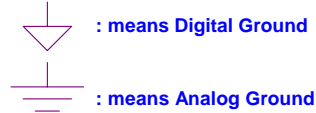
- USB-0 Right side
- USB-1 Right side
- USB-2 Left side(with ESATA)
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express
- USB-10 X
- USB-11 X

PCIe

assignment:

- PCIe-1 TV tuner/WWAN/Robeson
- PCIe-2 X
- PCIe-3 WLAN
- PCIe-4 New Card
- PCIe-5 Card
- PCIe-6 GLAN (Marvell)

Symbol Note :



@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

EC SM Bus1 address

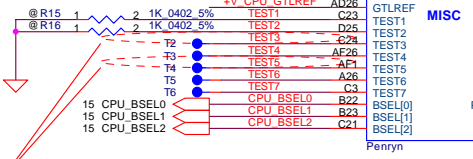
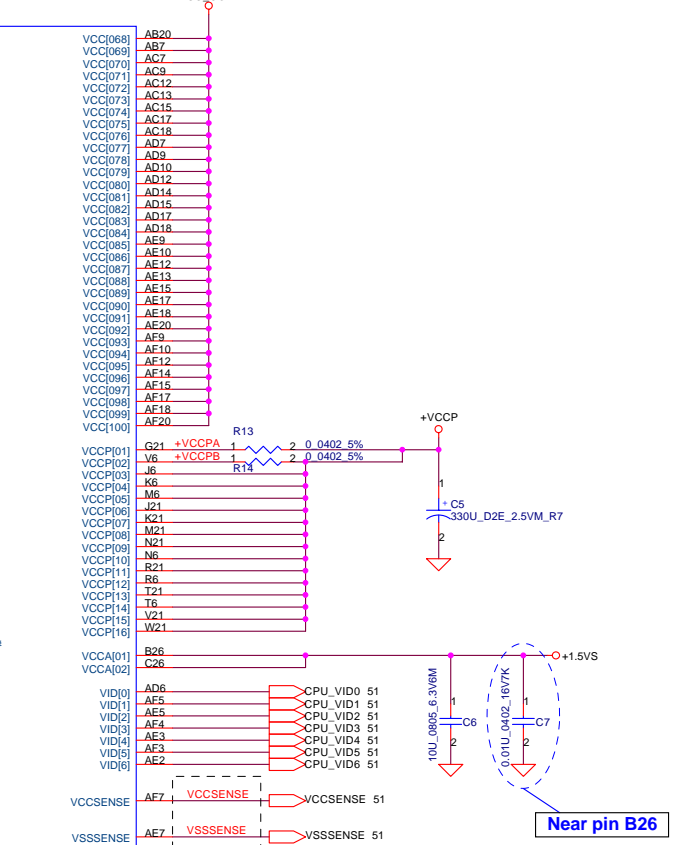
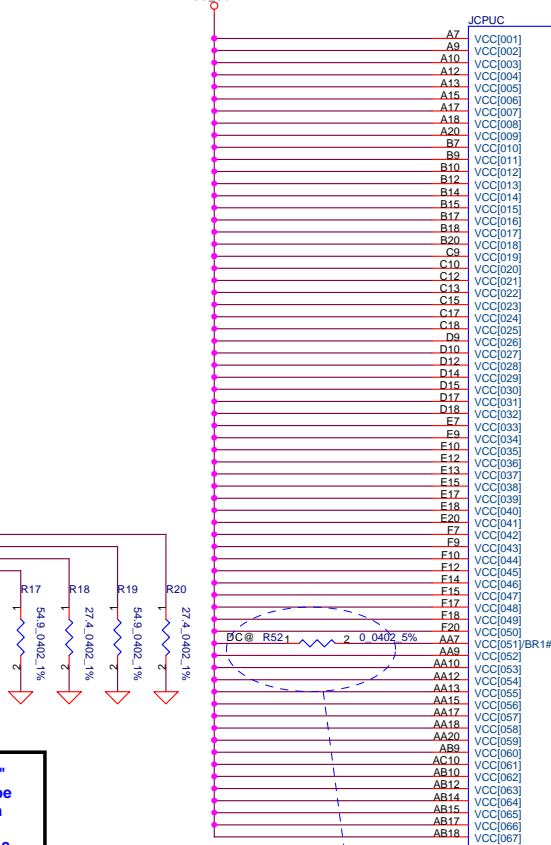
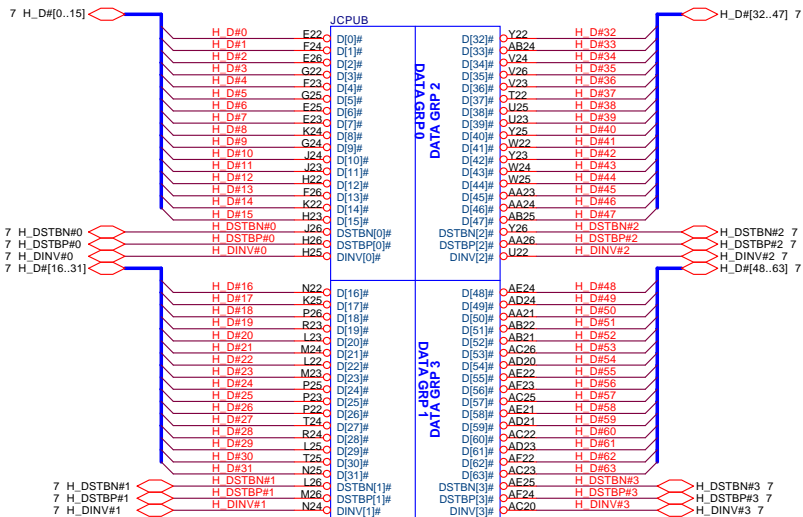
EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X	CPU EMC1402	4CH	1001 1000b
24C16	A0H	1010 000X	VGA	4DH	1001 1010b
CAP BOARD – Cypress	38H				
CAP BOARD – ST	b0H				

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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Size	Document Number	Rev		
Custom	LA-4082P Vader Discrete	0.2		
Date:	Wednesday, December 26, 2007	Sheet	3	of 58

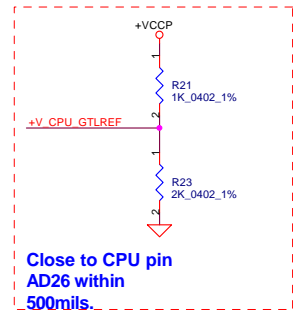


* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

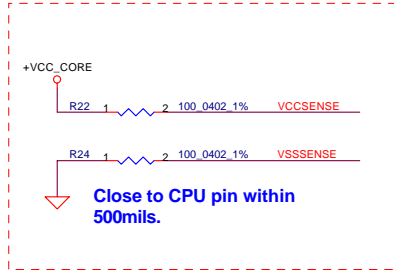
1025 For Support Dual core and Quad core

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

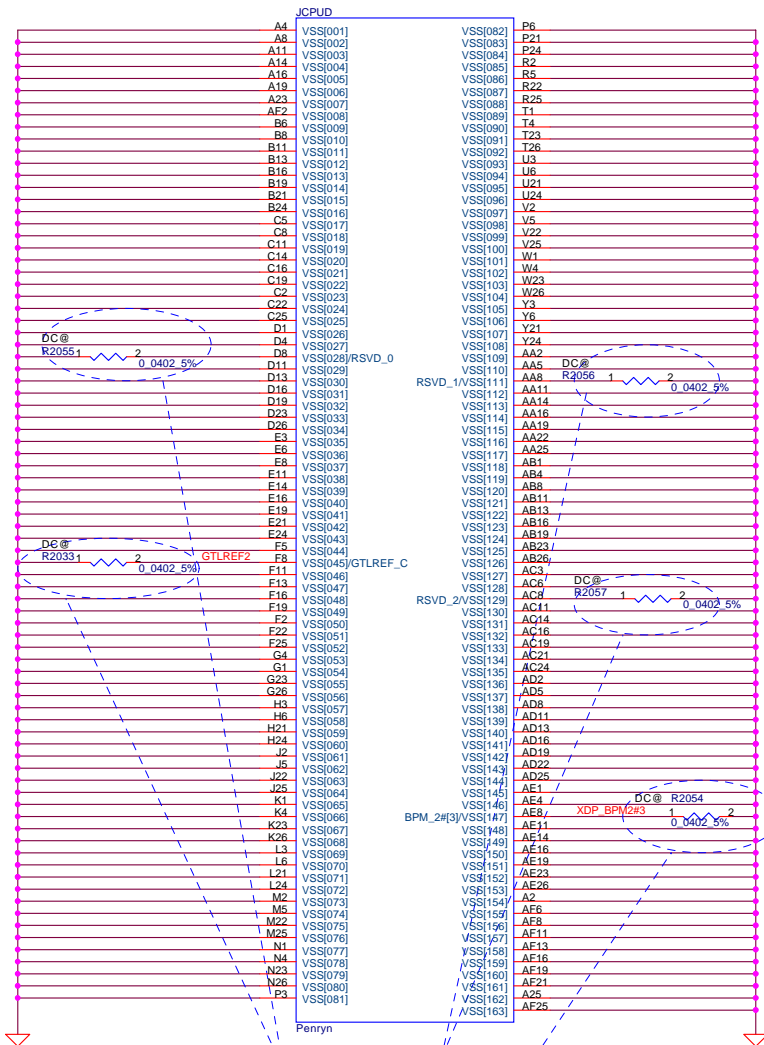


Close to CPU pin AD26 within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

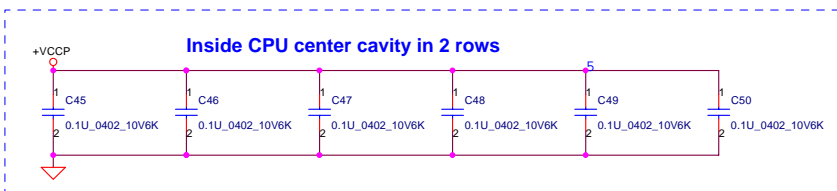
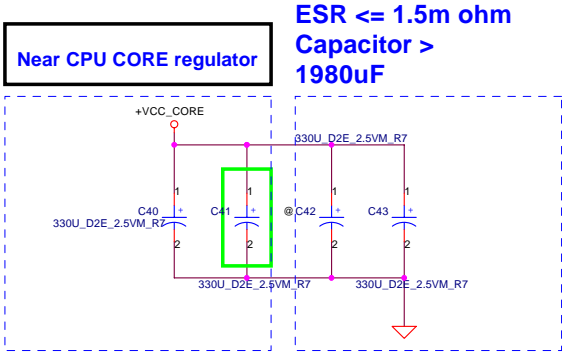
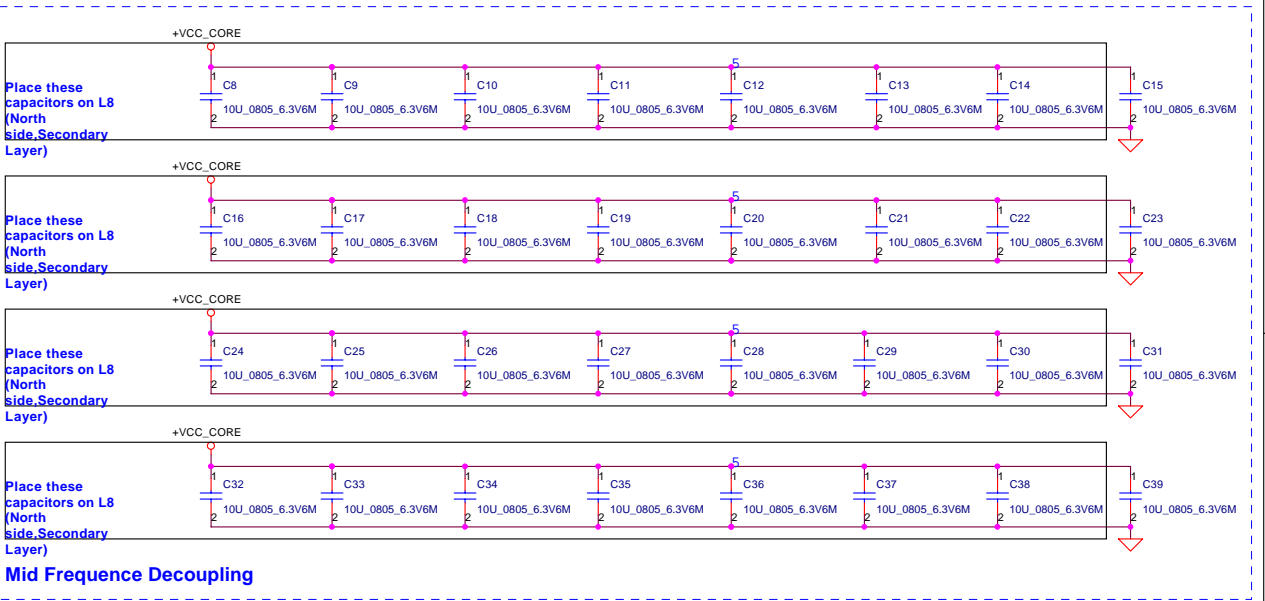


Close to CPU pin within 500mils.

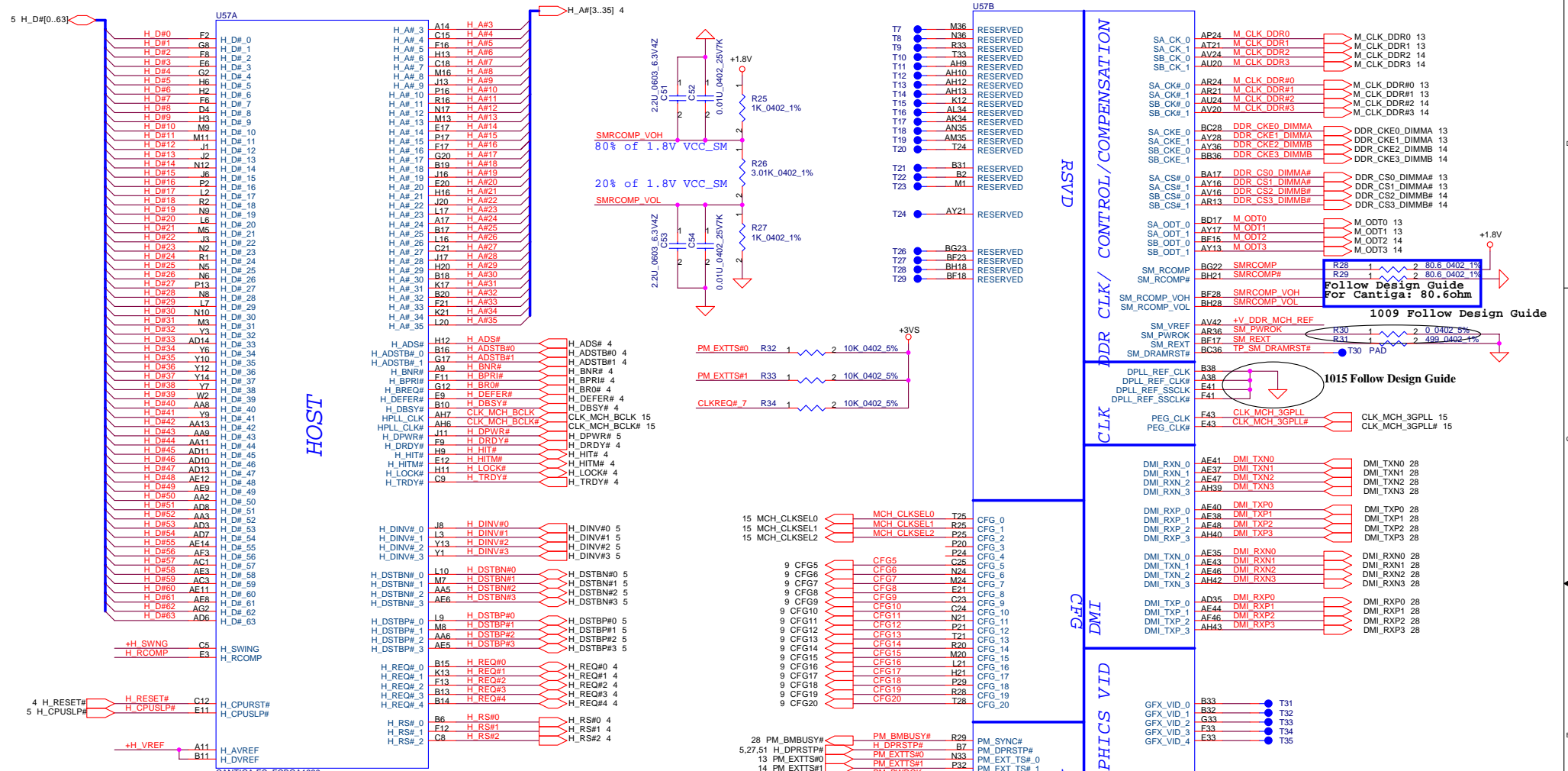


1025 For Support Dual core and Quad core

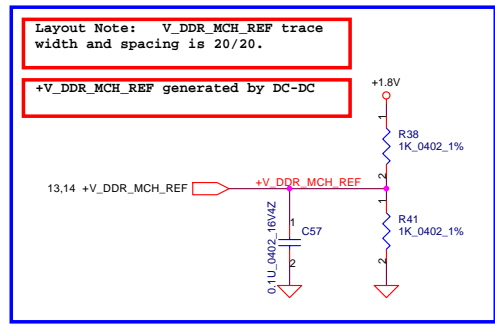
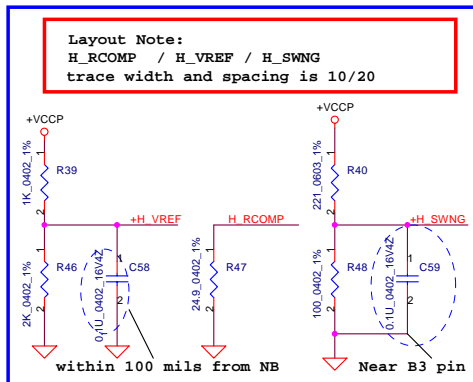
GTLREF2 → GTLREF2 4
 XDP_BPM2#3 → XDP_BPM2#3 4



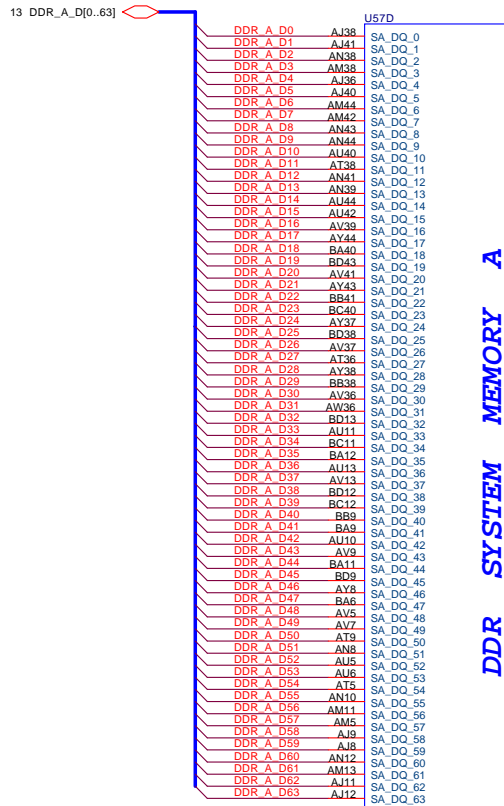
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				Penryn(3/3)-AGTL+/ITP-XDP		
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				Custom	LA-4082P Vader Discrete	0.2
				Date:	Wednesday, December 26, 2007	Sheet 6 of 58



layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

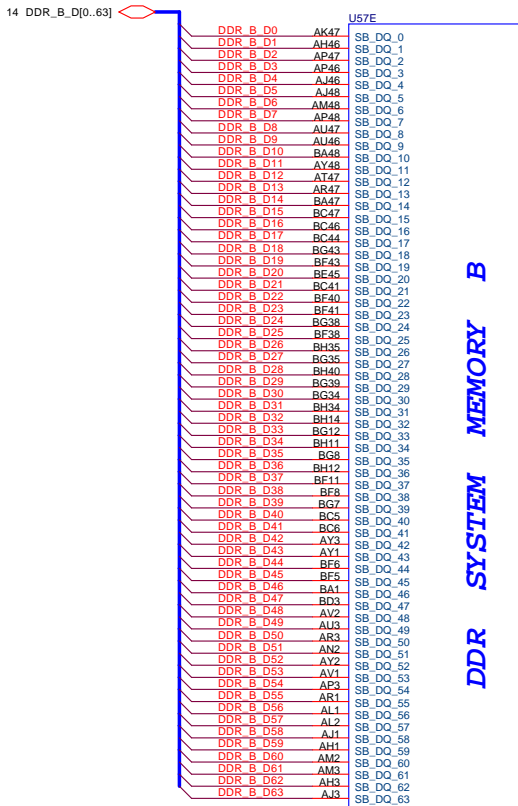


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Size	Document Number	Rev	Date		
Custom	LA-4082P Vader Discrete	0.2	Wednesday, December 26, 2007 [Sheet 7 of 58]		



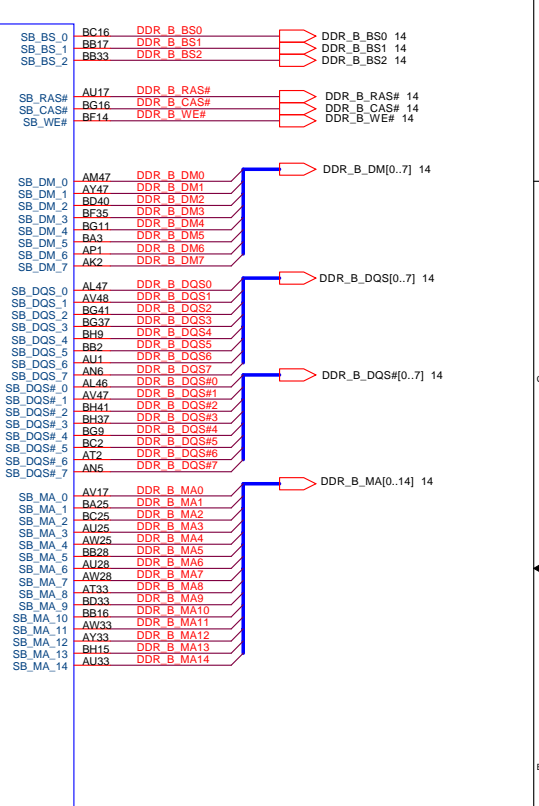
DDR SYSTEM MEMORY A

CANTIGA ES_FCBGA1329

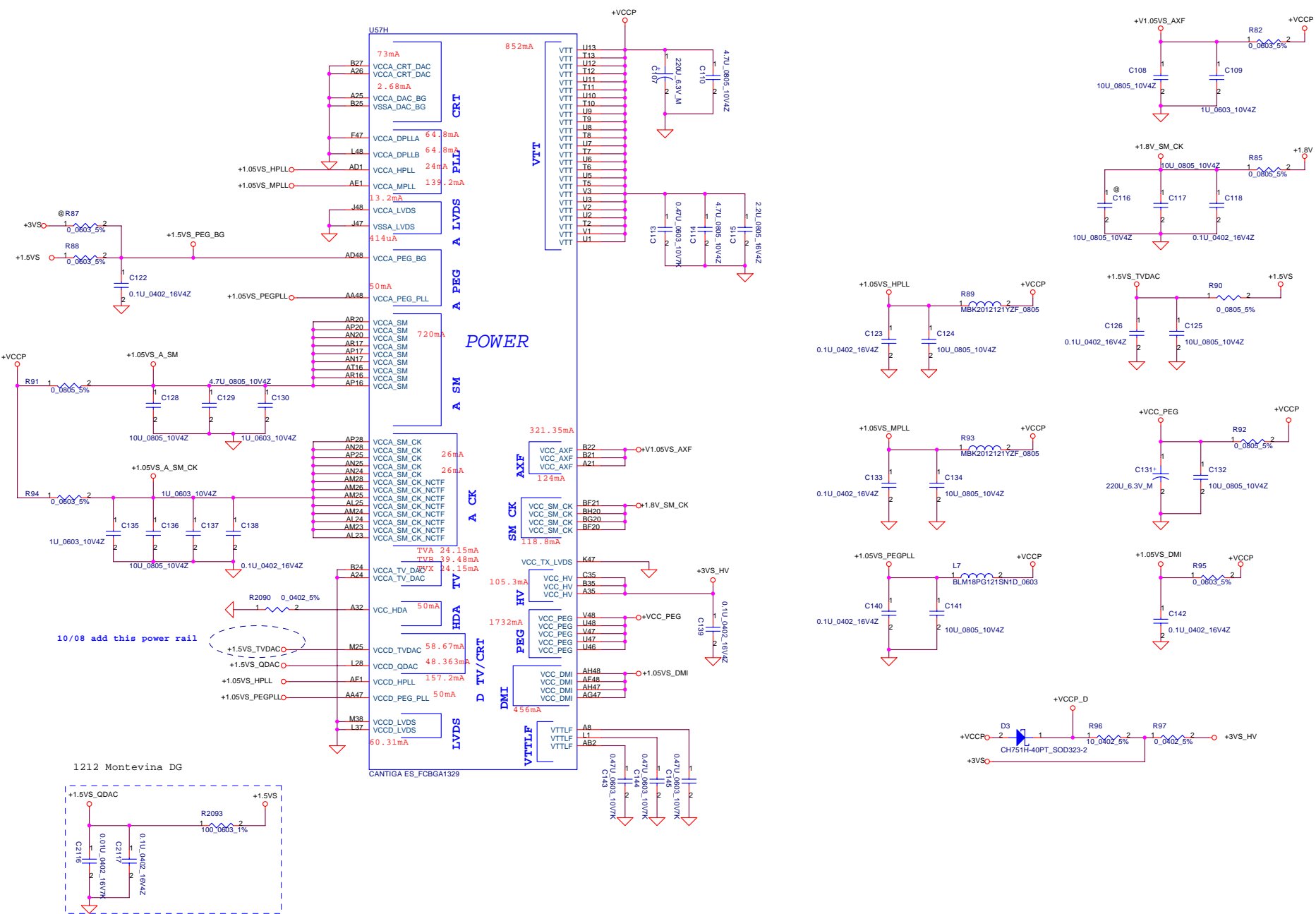


DDR SYSTEM MEMORY B

CANTIGA ES_FCBGA1329

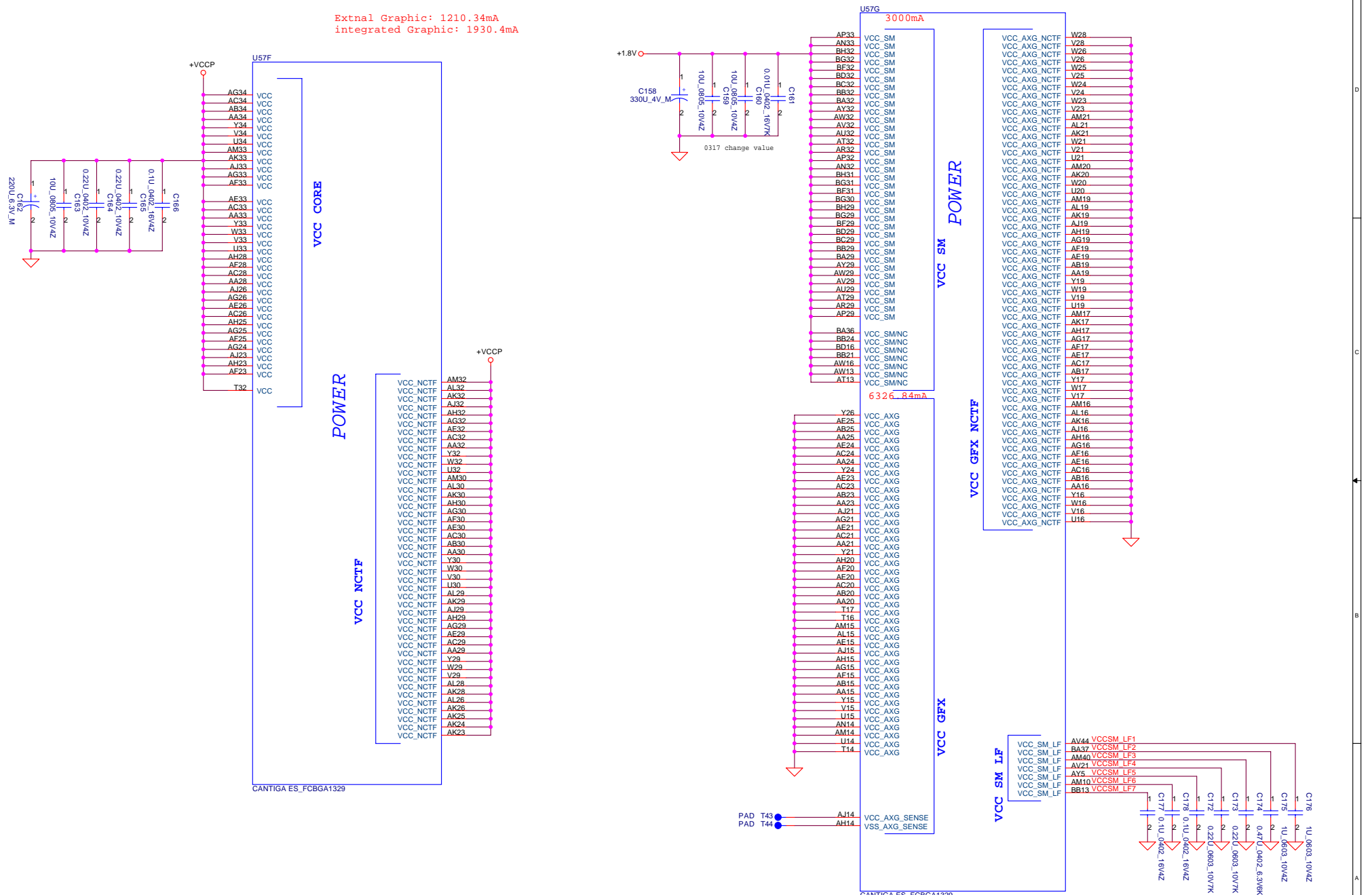


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Date:	Wednesday, December 26, 2007	Sheet	8	of	58

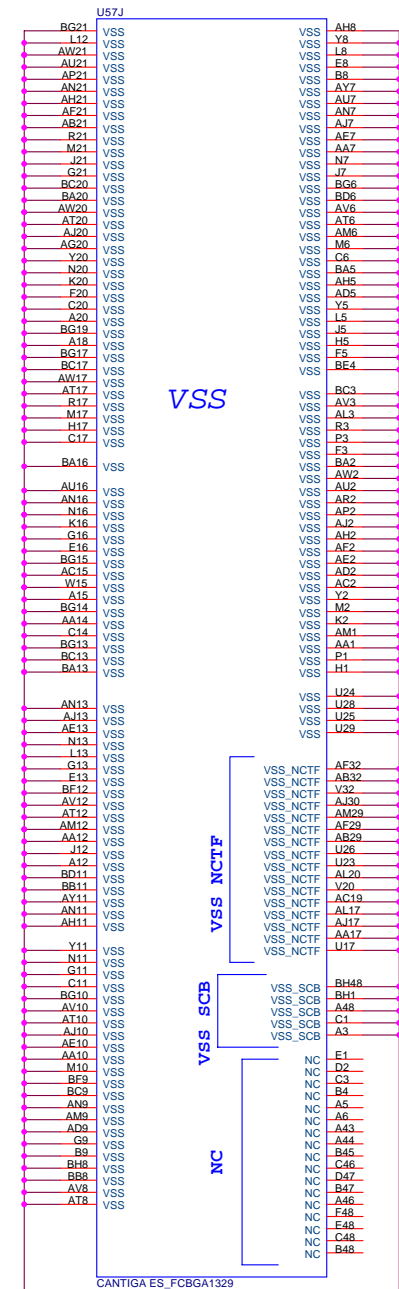
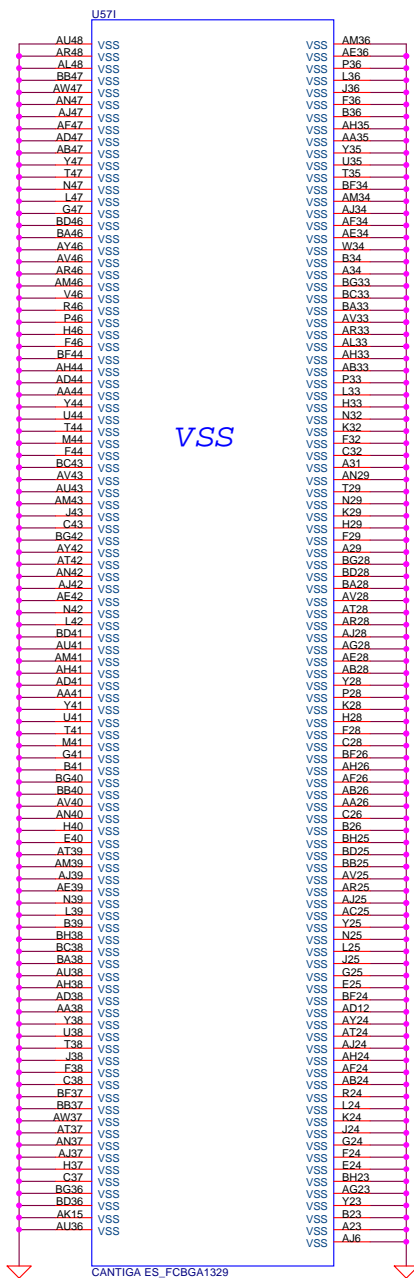


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Title	Cantiga(4/6)-PWR			
Size	Document Number	Rev		
Custom	LA-4082P Vader Discrete	0.2		
Date:	Wednesday, December 26, 2007	Sheet	10	of 58

Extenal Graphic: 1210.34mA
 integrated Graphic: 1930.4mA

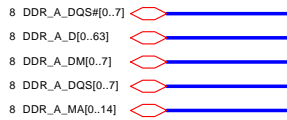


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Size	Document Number	Rev	Date: Wednesday, December 26, 2007 11 of 58		
Custom	LA-4082P Vader Discrete	0.2			

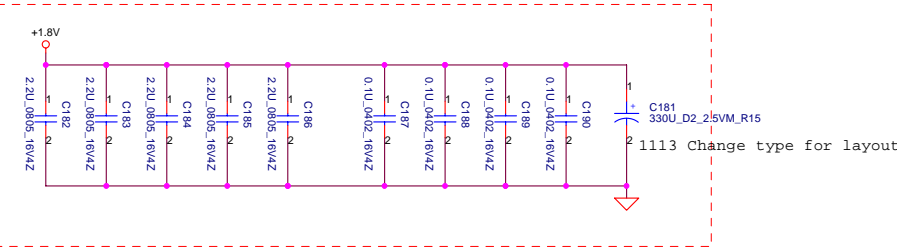


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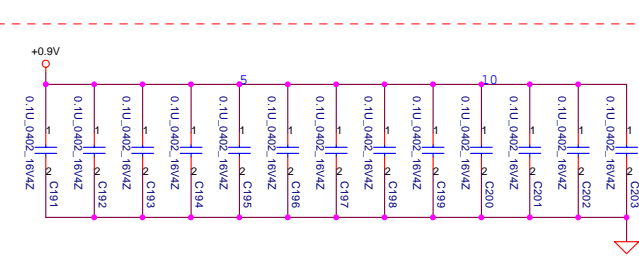
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Cantiga(6/6)-PWR/GND			
Size	Document Number	Rev	
Custom	LA-4082P Vader Discrete	0.2	
Date:	Wednesday, December 26, 2007	Sheet	12 of 58



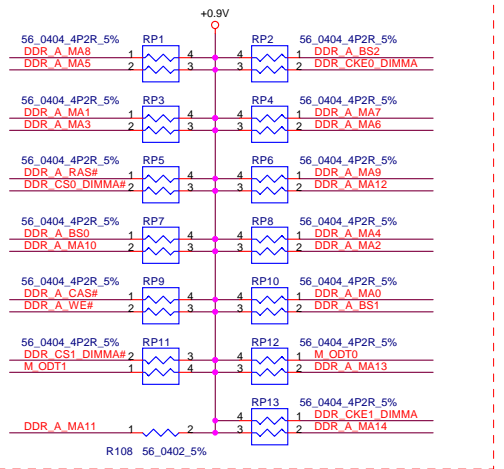
Layout Note:
Place near JP3



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

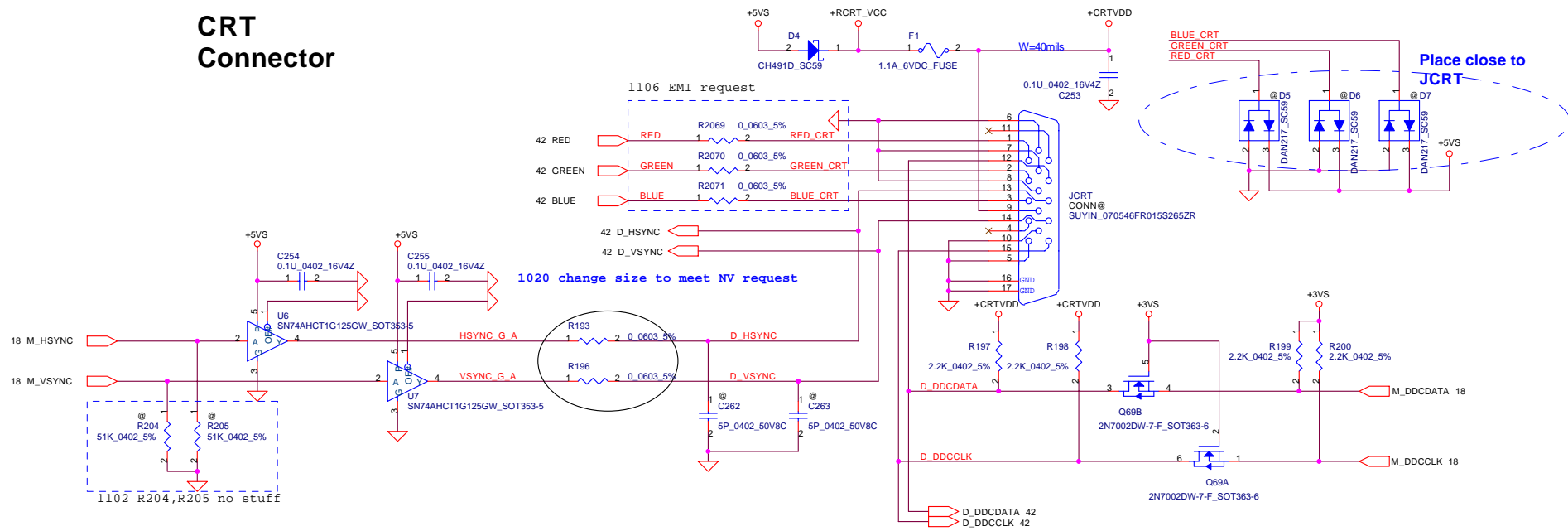


Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



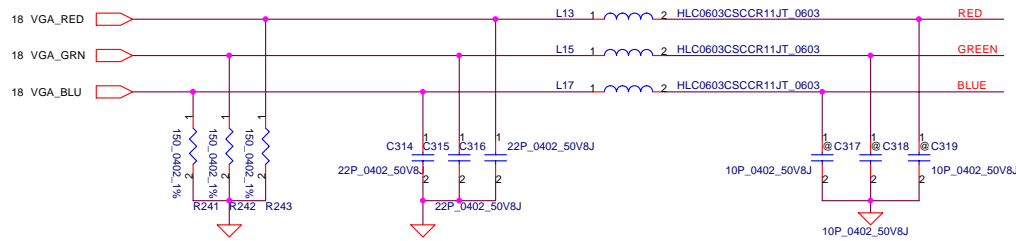
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Size	Document Number	Rev	0.2
Custom	LA-4082P Vader Discrete	Date:	Wednesday, December 26, 2007
Sheet		13 of 58	

CRT Connector

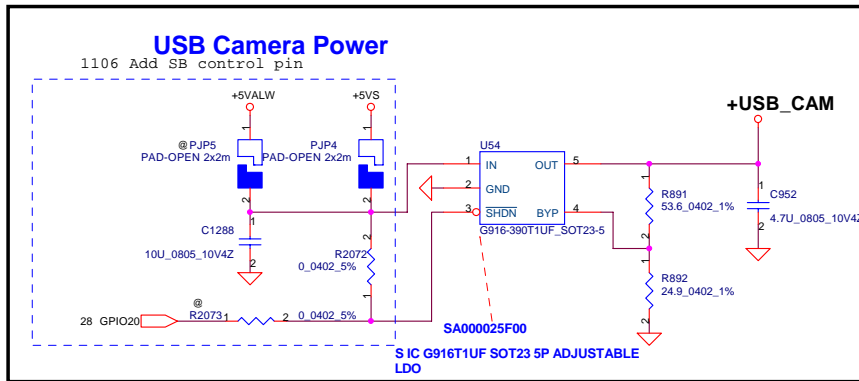
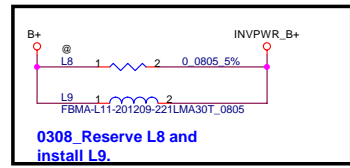
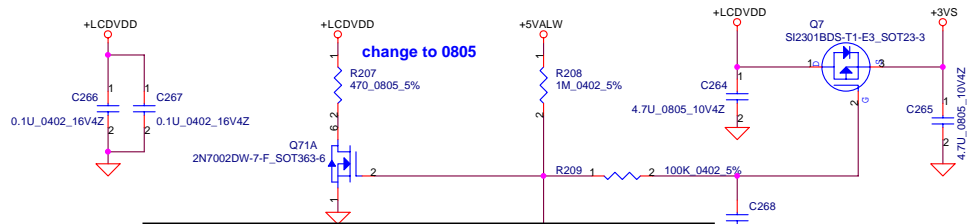
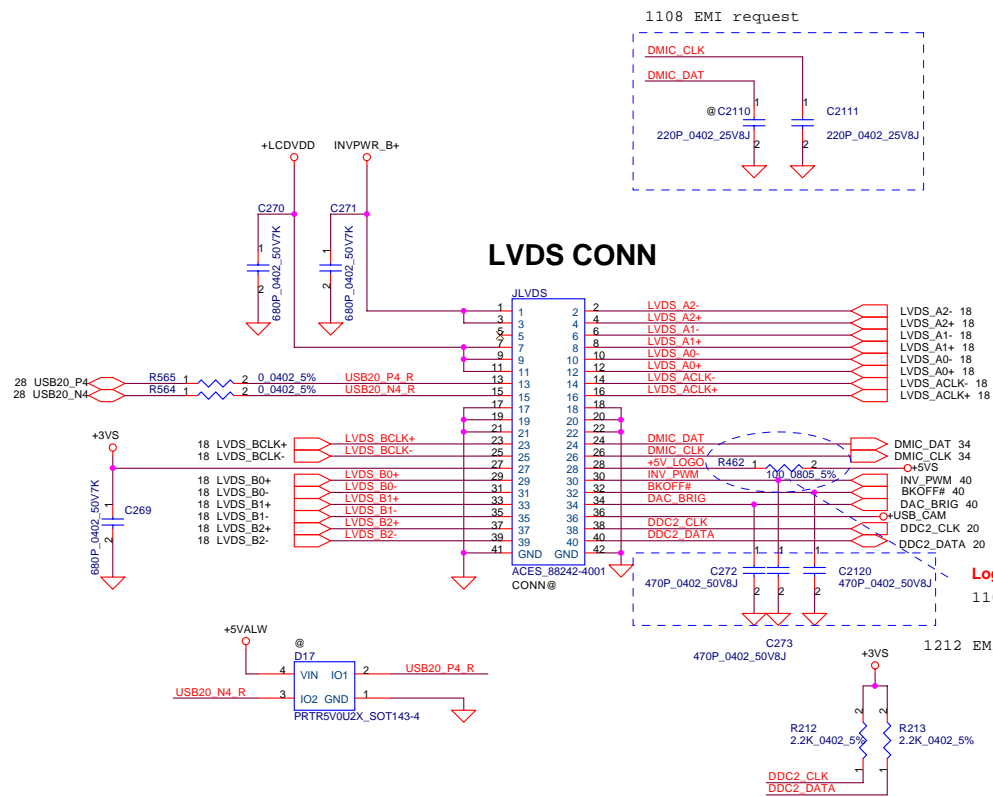


CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.



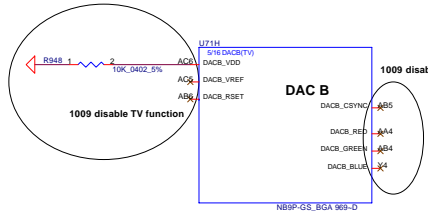
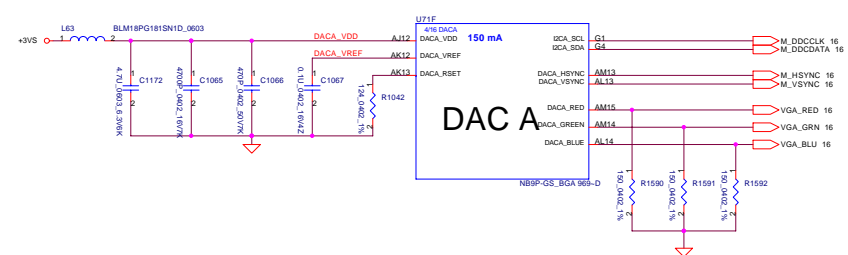
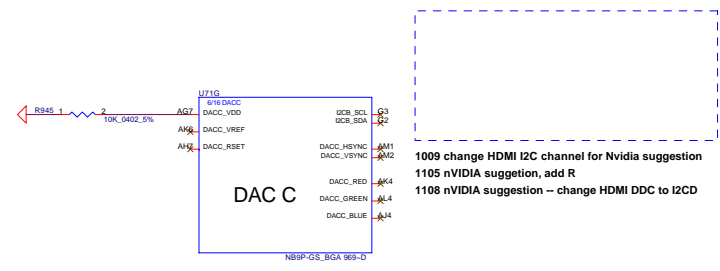
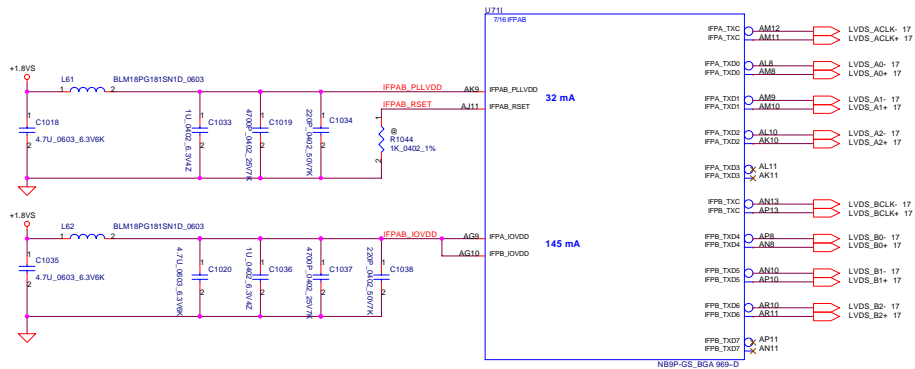
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				LA-4082P Vader Discrete		0.2
				Date:	Wednesday, December 26, 2007	Sheet 16 of 58



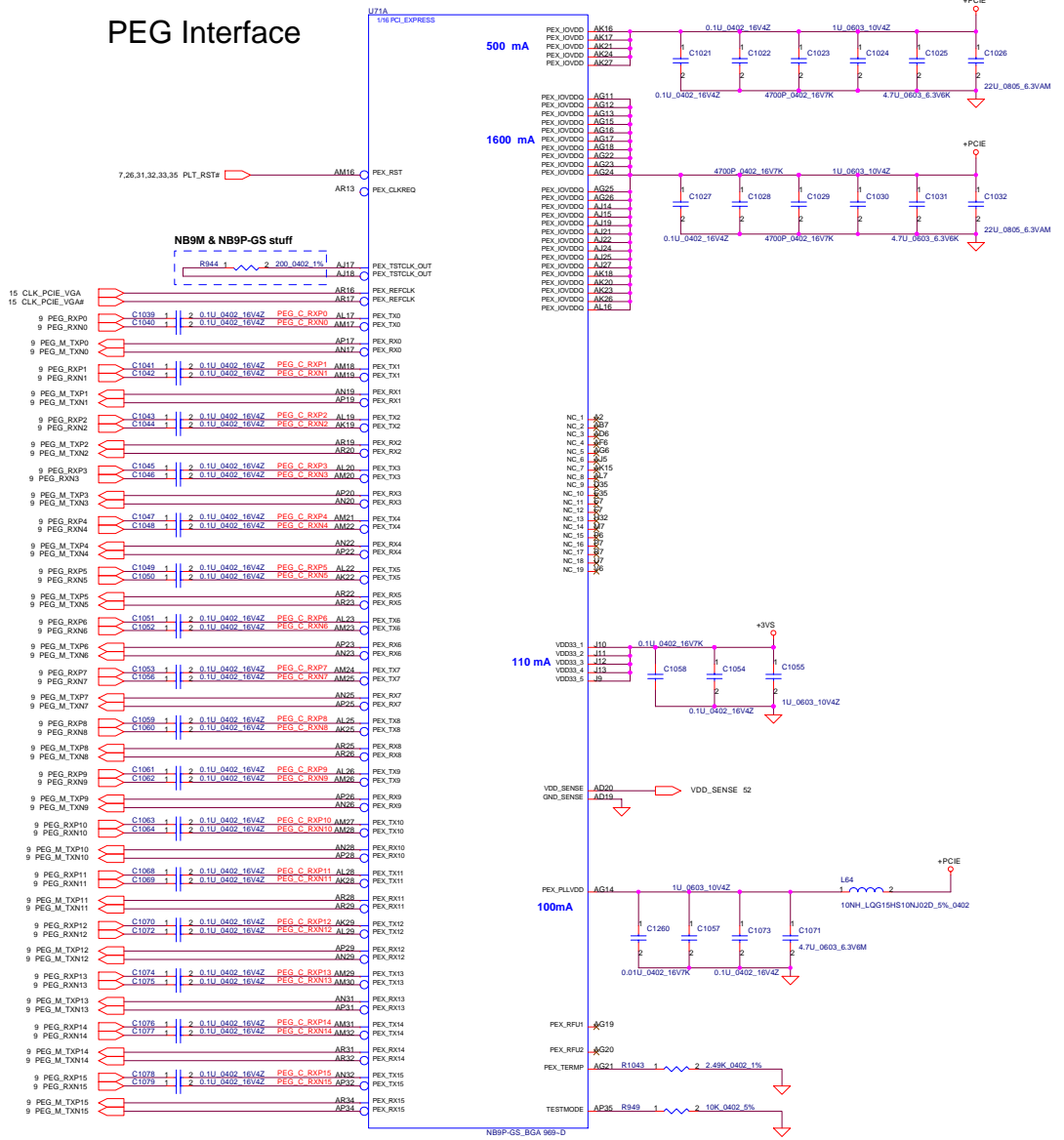
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Document Number		LCD CONN.	
Size	Custom	Rev	0.2
Date:	Wednesday, December 26, 2007	Sheet	17 of 58

LVDS & DAC Interface



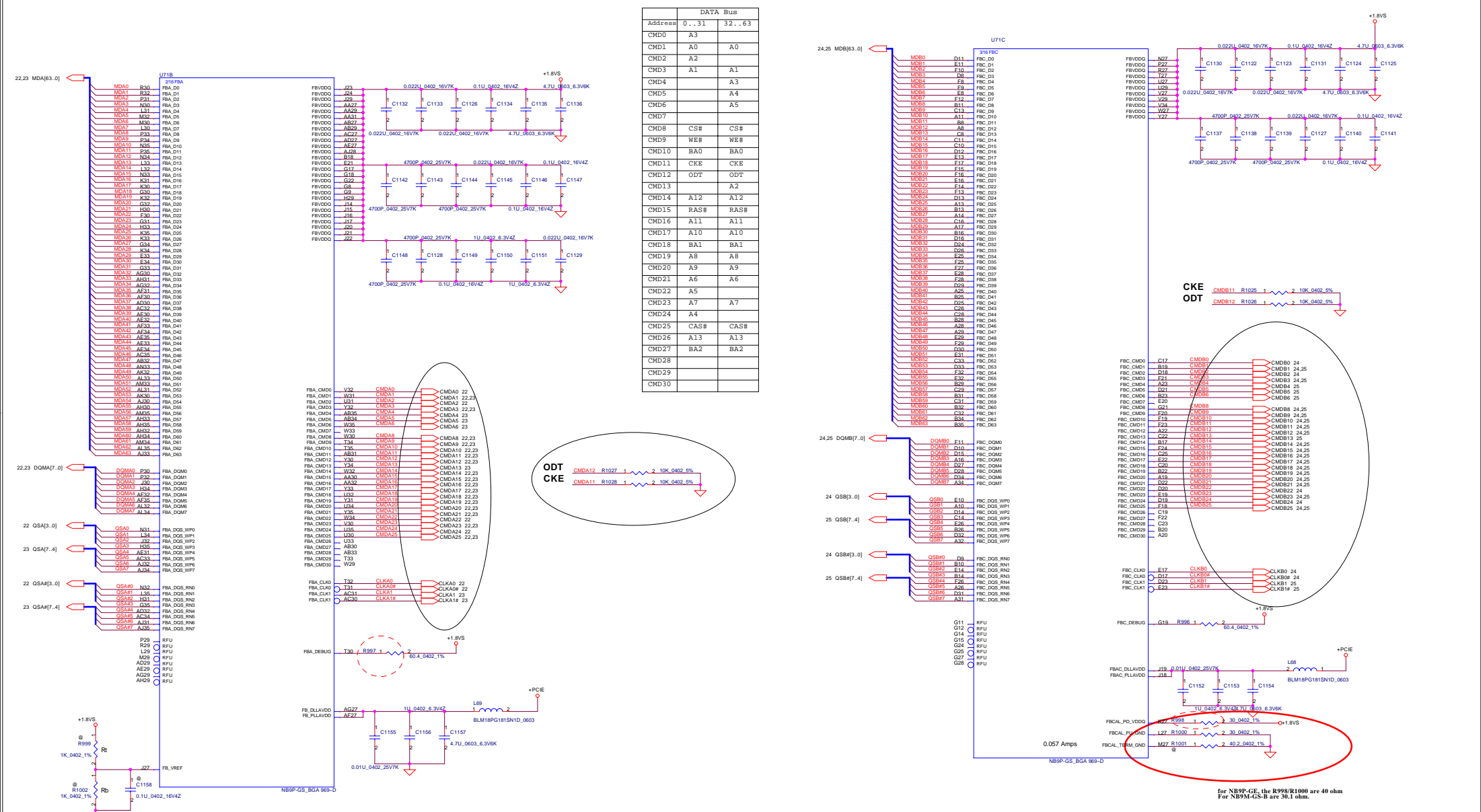
PEG Interface



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Size	Document Number	Rev	0.2
Customer	LA-4082P Vader Discrete	Date	Wednesday, December 26, 2007 Sheet 18 of 58

Compal Electronics, Inc.
PEG & LVDS & DAC

VRAM Interface



ODT CKE
 CMDA11 R1027 1 2 10K 0402 5%
 CMDA11 R1028 1 2 10K 0402 5%

For NB9P-GE, the R998/R1000 are 40 ohm
 For NB9M-GS-B are 30.1 ohm.

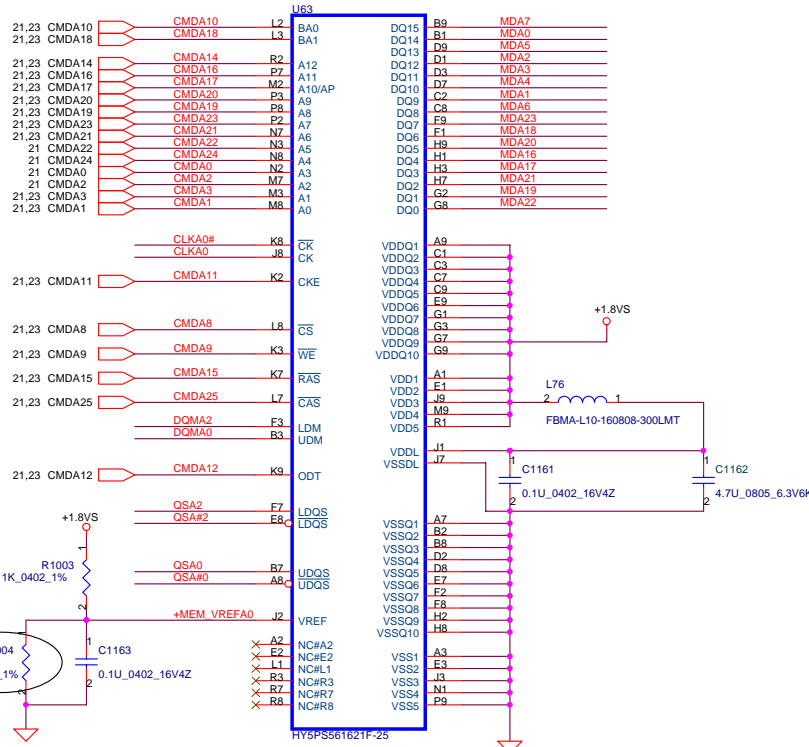
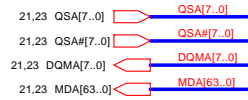
VREF = 0.5 * FBVDDQ
 DDR2: 1.0V = 2.0V * 1K/(1K + 1K)
 FBVREF = FBVDDQ * Rb/(Rt + Rb)

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VRAM Interface	
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Doc No	LA-4082P_Vader Discrete
Rev	0.2
Date	Wednesday, December 26, 2007
Sheet	21 of 58

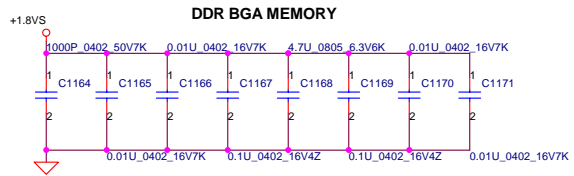
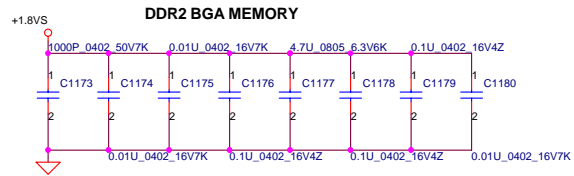
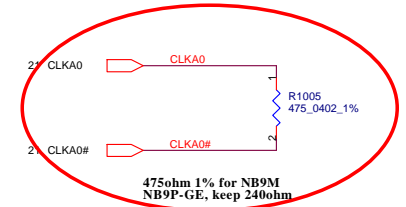
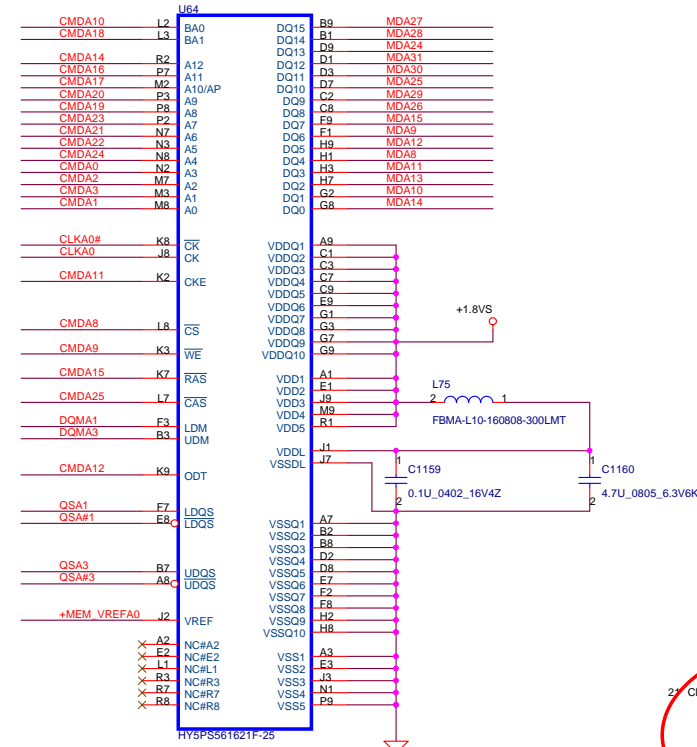
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB

32Mx16 DDR2 400MHz *4==>256MB



Vref= 0.5* 1.8V for NB9M, R1004=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1004=1K ohm

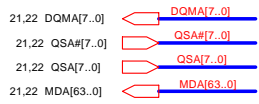


	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

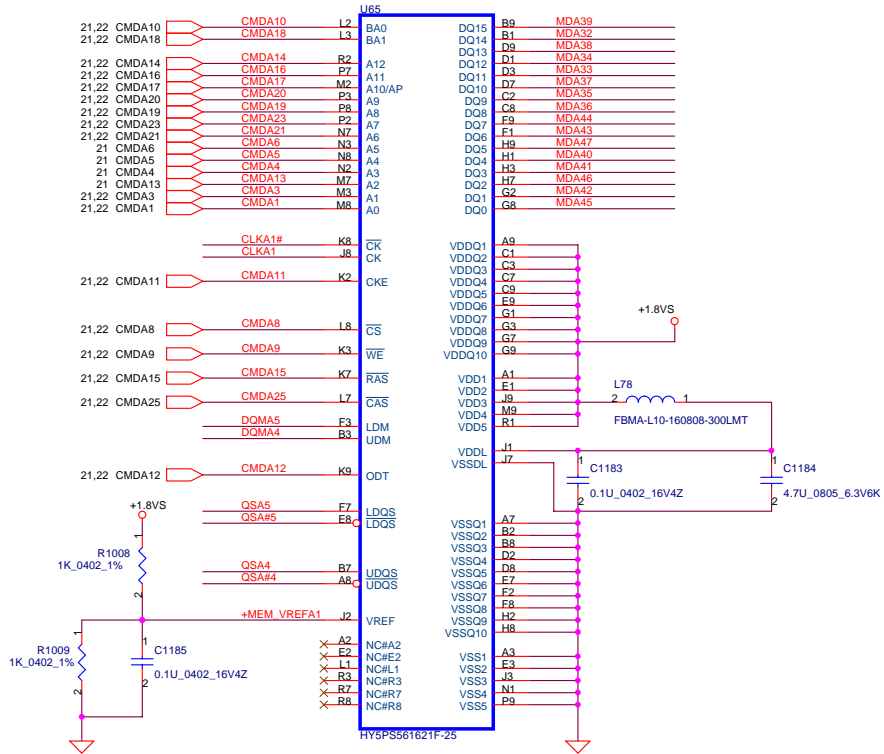
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB

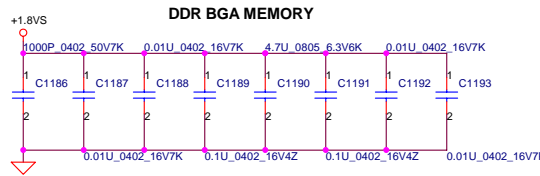
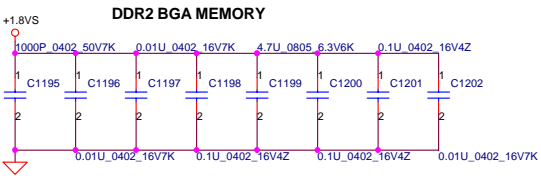
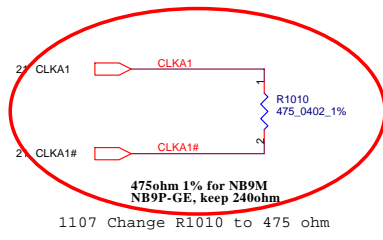
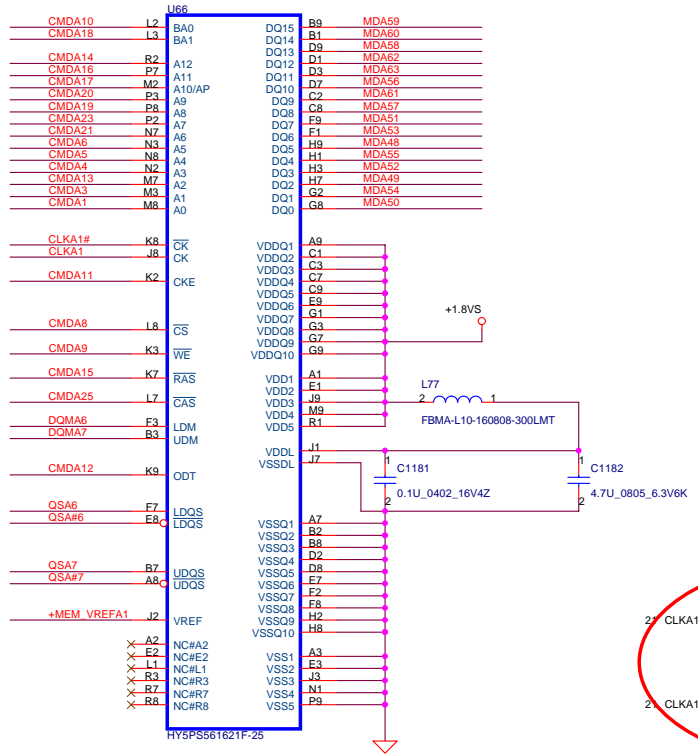
32Mx16 DDR2 400MHz *4==>256MB



Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



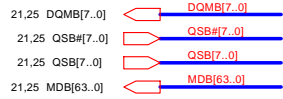
Vref= 0.5* 1.8V for NB9M, R1009=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1009=1K ohm



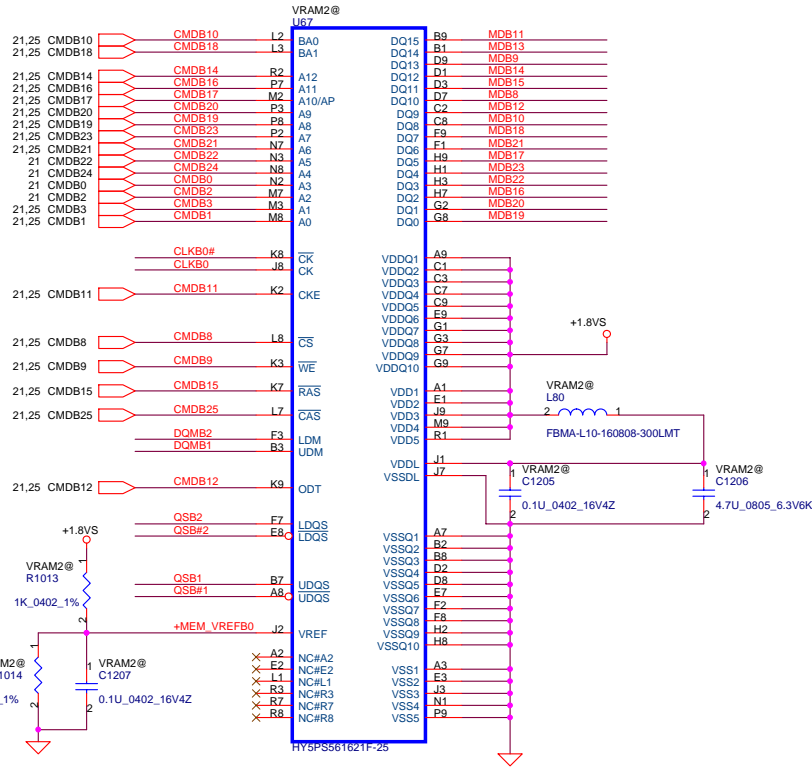
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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				Size	Document Number
Date:	Wednesday, December 26, 2007	Sheet	23	of	58

VRAM DDR2 chips (256MB & 512MB)

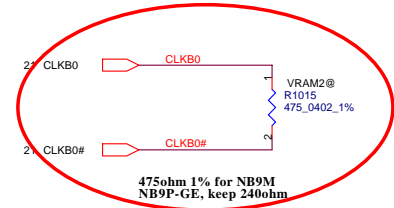
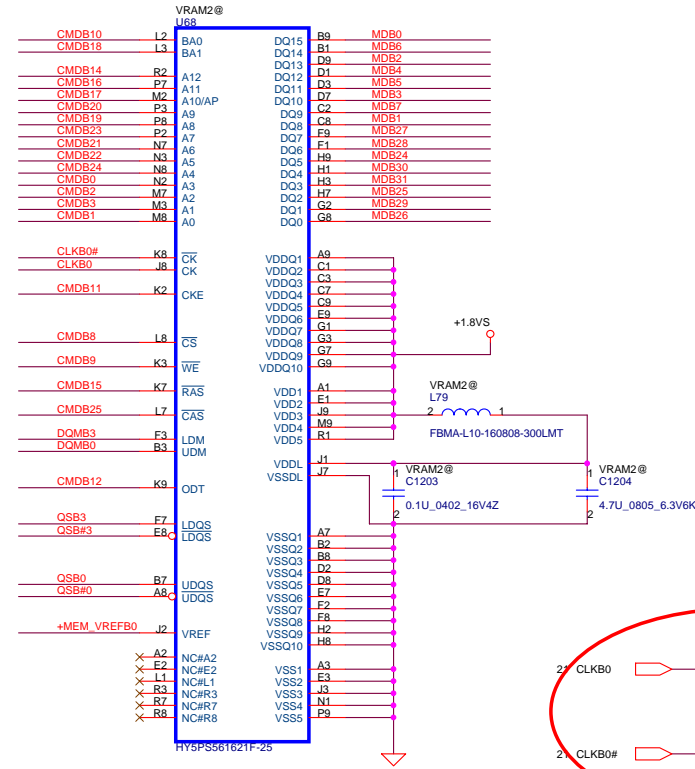
32Mx16 DDR2 400MHz *8==>512MB



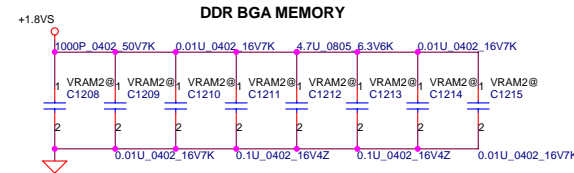
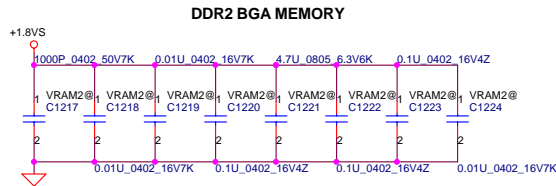
	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



Vref= 0.5* 1.8V for NB9M, R1014=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1014=1K ohm



1107 Change R1015 to 475 ohm



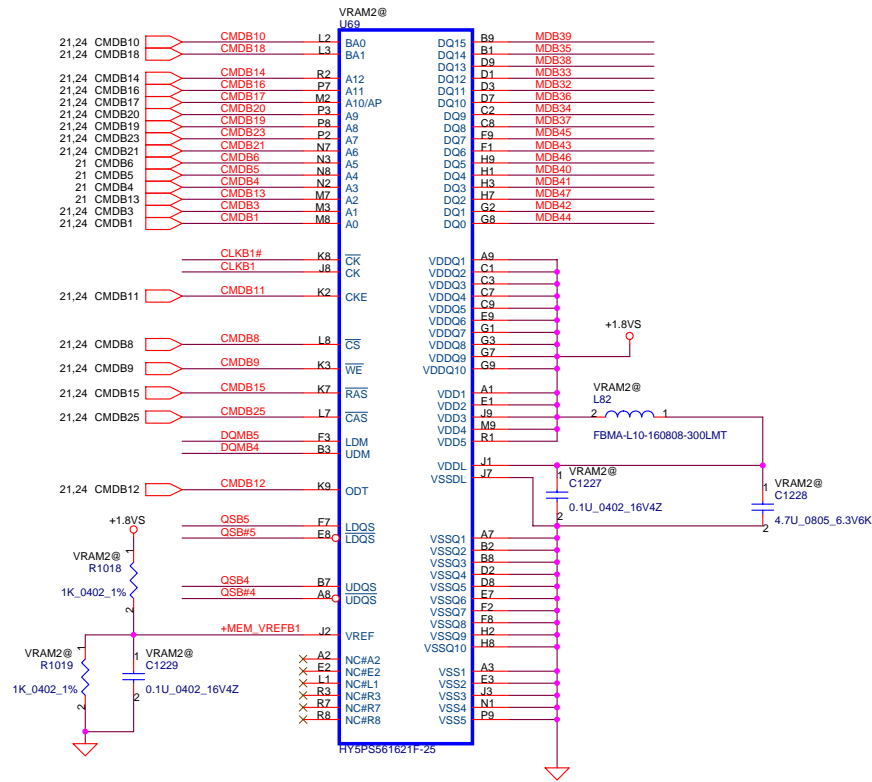
Security Classification	Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.
				CHANNEL B EXT. 256M 1
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				Date: Wednesday, December 26, 2007 Sheet 24 of 58

VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB

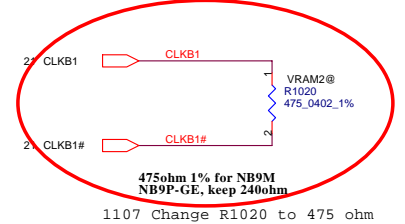
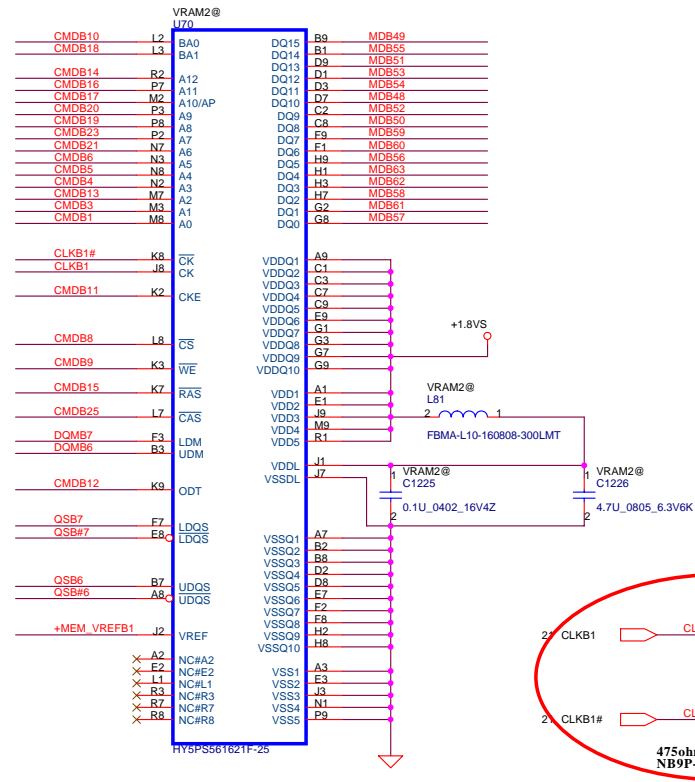


		DATA Bus	
Address	0..31	32..63	
CMD0	A3		
CMD1	A0	A0	
CMD2	A2		
CMD3	A1	A1	
CMD4		A3	
CMD5		A4	
CMD6		A5	
CMD7			
CMD8	CS#	CS#	
CMD9	WE#	WE#	
CMD10	BA0	BA0	
CMD11	CKE	CKE	
CMD12	ODT	ODT	
CMD13		A2	
CMD14	A12	A12	
CMD15	RAS#	RAS#	
CMD16	A11	A11	
CMD17	A10	A10	
CMD18	BA1	BA1	
CMD19	A8	A8	
CMD20	A9	A9	
CMD21	A6	A6	
CMD22	A5		
CMD23	A7	A7	
CMD24	A4		
CMD25	CAS#	CAS#	
CMD26	A13	A13	
CMD27	BA2	BA2	
CMD28			
CMD29			
CMD30			

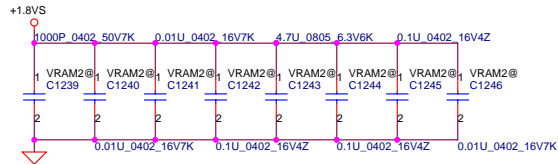


Vref= 0.5* 1.8V for NB9M, R1019=1K ohm

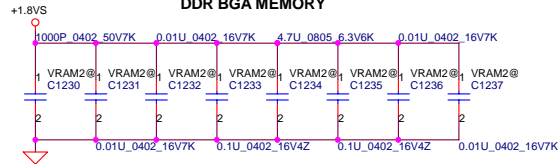
Vref= 0.5* 1.8V for NB9P-GS/GE2, R1019=1K ohm



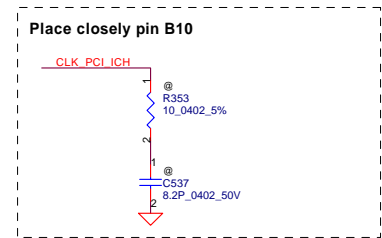
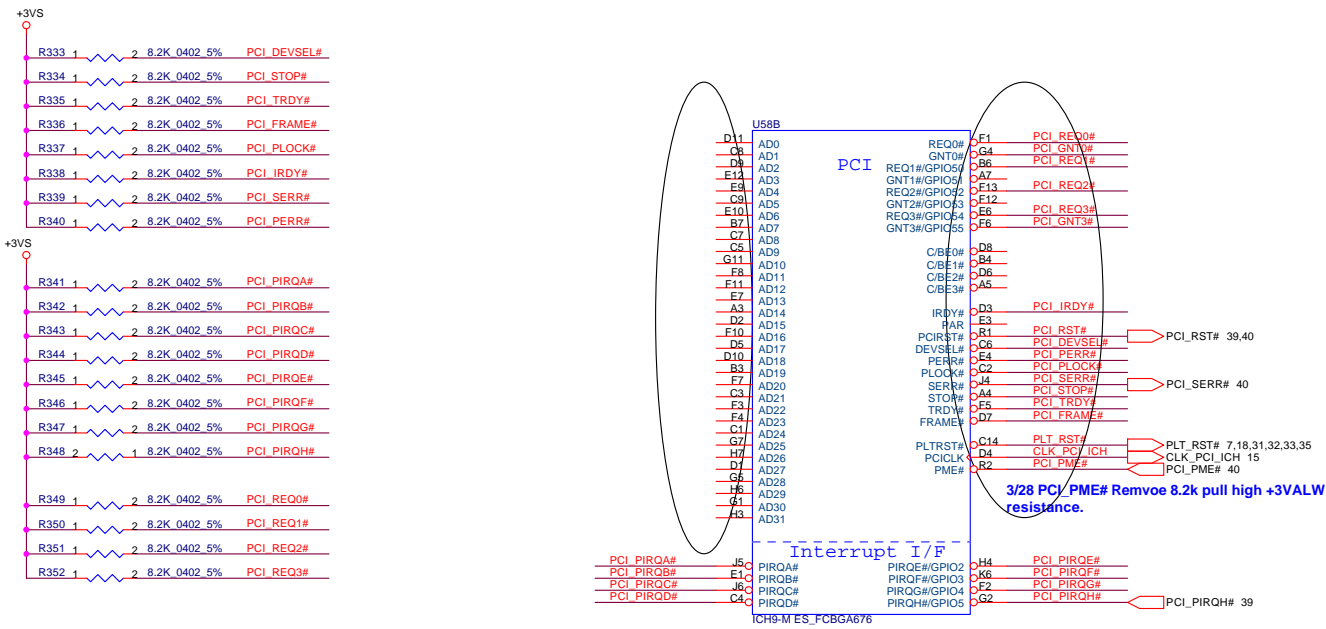
DDR2 BGA MEMORY



DDR BGA MEMORY



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Issued Date	2006/02/13	Deciphered Date	2006/03/10	
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Title			Compal Electronics, Inc.	
Size			CHANNEL B EXT. 256M 2	
Customer	Document Number		Rev	
LA-4082P	Vader Discrete		0.2	
Date:	Wednesday, December 26, 2007	Sheet	25	of 58

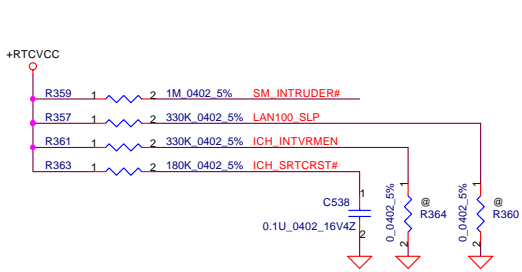


A16 swap override Strap

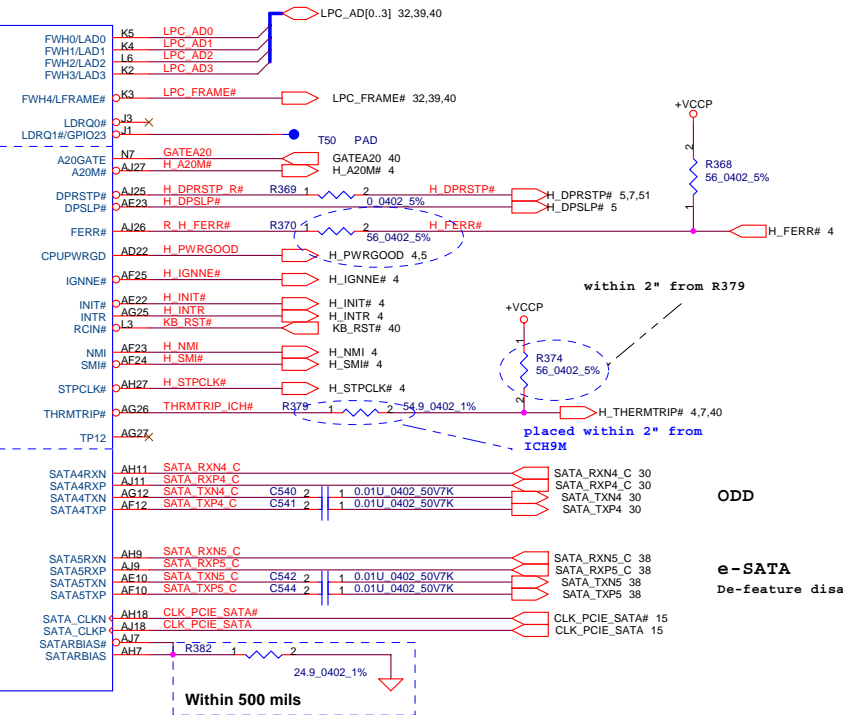
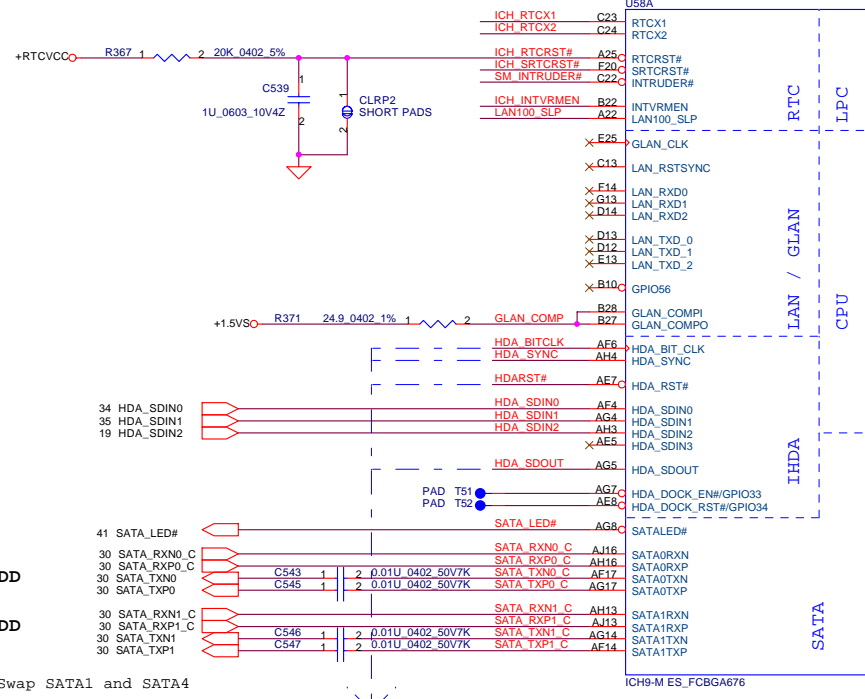
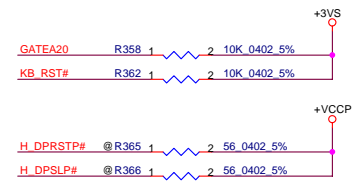
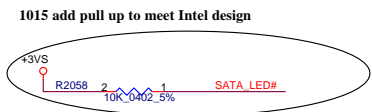
PCI_GNT3#	Low= A16 swap override Enble High= Default *
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Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

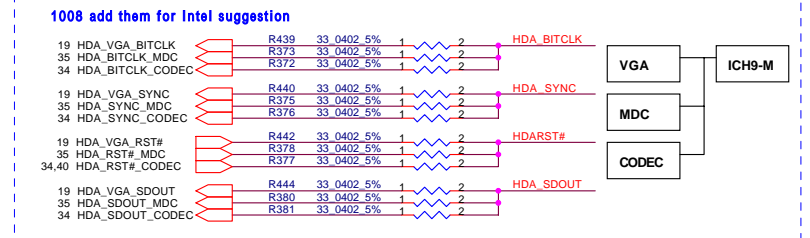
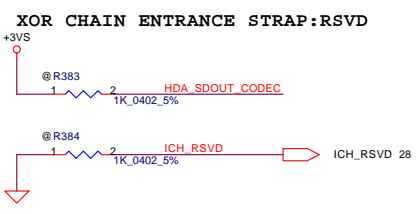


ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

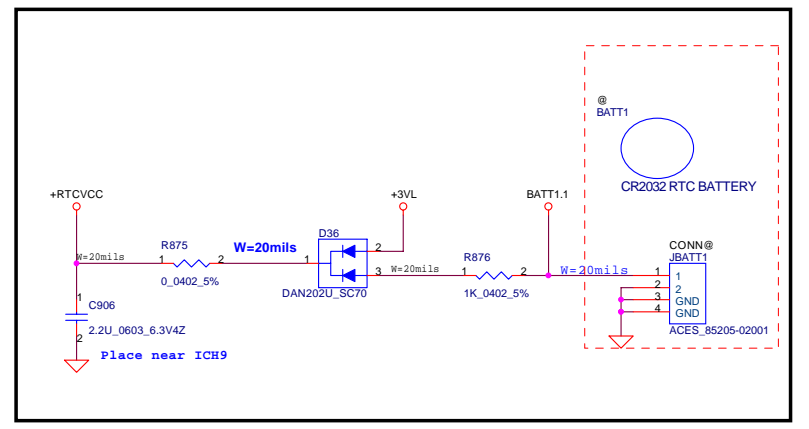
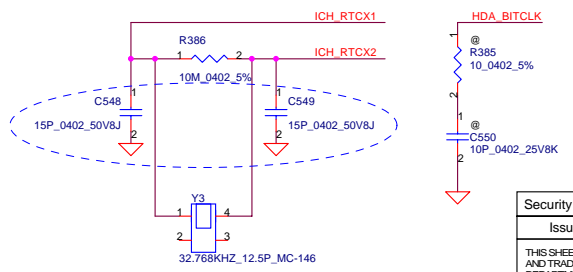


P- HDD
S- HDD
1212 Swap SATA1 and SATA4

ODD
e-SATA
De-feature disable

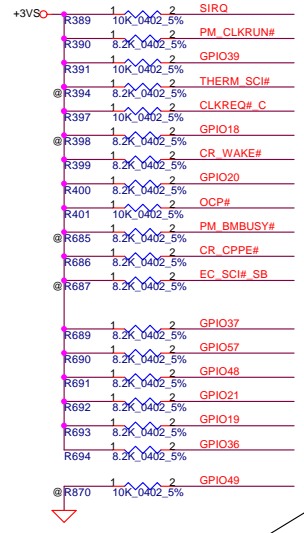


ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

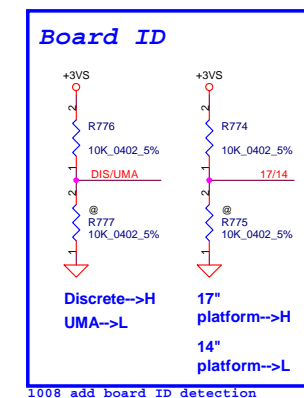
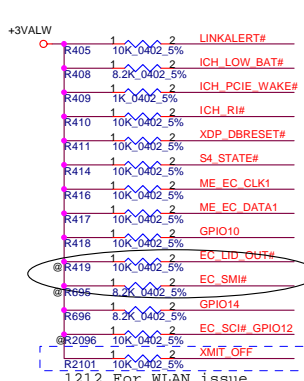


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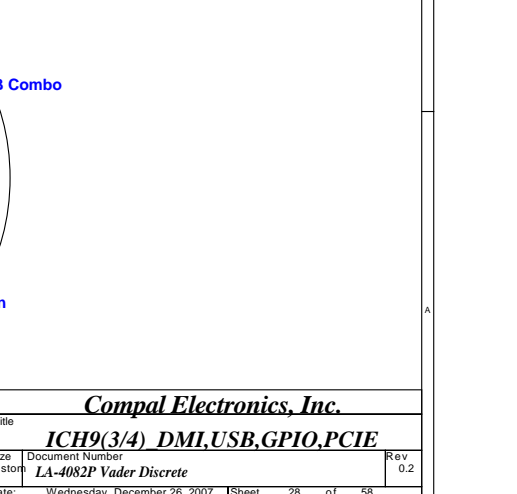
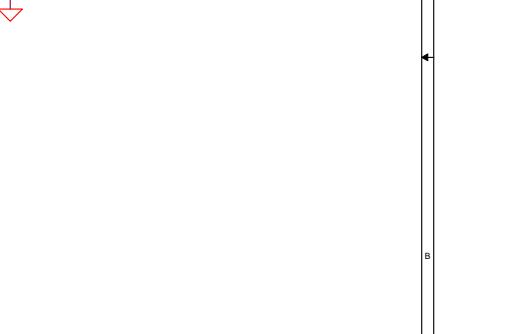
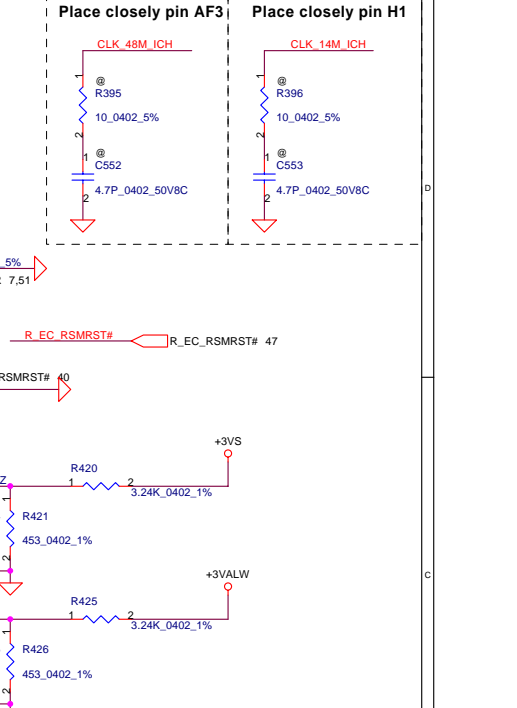
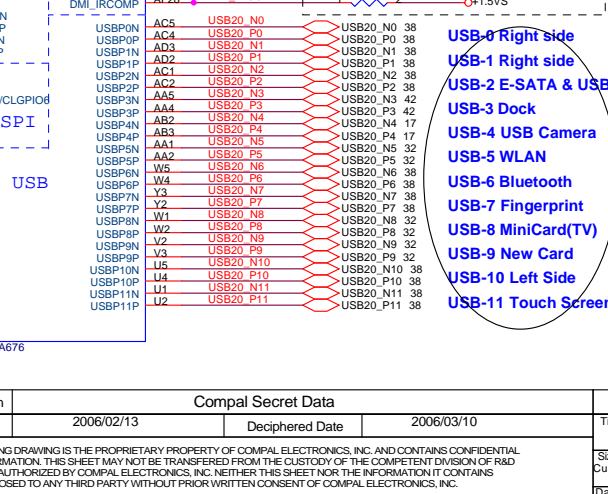
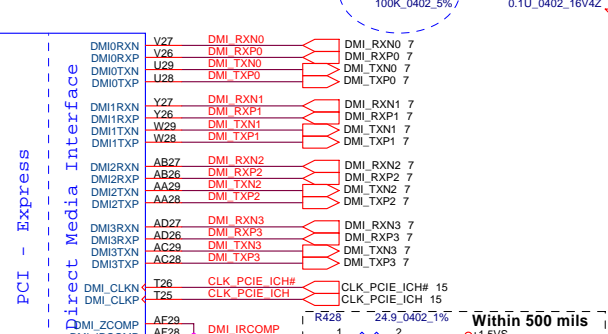
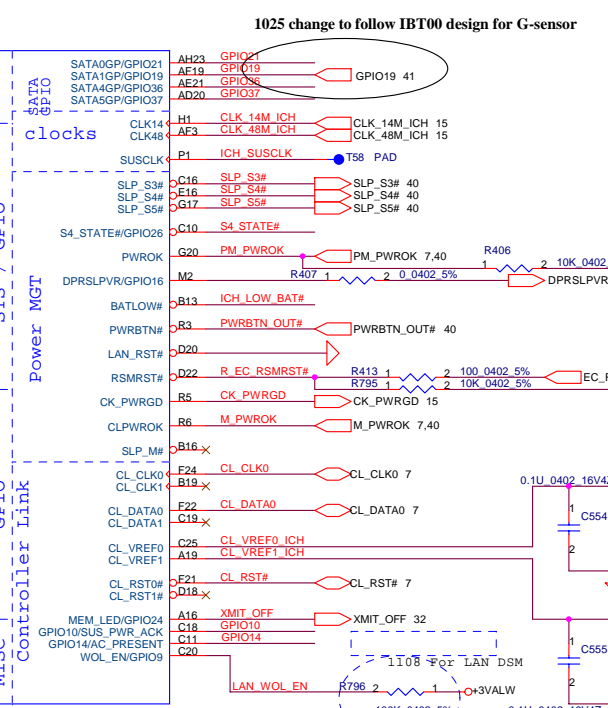
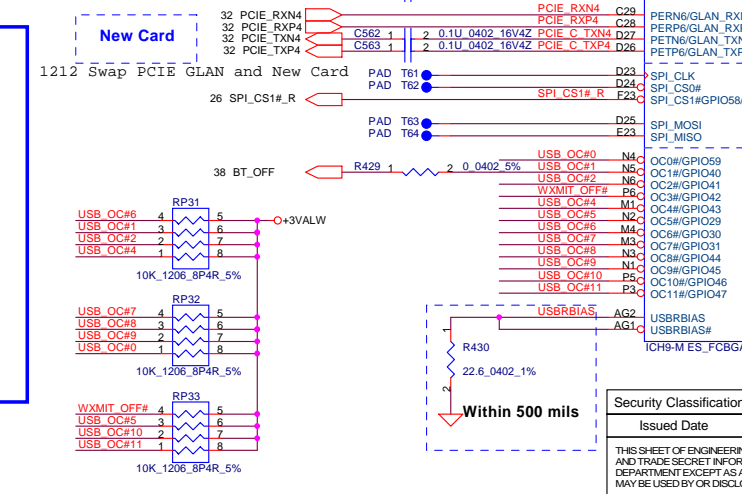
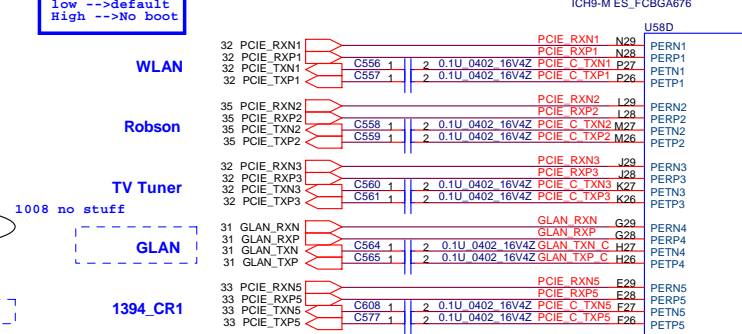
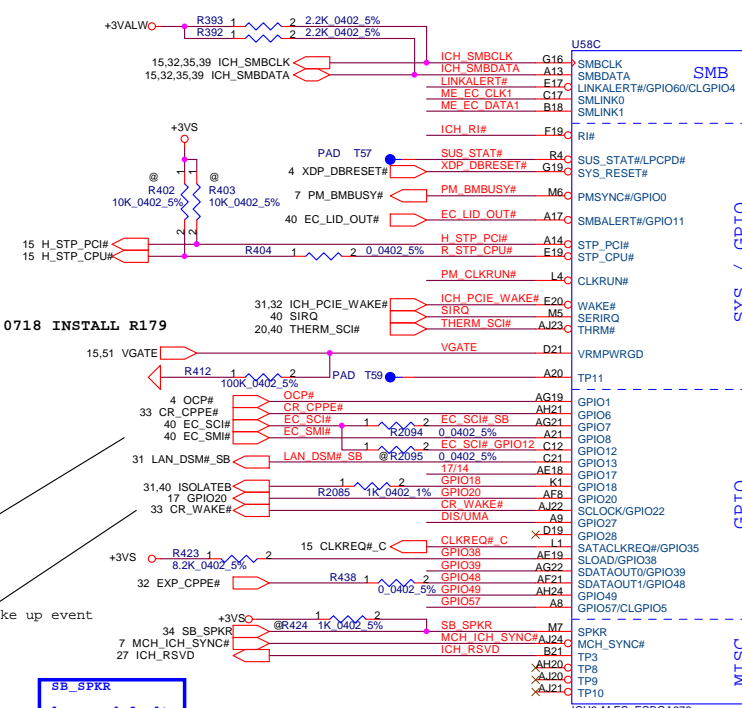
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Size		ICH9(2/4) LAN,HD,SATA,LPC	
Document Number	LA-4082P	Revision	0.2
Customer	Vader Discrete	Date	Wednesday, December 26, 2007
Sheet	27	of	58



1102 Add test point
1212 Add R2095 for EC_SCI#
1108 For LAN DSM
1109 Add GPIO22 for card reader wake up event



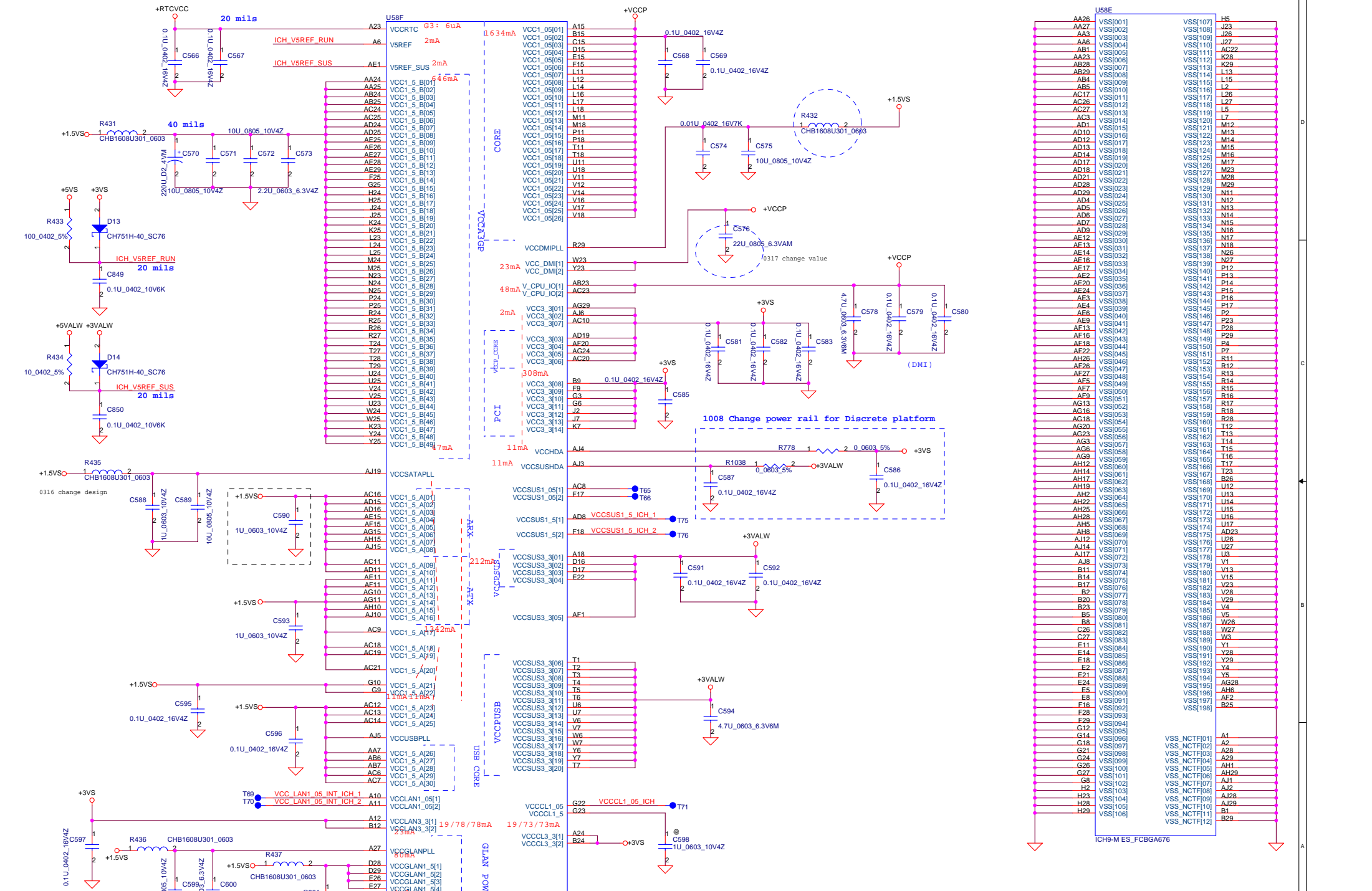
1008 add board ID detection



Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date
		2006/03/10

Compal Electronics, Inc.		
Title		
ICH9(3A) DMI,USB,GPIO,PCIE		
Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2
Date:	Wednesday, December 26, 2007	Sheet 28 of 58

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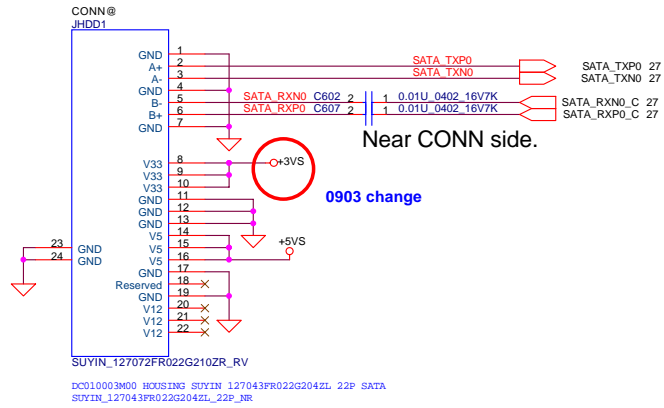
Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date
		2006/03/10

Title	
Compal Electronics, Inc.	
ICH9(4/4) POWER&GND	
Size	Document Number
Custom	LA-4082P Vader Discrete
Date	Wednesday, December 26, 2007
Sheet	29 of 58

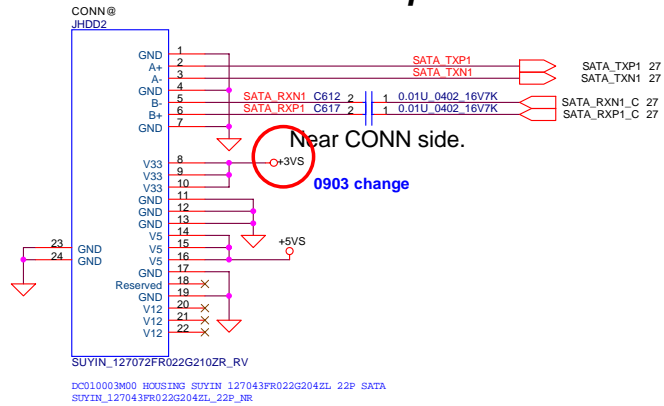
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Title	
Compal Electronics, Inc.	
ICH9(4/4) POWER&GND	
Size	Document Number
Custom	LA-4082P Vader Discrete
Date	Wednesday, December 26, 2007
Sheet	29 of 58

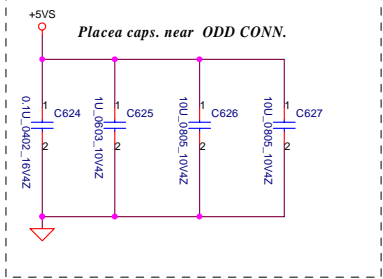
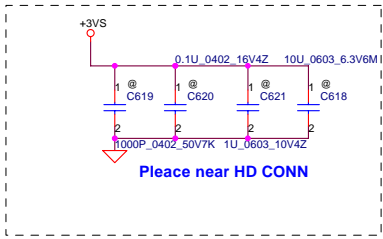
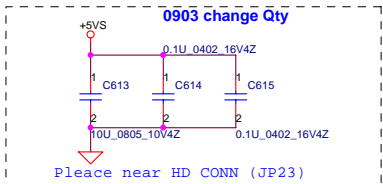
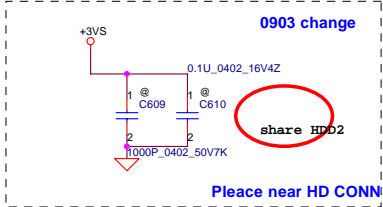
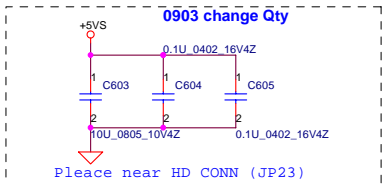
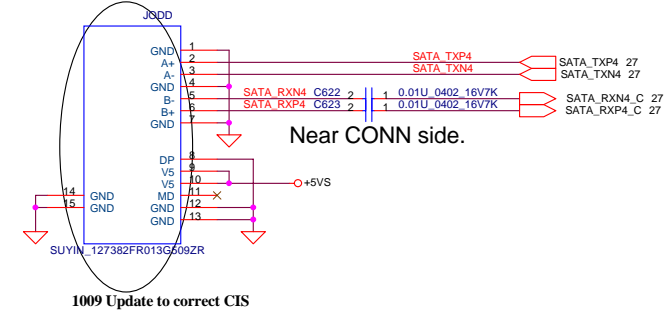
HDD Connector



2nd HDD Connector-option



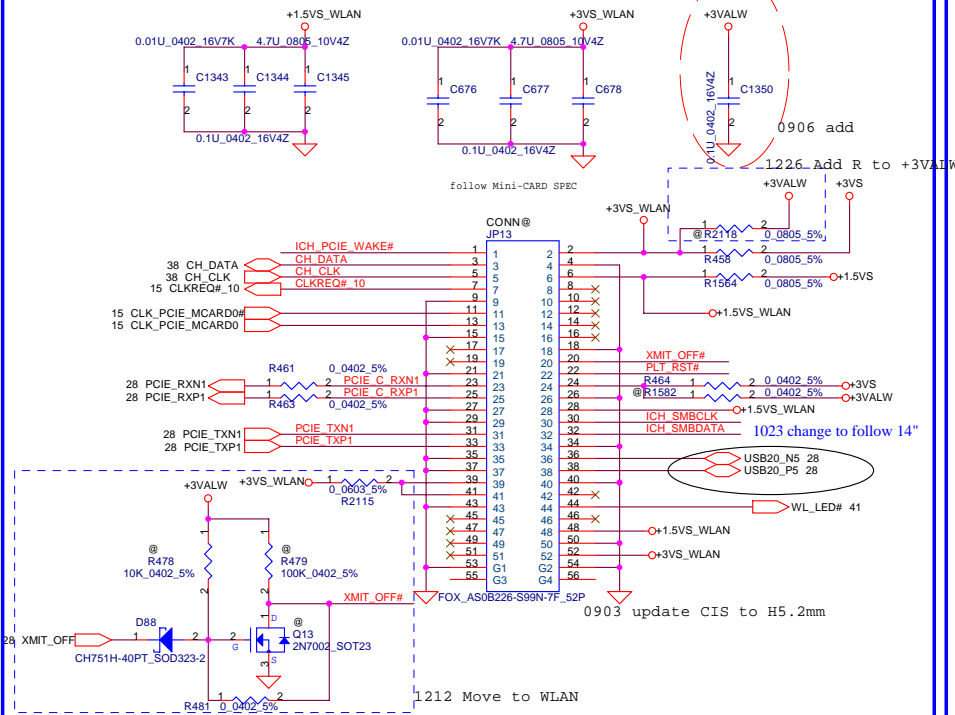
CD-ROM Connector



Security Classification	Compal Secret Data			Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	HDD & CDROM	
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				Custom	LA-4082P Vader Discrete
				Date	Wednesday, December 26, 2007
				Sheet	30 of 58

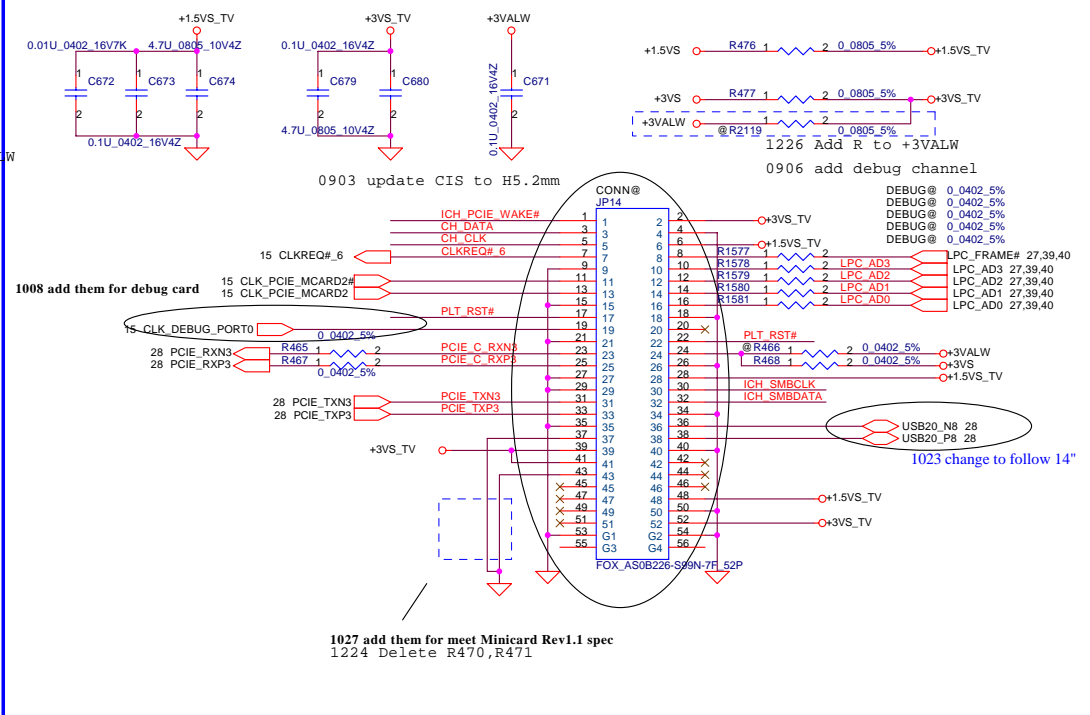
Mini Card 0--WLAN

1022 change to follow HP design

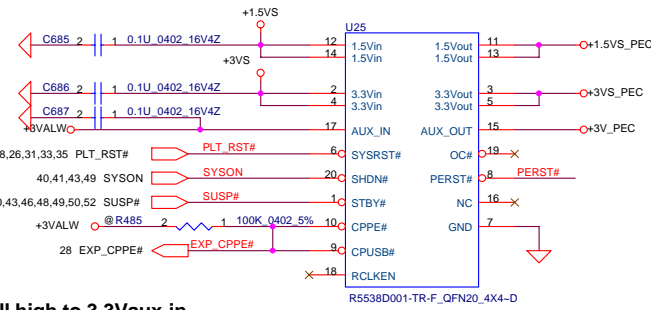


Mini Card 2--TV tuner

1022 change to follow HP design

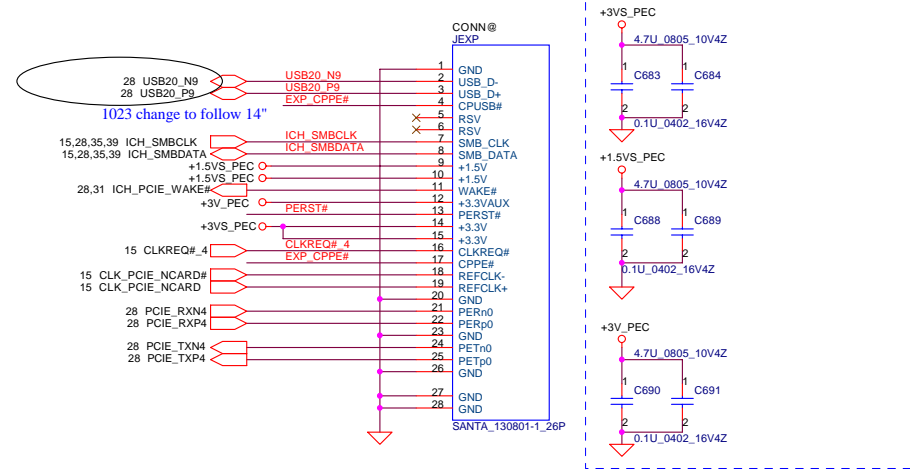


New Card



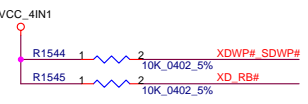
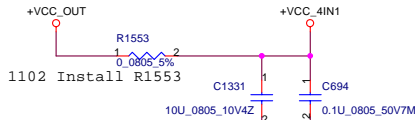
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

Near to Express Card slot.

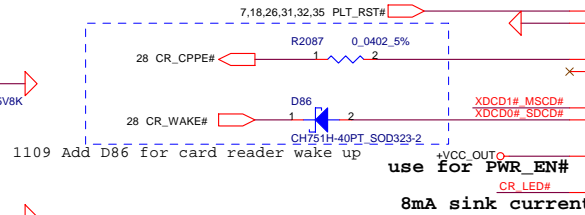
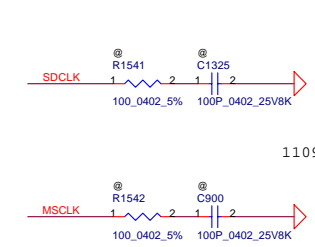
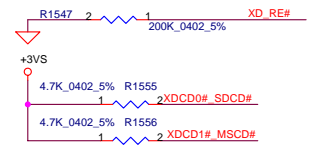
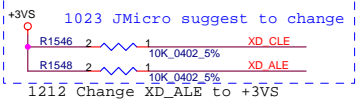


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Issued Date	2006/02/13	Deciphered Date	2006/03/10	WLAN, WWAN, New Card	
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Size	Document Number	Date	Wednesday, December 26, 2007	Sheet	32 of 58
Custom	LA-4082P Vader Discrete	Rev	0.2		

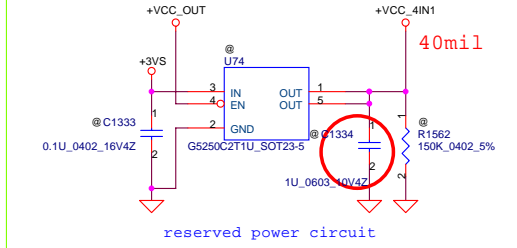
Use 0603 type and over 20 mils trace width on both side



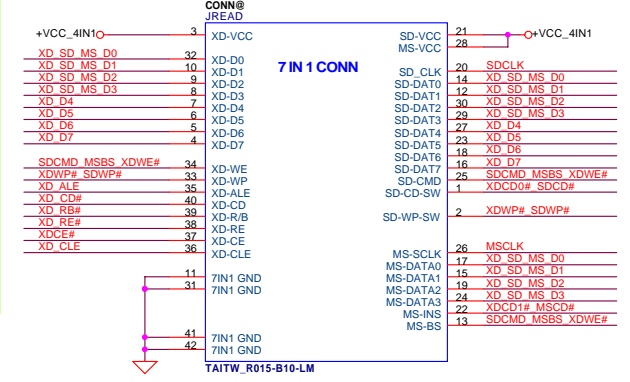
Strap pin for JMicro



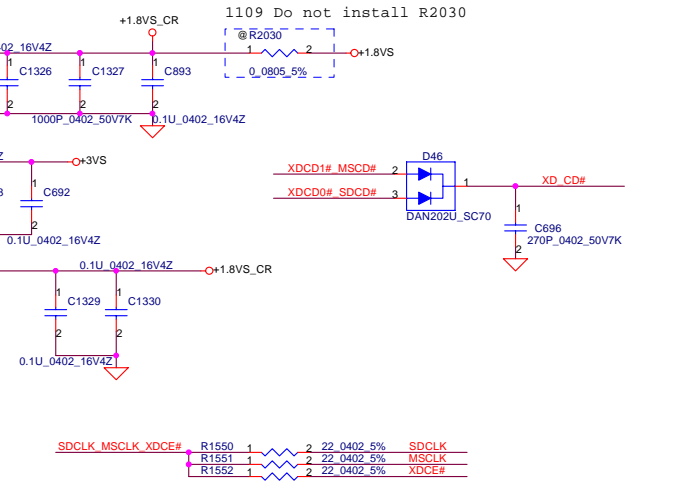
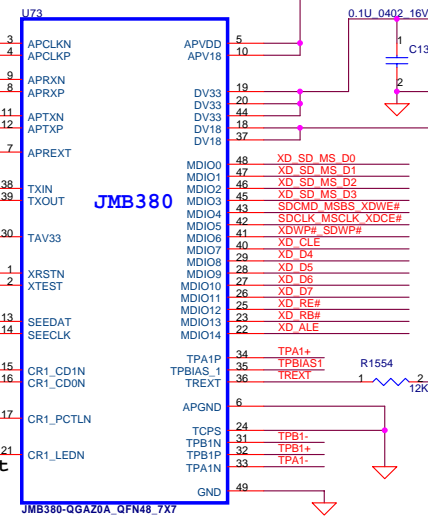
need change to low active switch



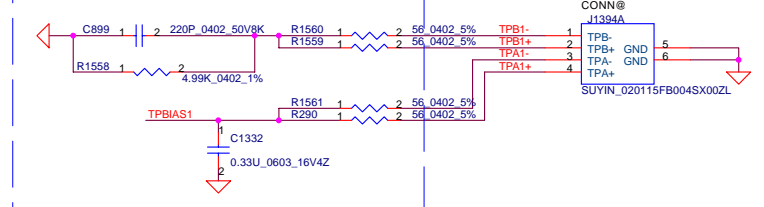
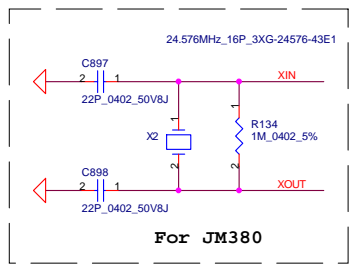
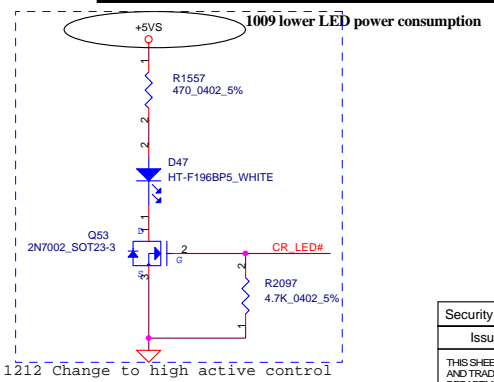
Card Reader Connector



Power Circuit

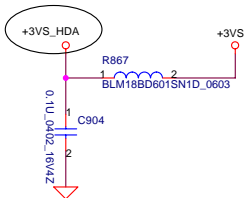


White LED: VF=3V, IF = 5mA, Res = 56ohm

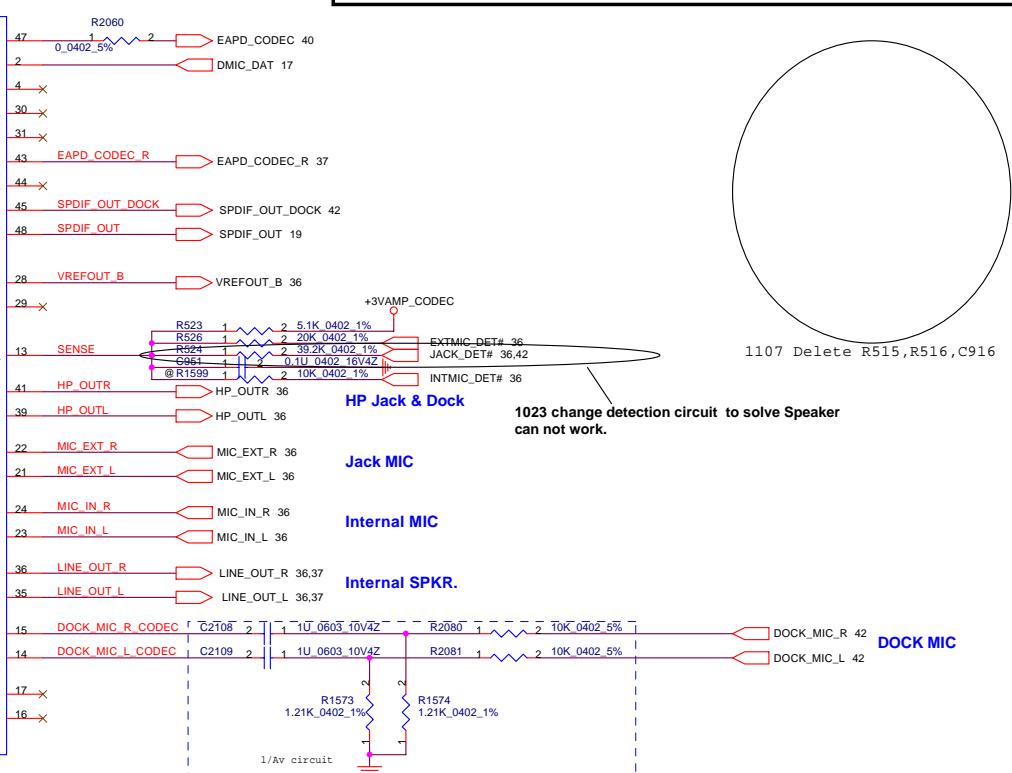
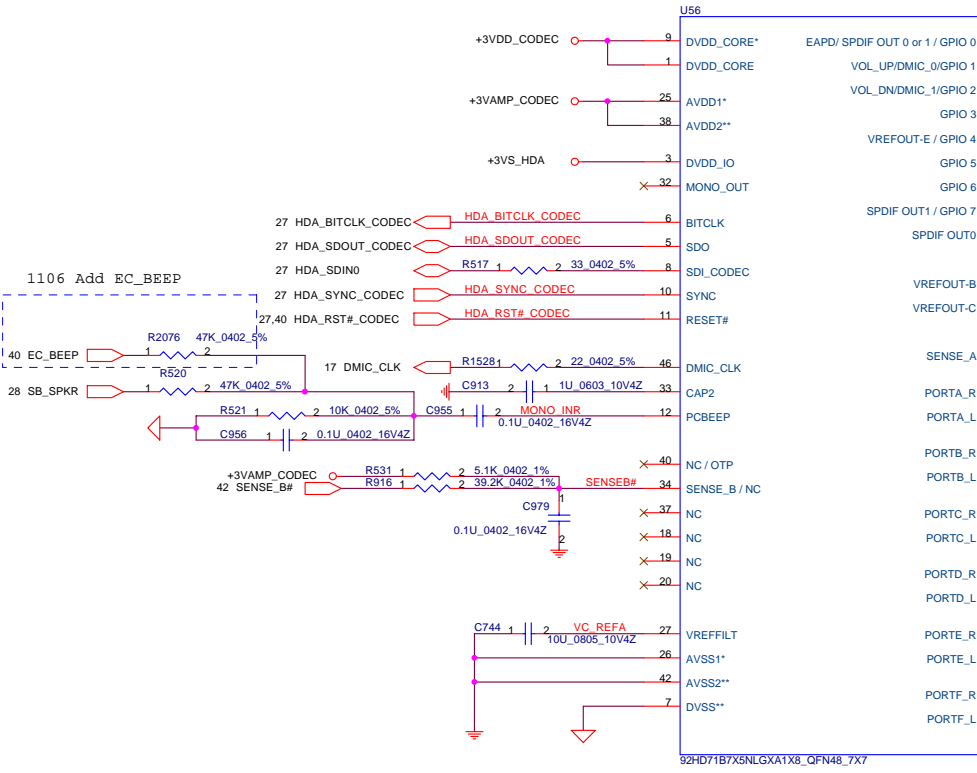
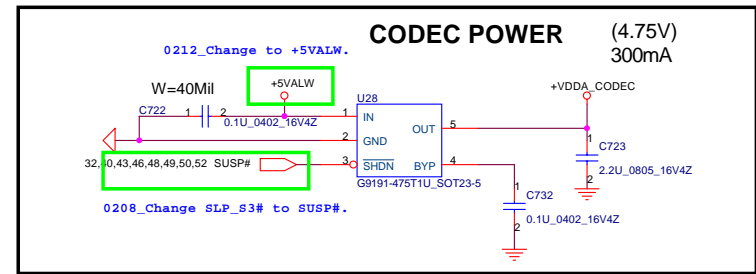
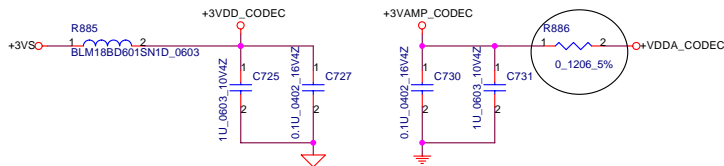


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Issued Date	2006/02/13	Deciphered Date	2006/03/10	JMB380/385 card reader/1394
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Size	Document Number	Date	Wednesday, December 26, 2007	Rev 0.2
Custom	LA-4082P Vader Discrete	Sheet	33 of 58	

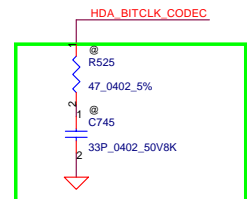
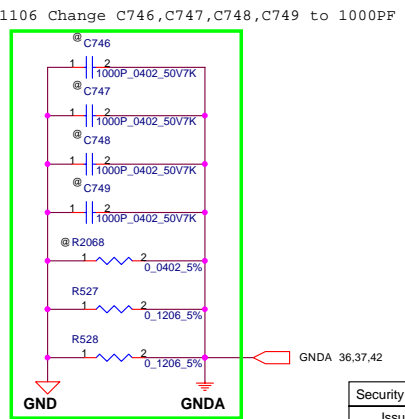
1008 Change to +3V



1019 Change Size to 1206 for IDT request

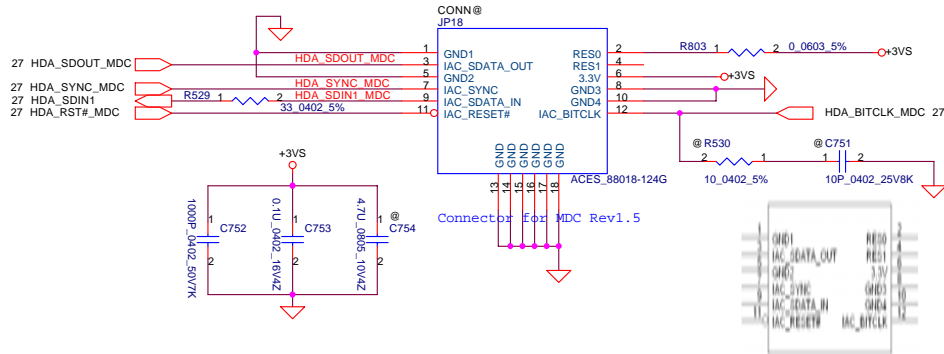


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

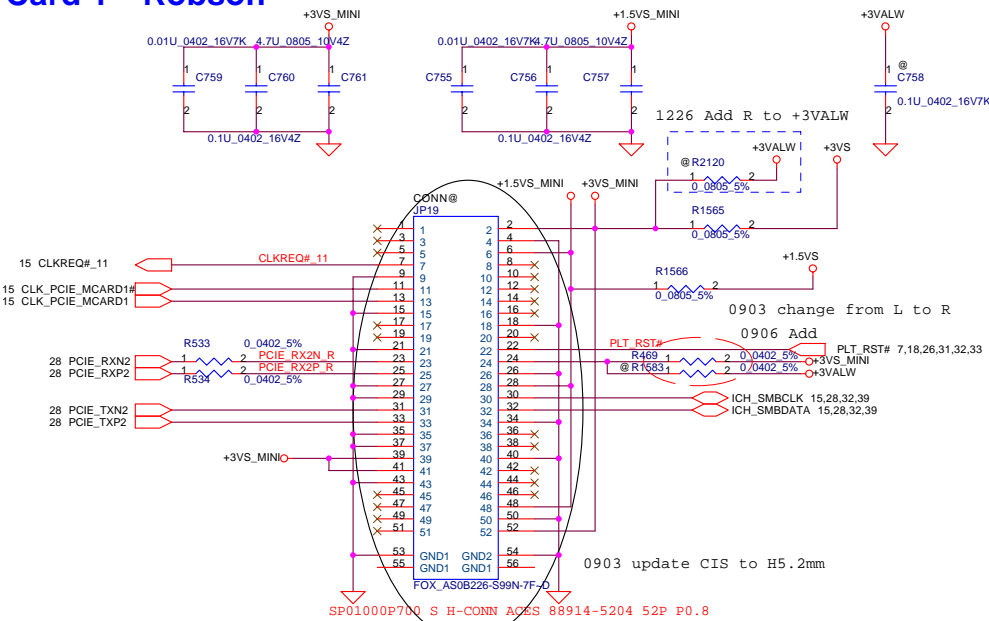


MDC 1.5 Conn.

Change type 4/25

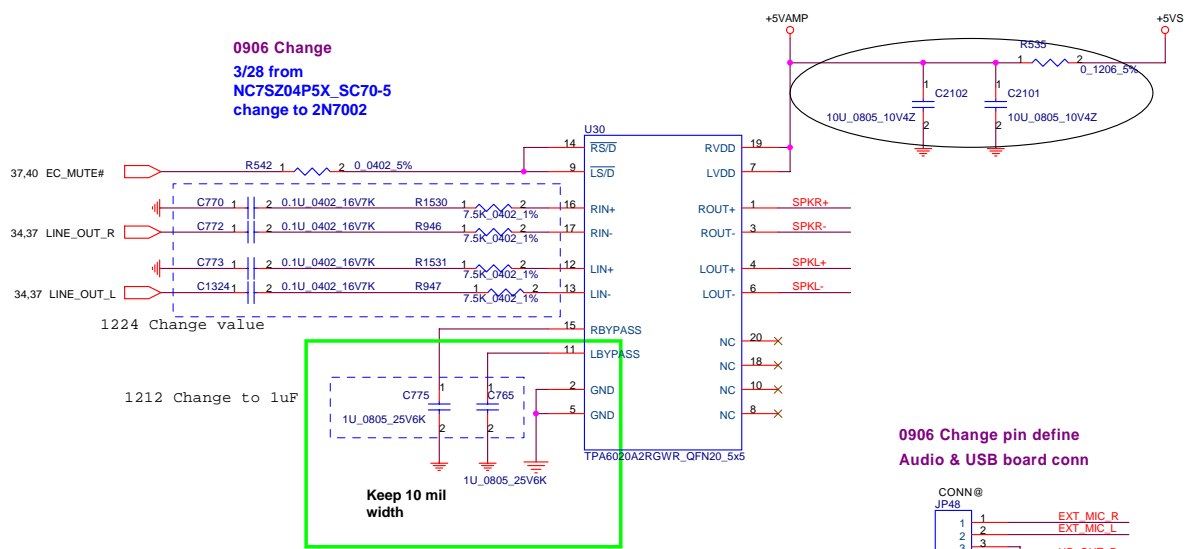


Mini Card 1---Robson

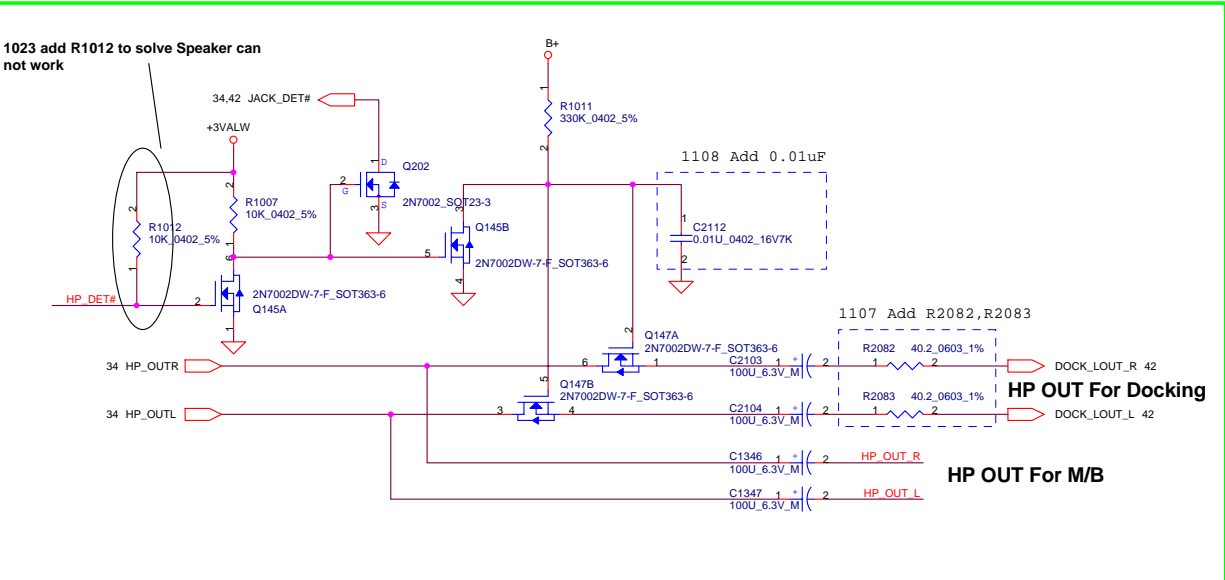
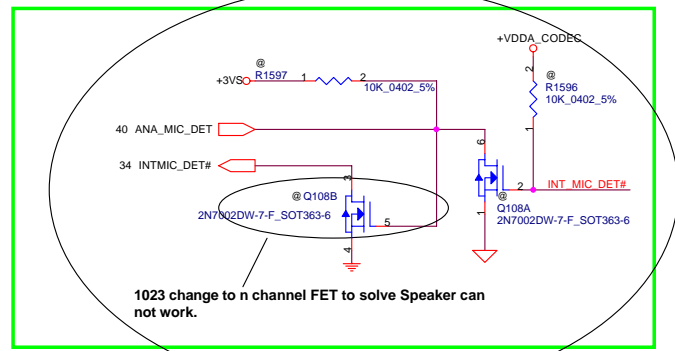
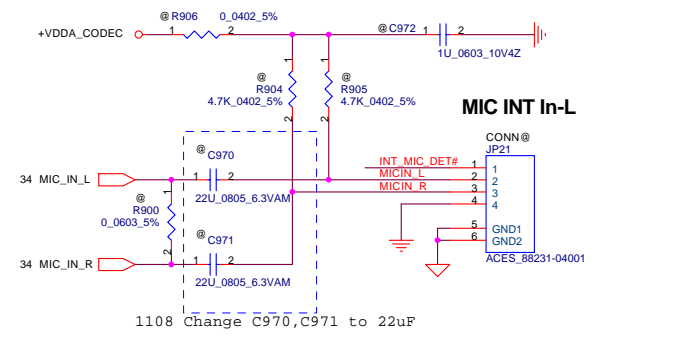
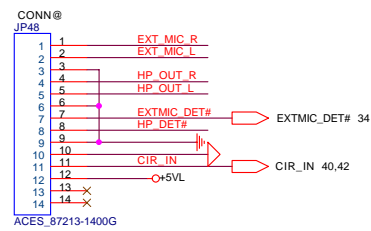


Security Classification	Compal Secret Data			Title		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc. MDC 1.5 & Robson		
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				Custom	LA-4082P Vader Discrete	0.2
				Date:	Wednesday, December 26, 2007	Sheet 35 of 58

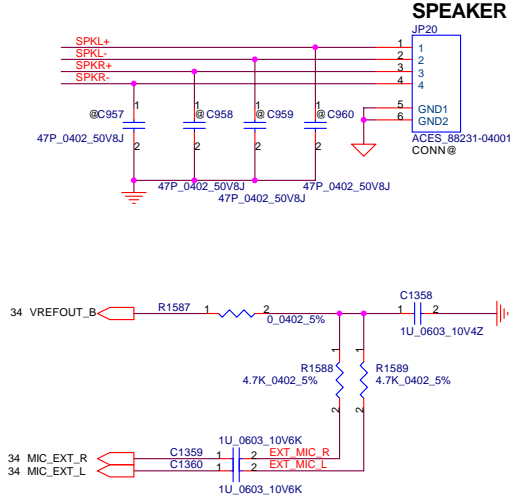
0906 Change
3/28 from
NC7SZ04P5X_SC70-5
change to 2N7002



0906 Change pin define
Audio & USB board conn

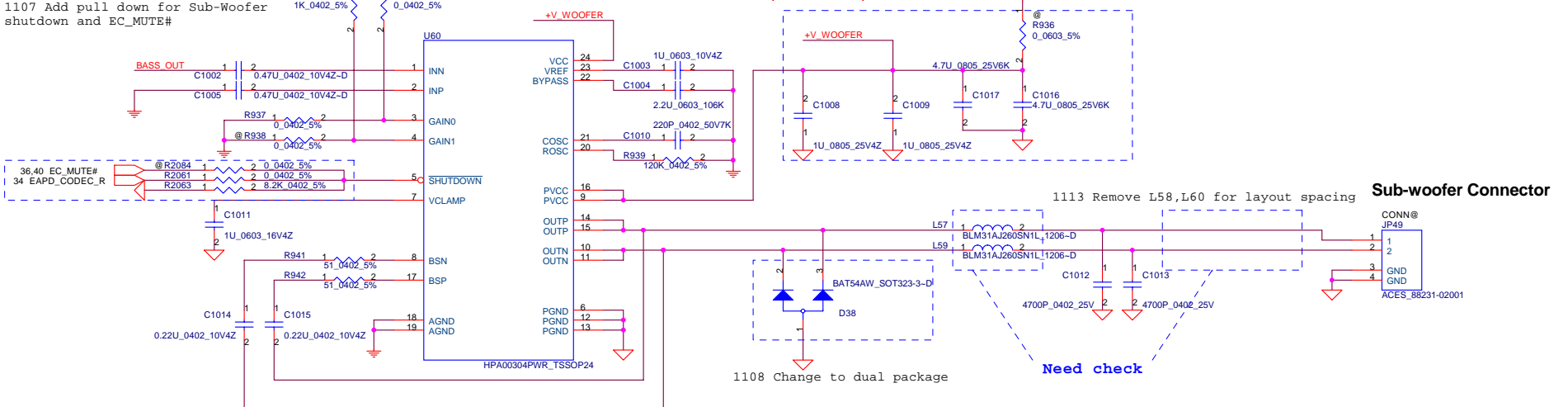
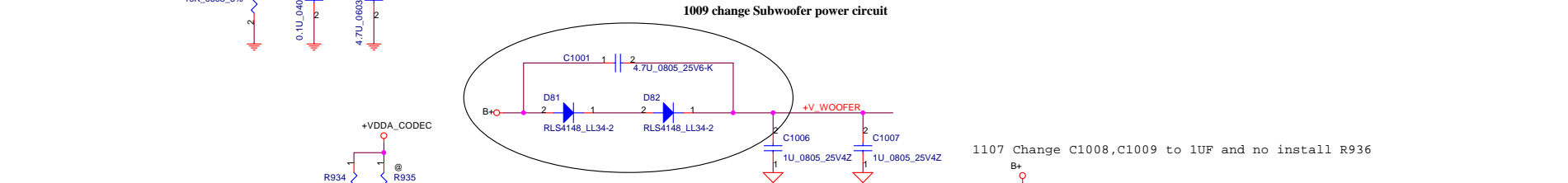
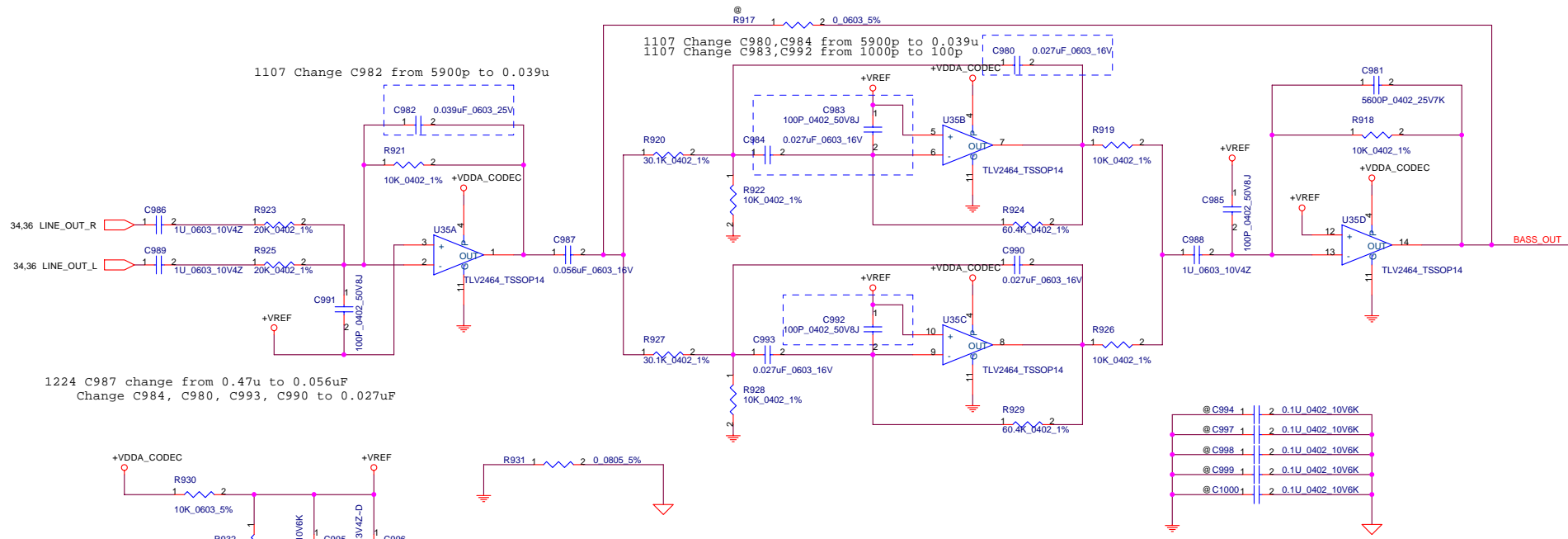


SP0200D000 S W-CONN ACES 85204-04001 4P P1.25



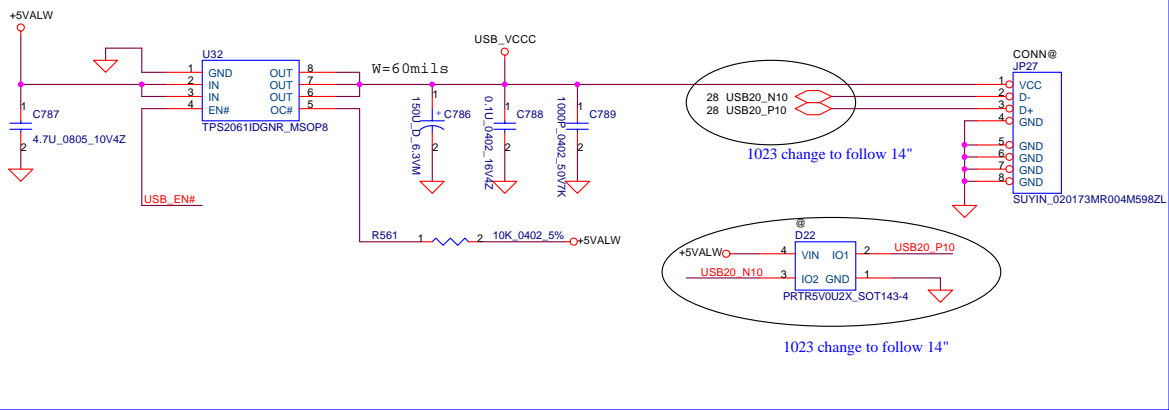
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Issued Date	2006/02/13	Deciphered Date
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Compal Electronics, Inc.		
AMP & Audio Jack		
Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2
Date:	Wednesday, December 26, 2007	Sheet 36 of 58

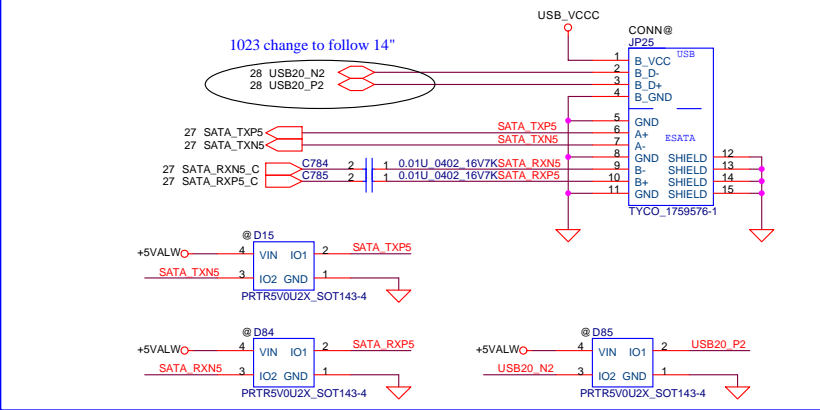


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				Custom	LA-4082P Vader Discrete
				Date:	Wednesday, December 26, 2007 Sheet 37 of 58

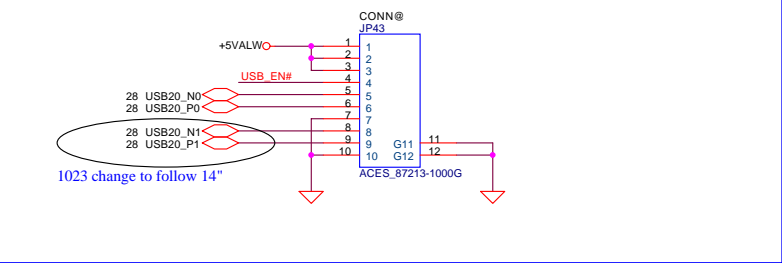
Left side USB Connector



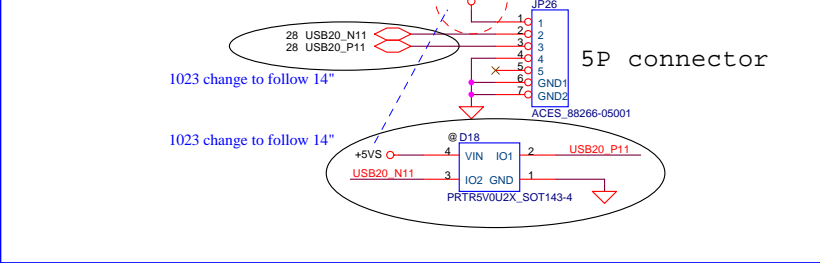
Left side ESATA/USB combination Connector



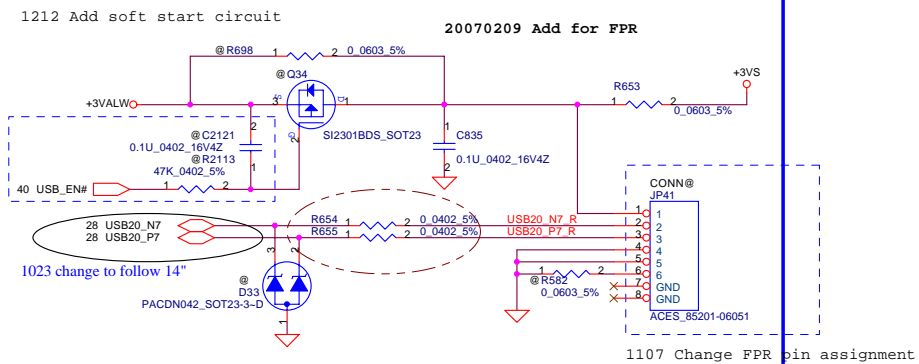
USB cable connector for Right side



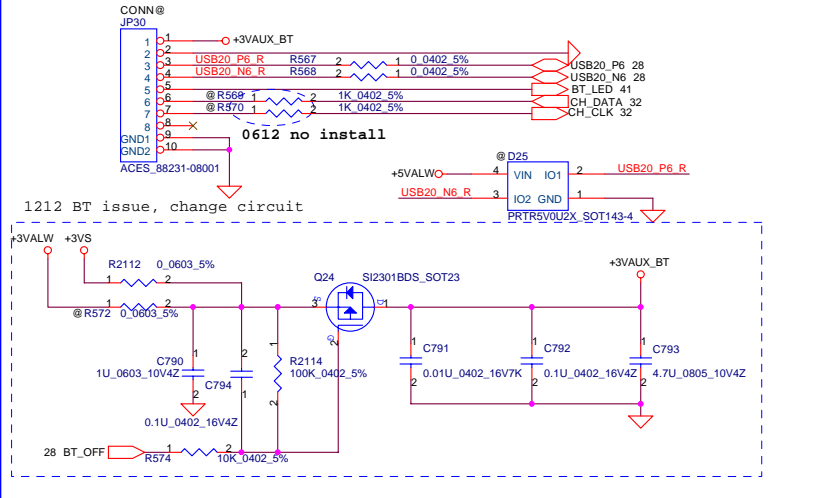
Touch screen connector



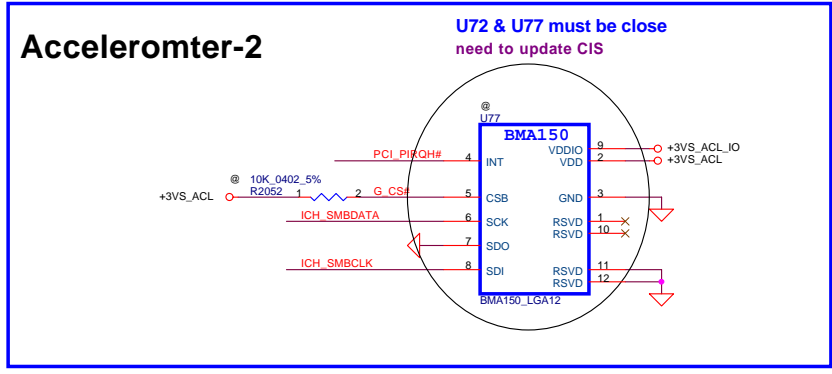
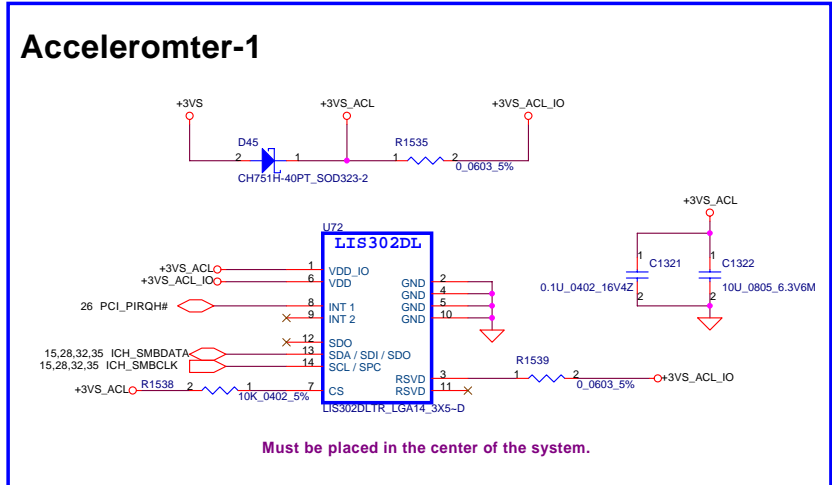
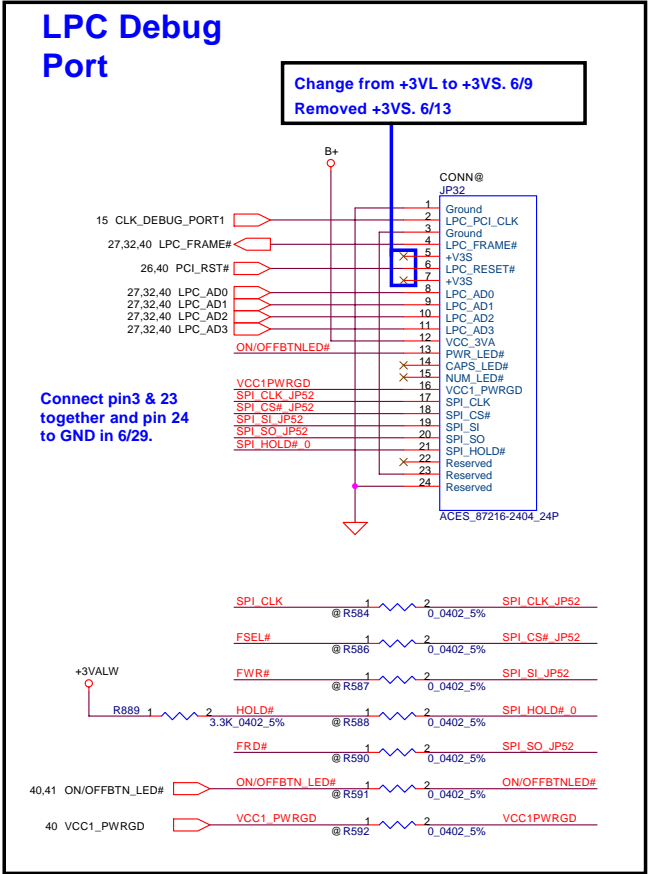
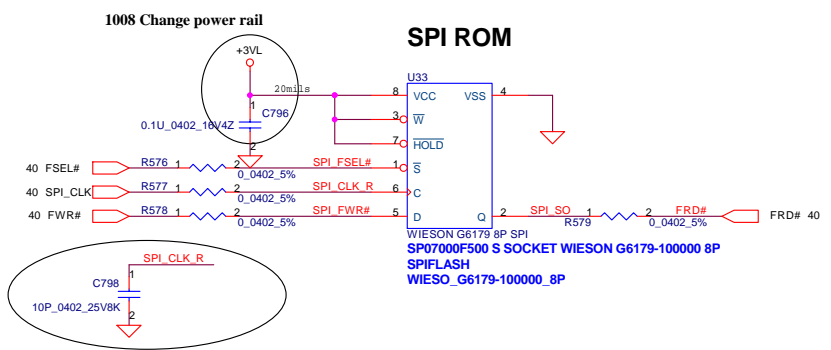
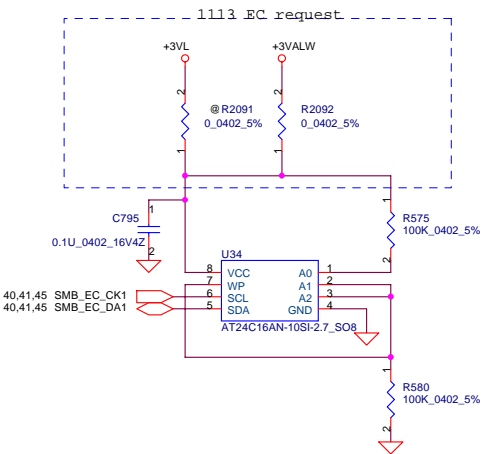
Finger printer



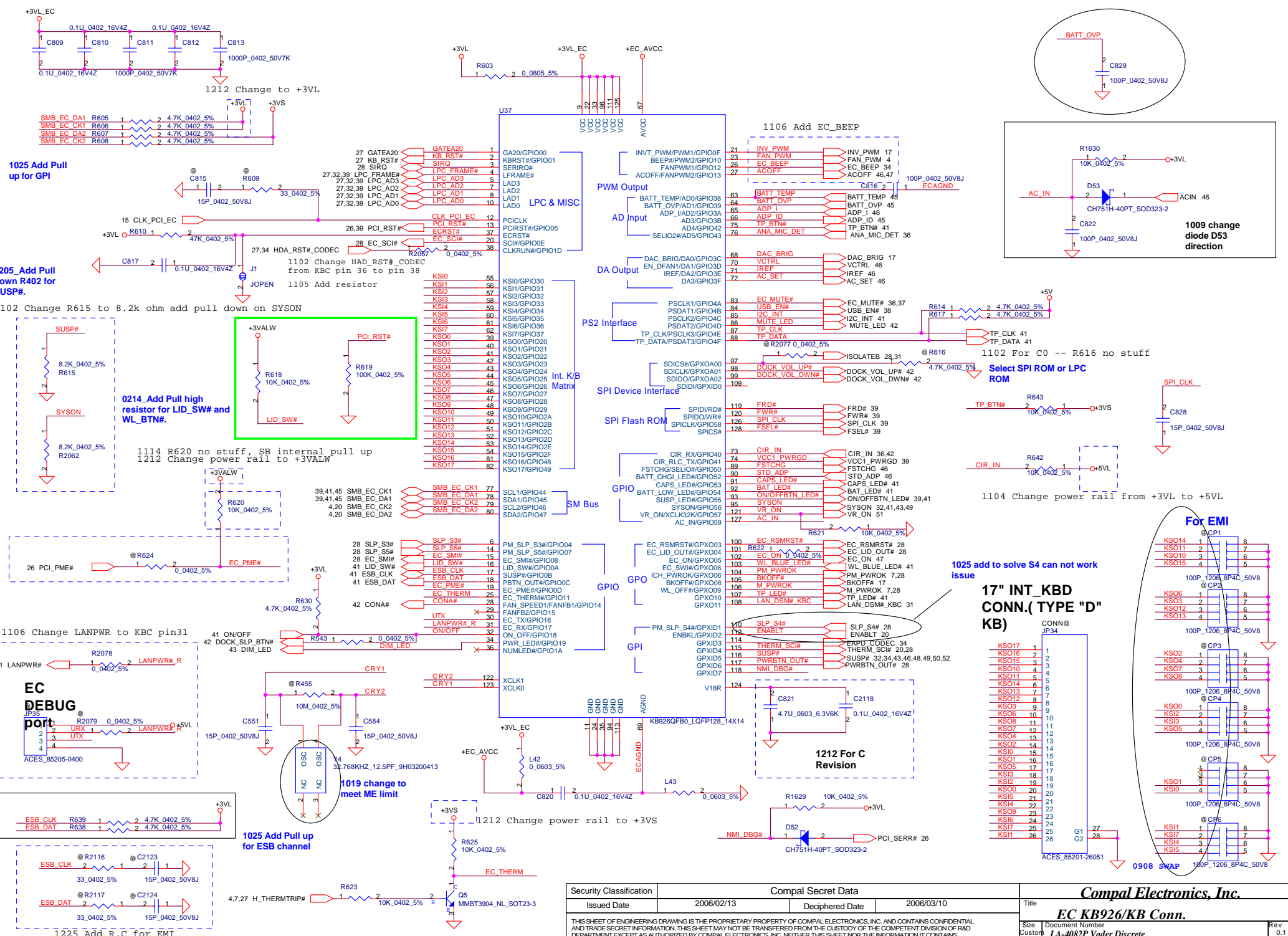
BT Connector



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Issued Date	2006/02/13	Deciphered Date	2006/03/10	USB, BT, eSATA
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Date:	Wednesday, December 26, 2007	Sheet	38	Rev 0.2



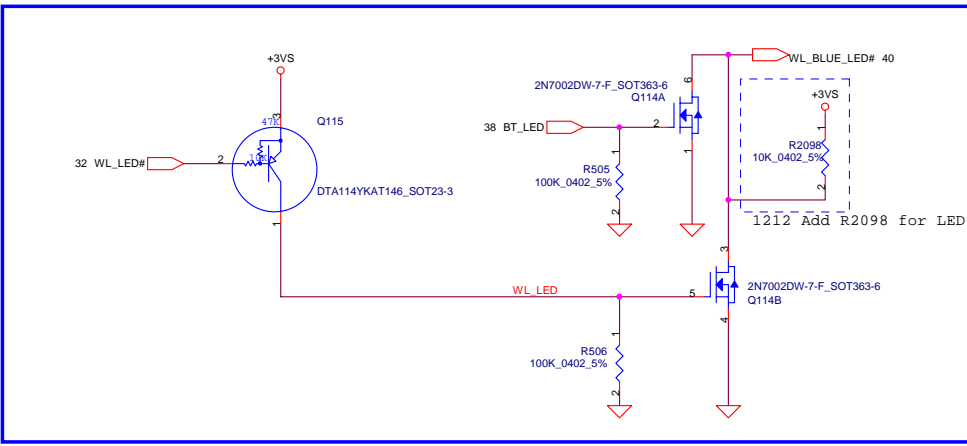
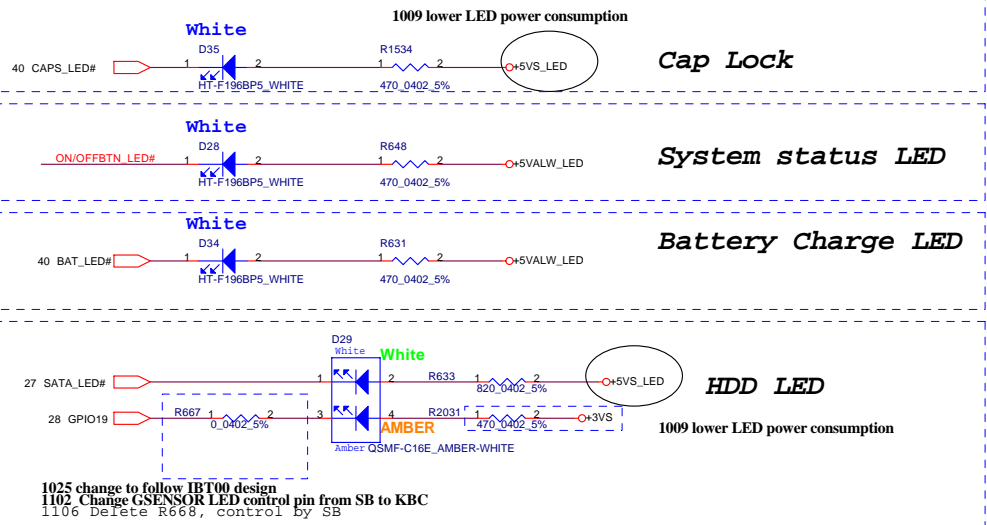
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title BIOS ROM	
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Date	Wednesday, December 26, 2007	Sheet	39	of	58



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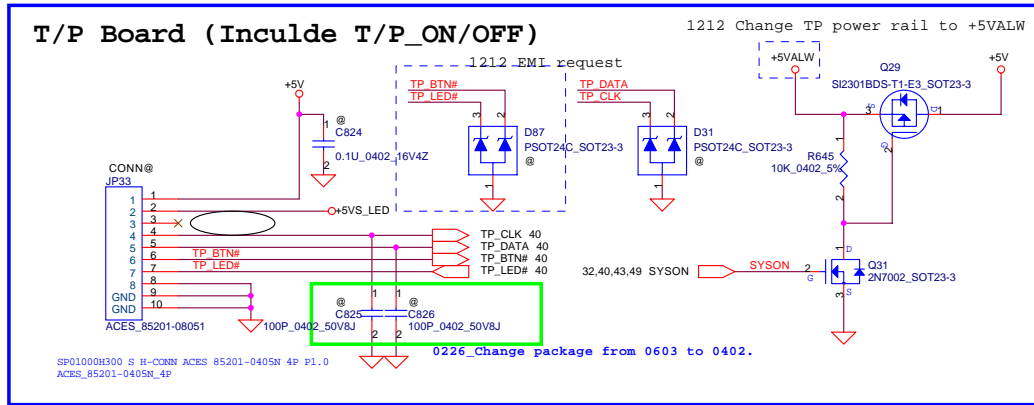
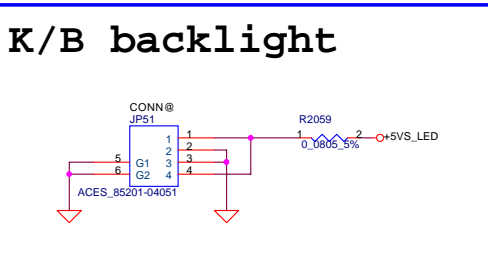
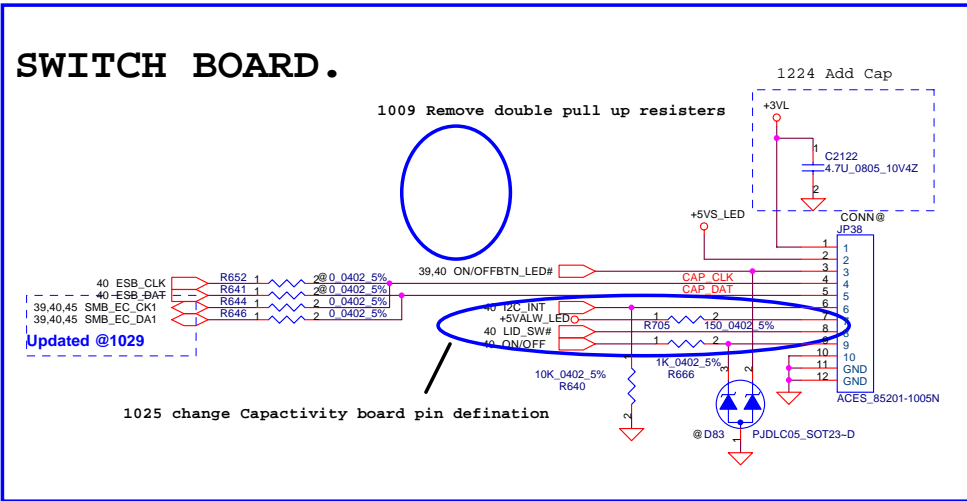
Compal Electronics, Inc.	
Title	EC KB926/KB Conn.
Size	Document Number
Customer	LA-4082P Vader Discrete
Date	Wednesday, December 26, 2007
Sheet	40 of 58
Rev	0.1

LED

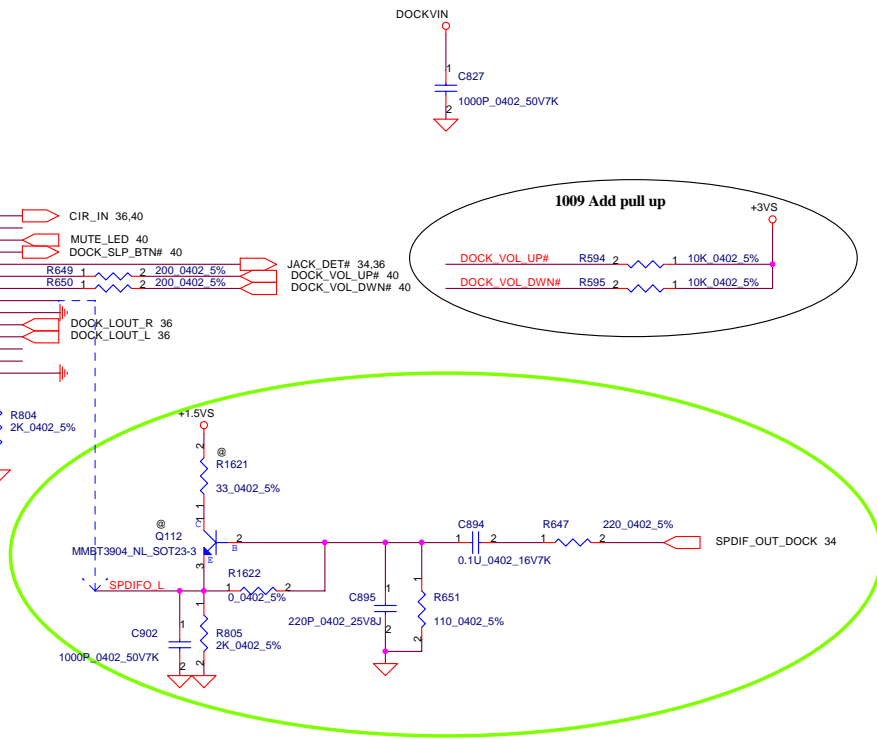
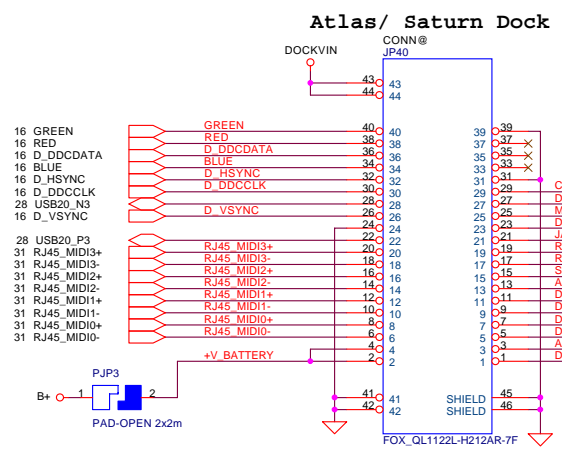
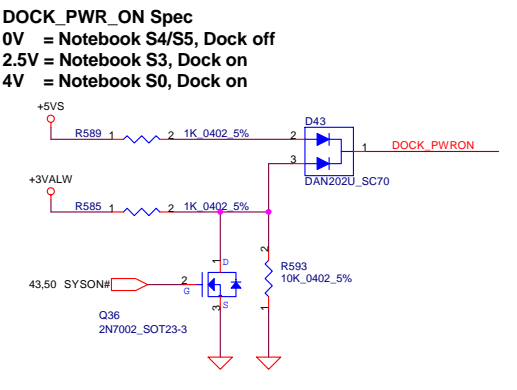


for debug only

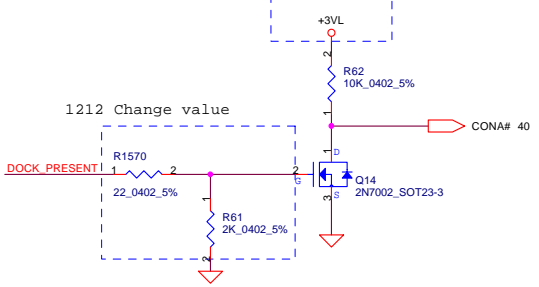
1212 Delete SW5, SW6



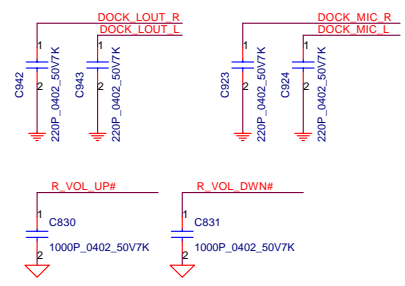
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	KBD, ON/OFF, SW, CIR	
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Size	Document Number	Rev	Date: Wednesday, December 26, 2007 Sheet 41 of 58		
Custom	LA-4082P Vader Discrete	0.1			



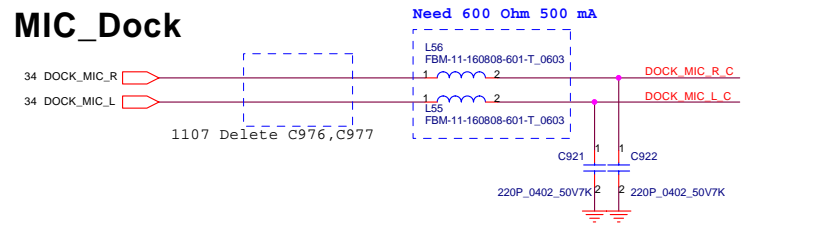
1112 Change power rail from +3VALW to +3VL



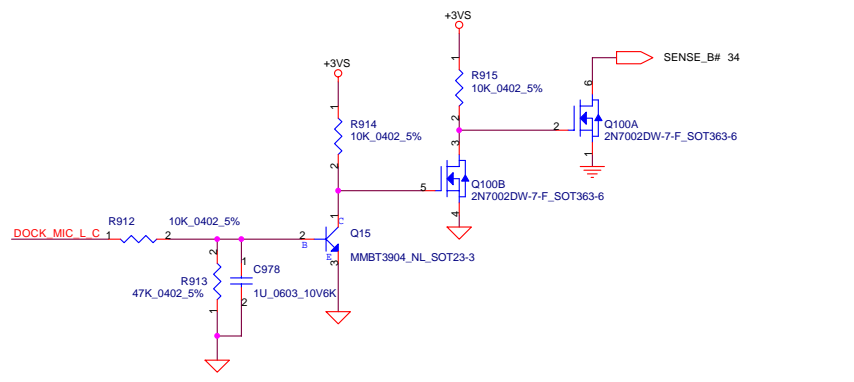
need change to reverse type connector



MIC_Dock

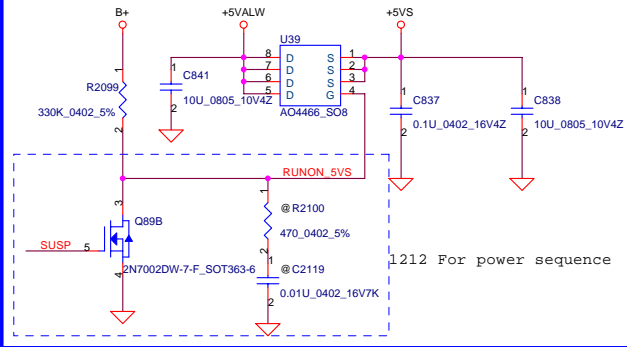


1009 Remove TV components

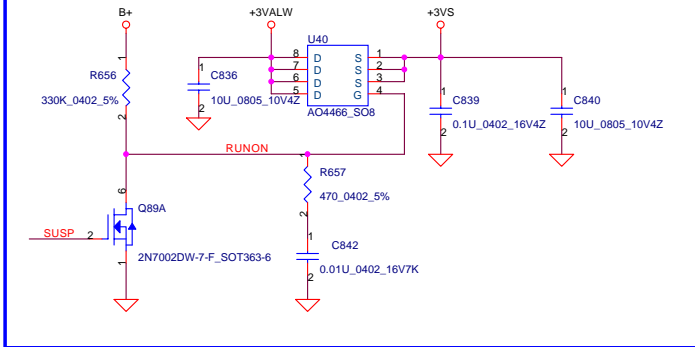


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Size	Document Number	Rev		
Custom	LA-4082P Vader Discrete	0.1		
Date:	Wednesday, December 26, 2007	Sheet	42	of 58

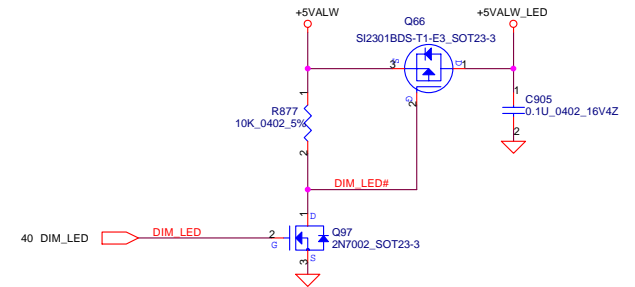
+5VALW to +5VS Transfer



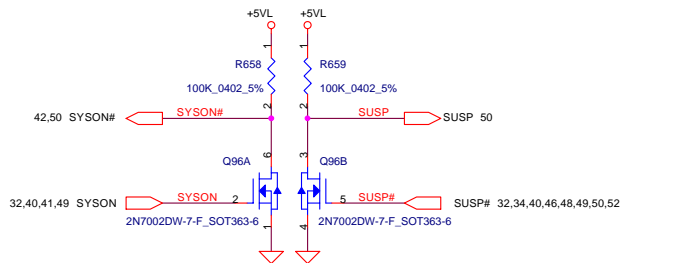
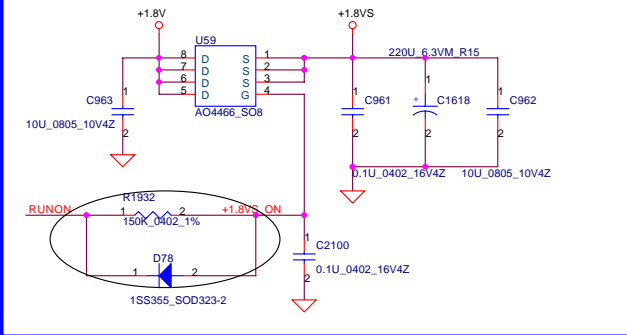
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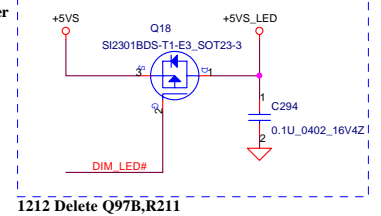
DIMM LED



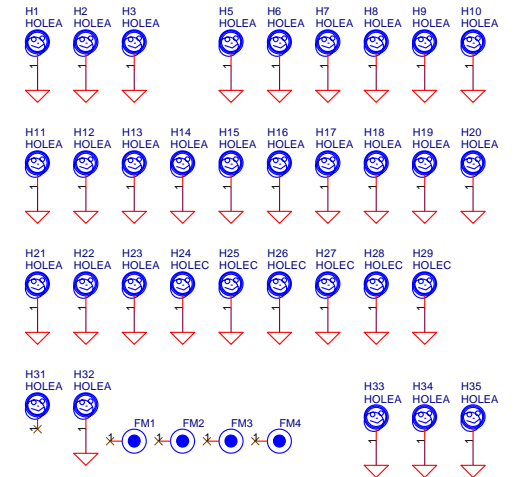
+1.8V to +1.8VS Transfer



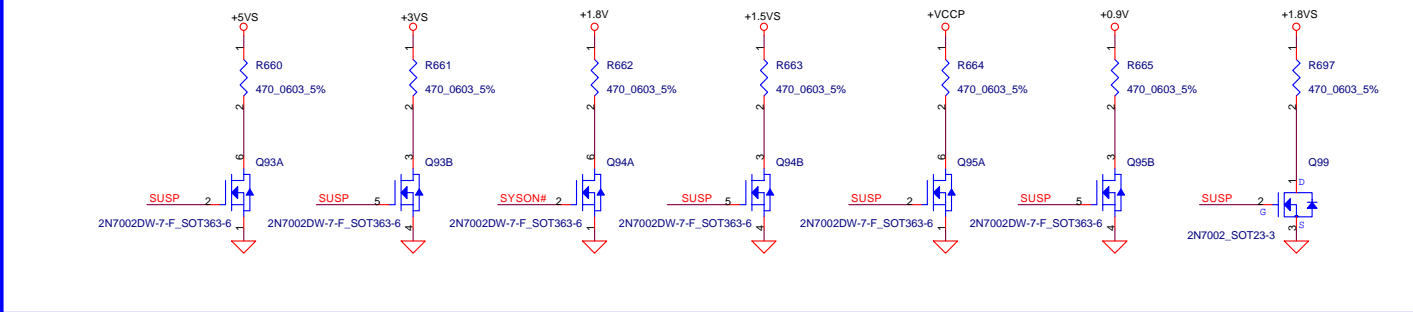
1009 Add for LED power



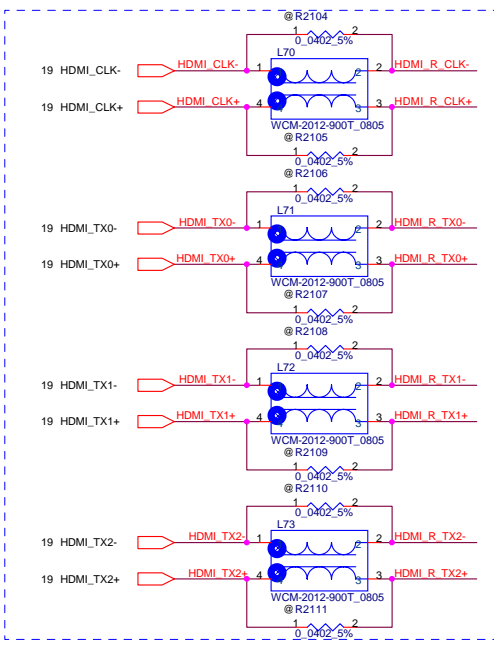
1212 Outline modify



Discharge circuit

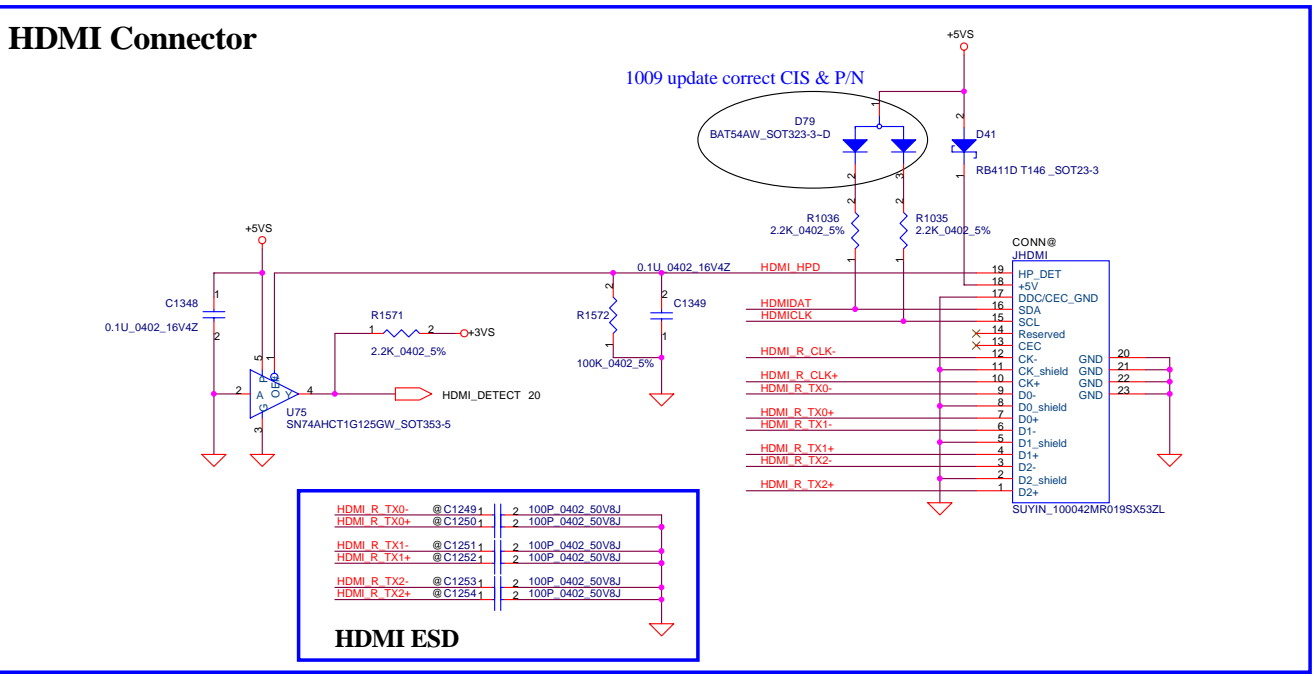


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Issued Date	2006/02/13	Deciphered Date	2006/03/10	DC/DC Interface	
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				Custom	LA-4082P Vader Discrete
				Date:	Wednesday, December 26, 2007
				Sheet	43 of 58
				Rev	0.1

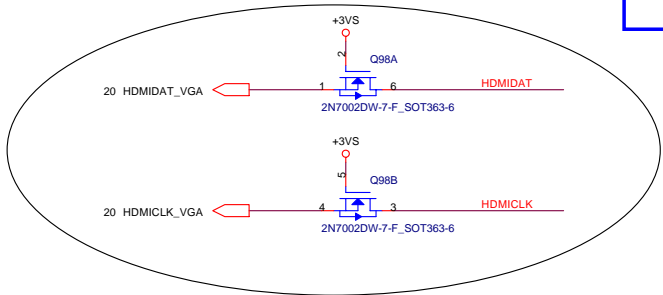


1212 Add 0 ohm

HDMI Connector

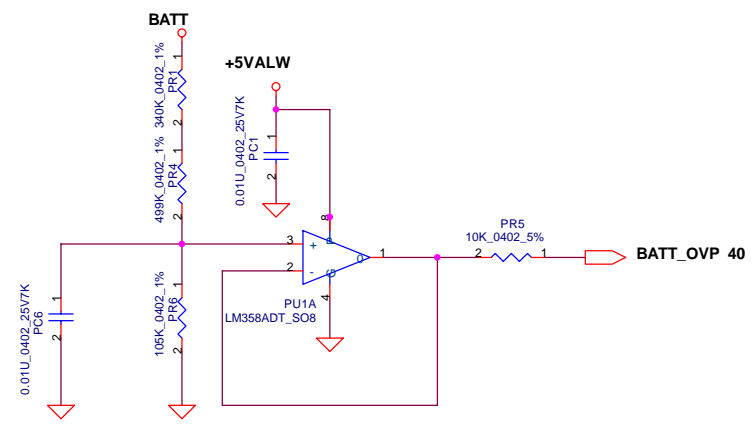
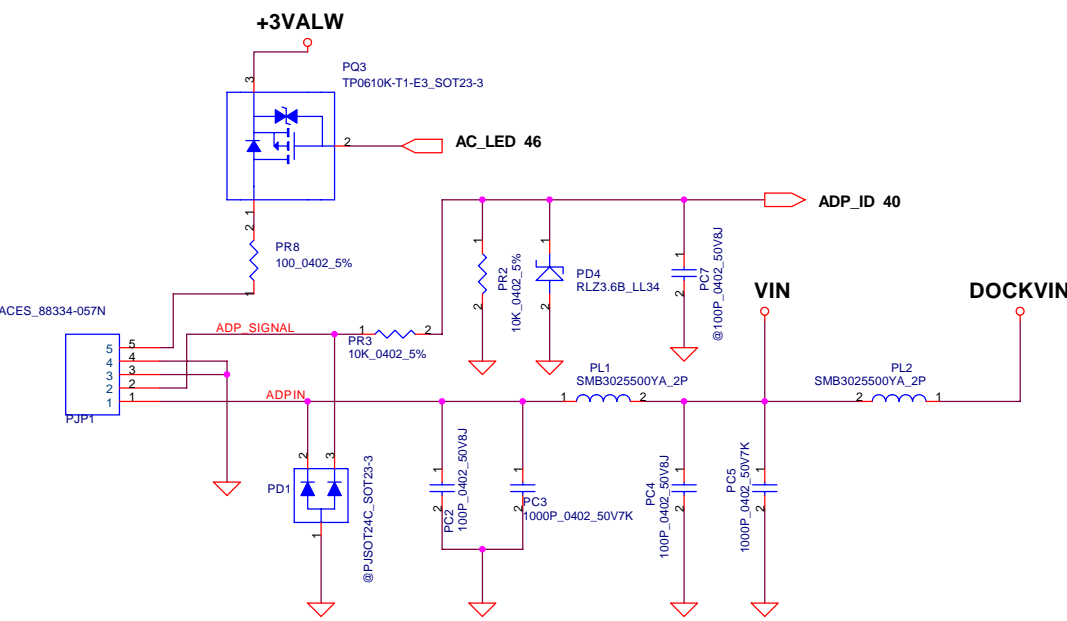


HDMI ESD		
HDMI_R_TX0-	@ C1249.4	2 100P 0402 50V8J
HDMI_R_TX0+	@ C1250.1	2 100P 0402 50V8J
HDMI_R_TX1-	@ C1251.1	2 100P 0402 50V8J
HDMI_R_TX1+	@ C1252.1	2 100P 0402 50V8J
HDMI_R_TX2-	@ C1253.1	2 100P 0402 50V8J
HDMI_R_TX2+	@ C1254.1	2 100P 0402 50V8J

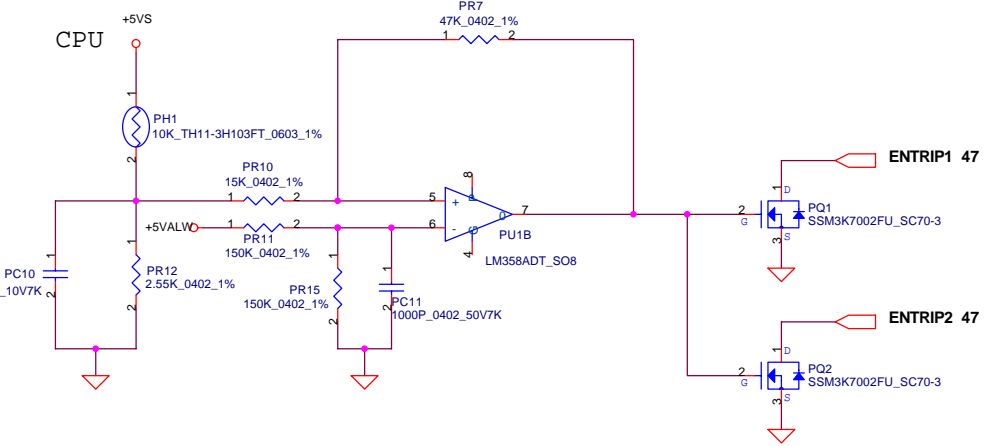
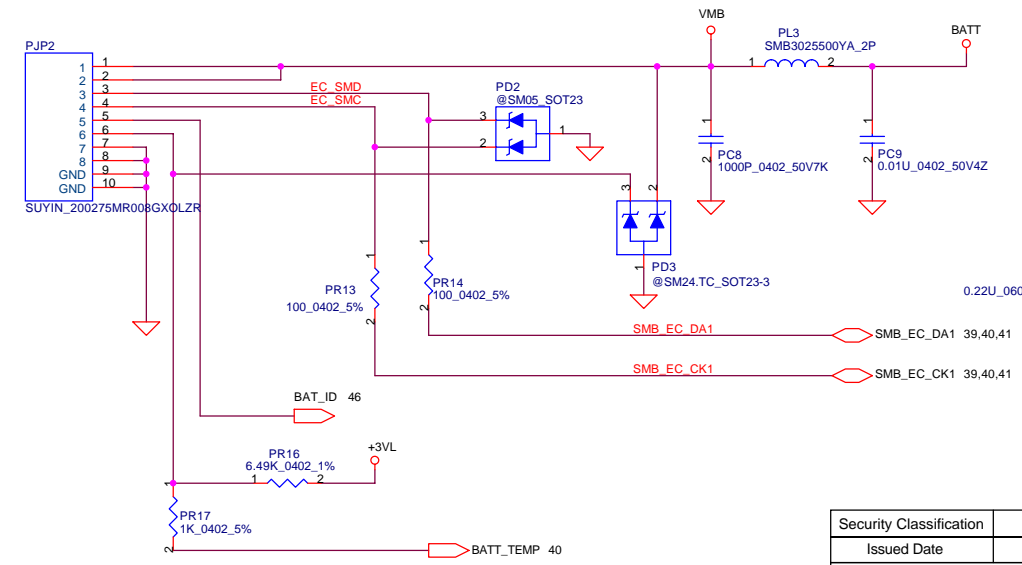


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Issued Date	2006/02/13	Deciphered Date 2006/03/10
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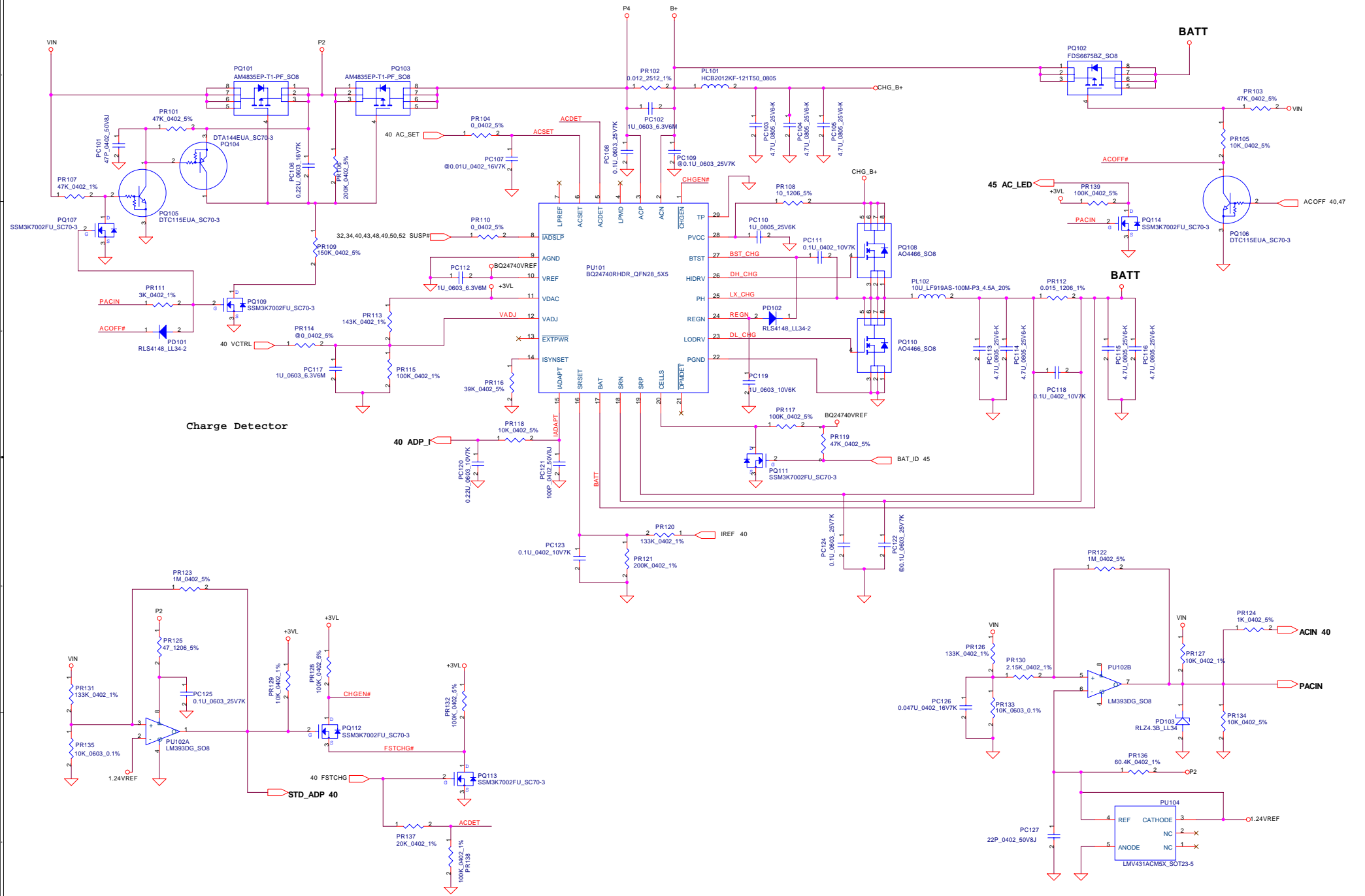
Compal Electronics, Inc.		
Title HDMI LS & Conn.		
Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.1
Date:	Wednesday, December 26, 2007	Sheet 44 of 58



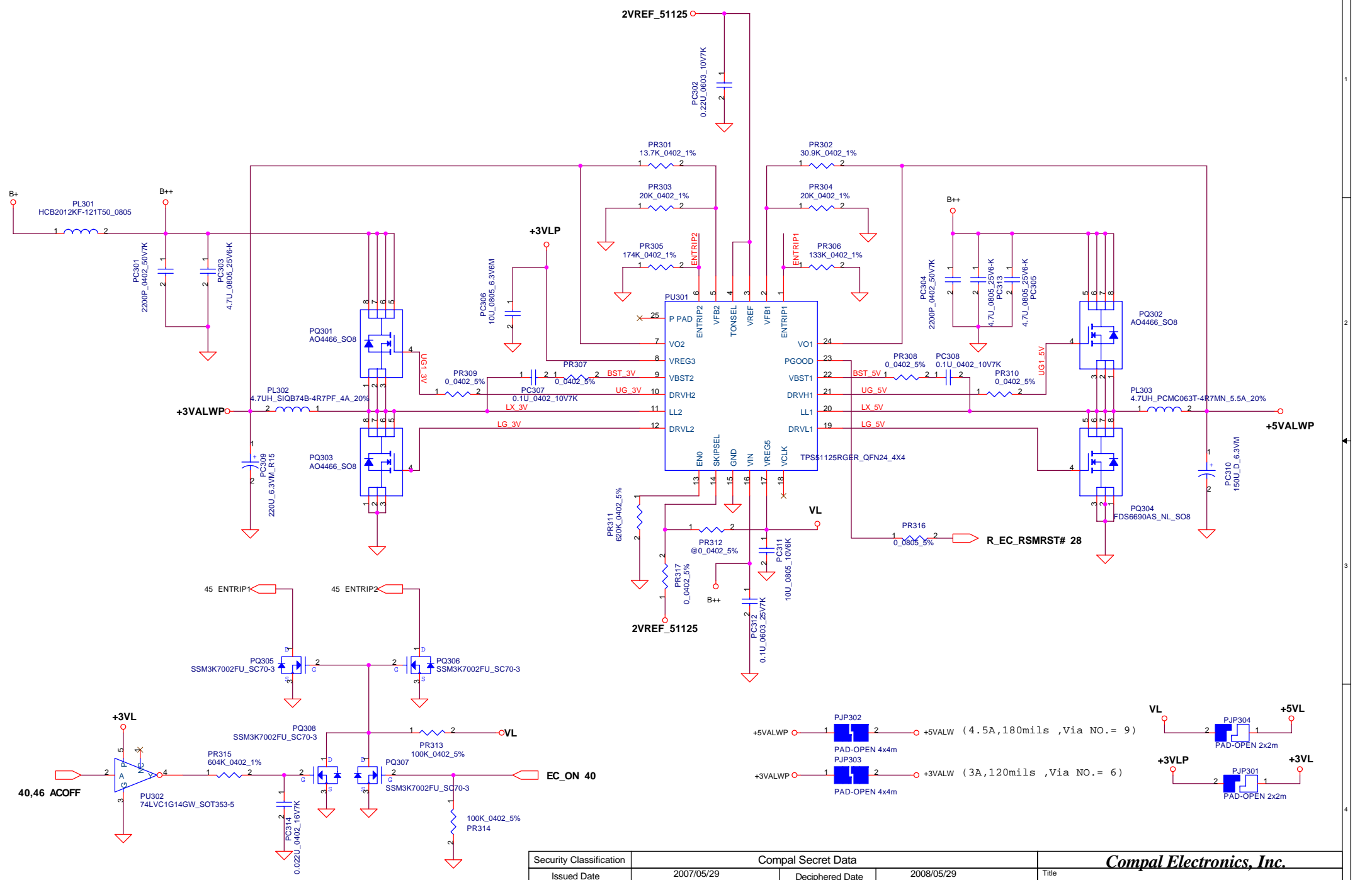
PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 47 +-3 degree C



Security Classification		Compal Secret Data		Compal Electronics, Inc. DC Connector/CPU OTP	
Issued Date	2007/05/29	Deciphered Date	2008/05/29		
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Date: Wednesday, December 26, 2007				Sheet	45 of 58

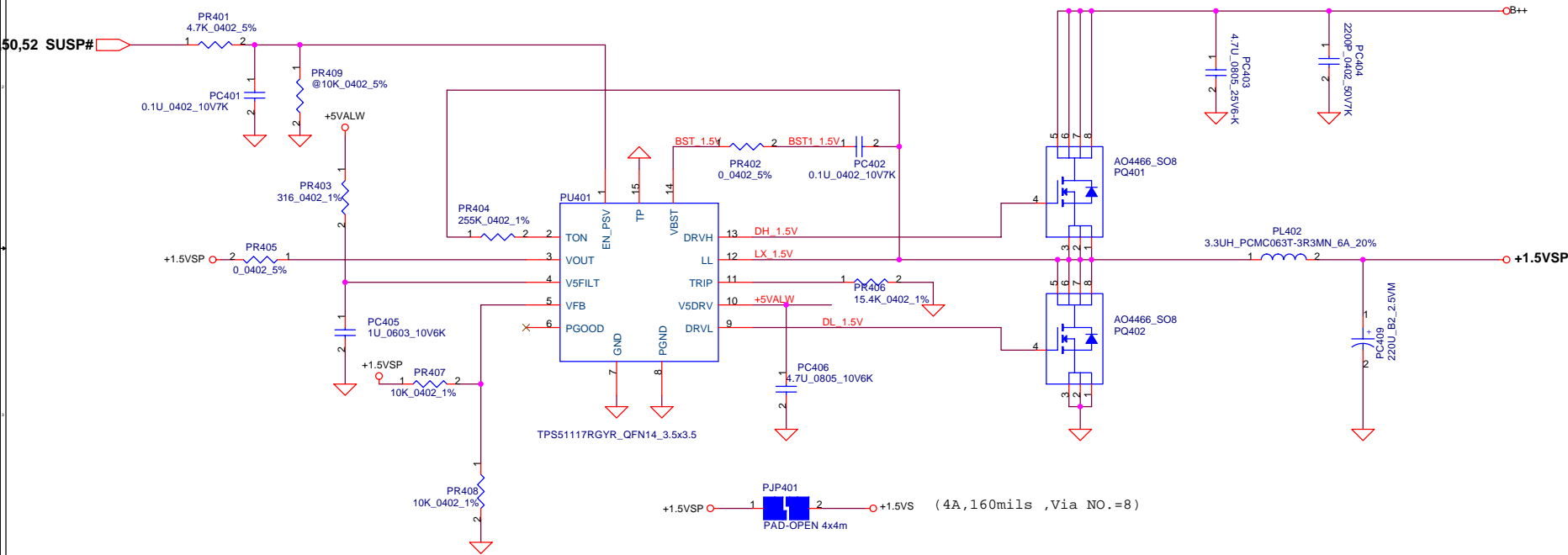


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Issued Date	2007/05/29	Deciphered Date	2008/05/29	Charger		
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Size	Document Number	Montevina Consumer Discrete		Rev	0.1	
Date:	Wednesday, December 26, 2007				Sheet	46 of 58

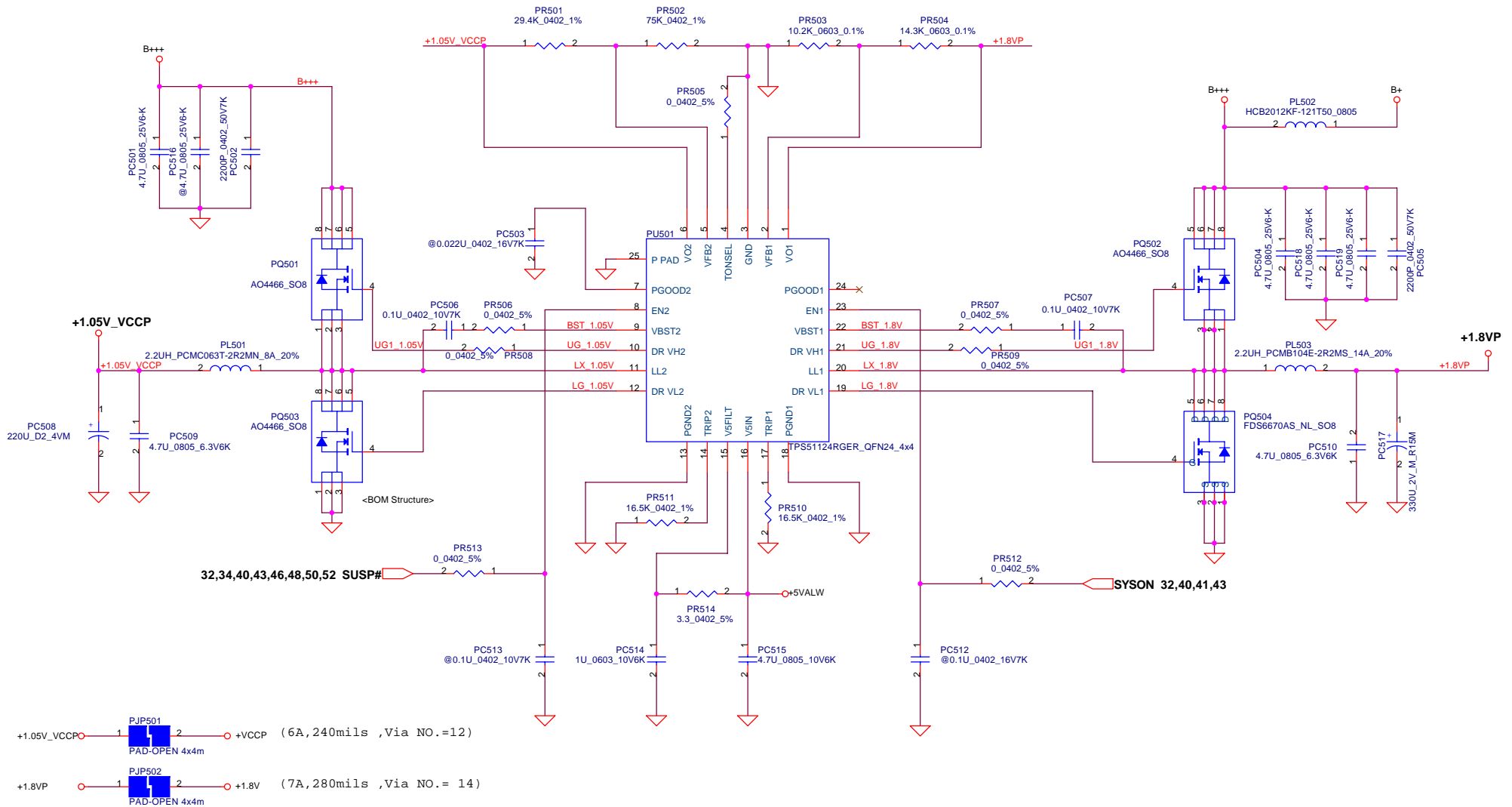


Security Classification		Compal Secret Data	
Issued Date	2007/05/29	Deciphered Date	2008/05/29
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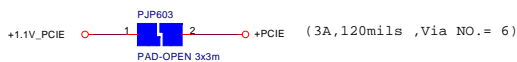
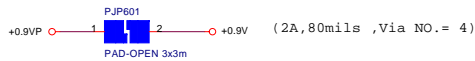
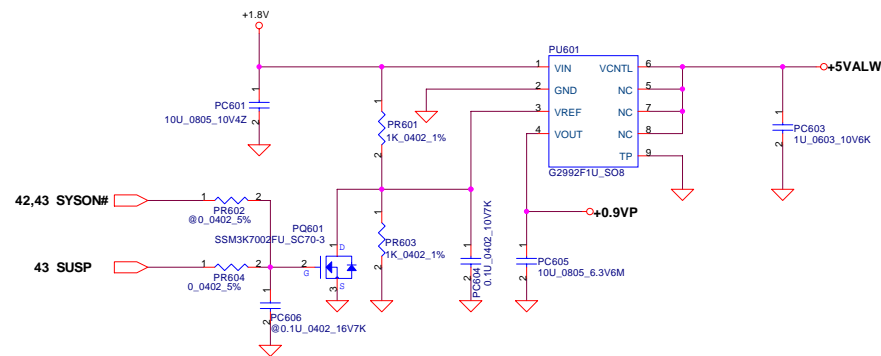
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Size			3.3VALWP/5VALWP		
Document Number			Montevina Consumer Discrete		
Date			Wednesday, December 26, 2007		
Sheet			47 of 58		
Rev			0.1		



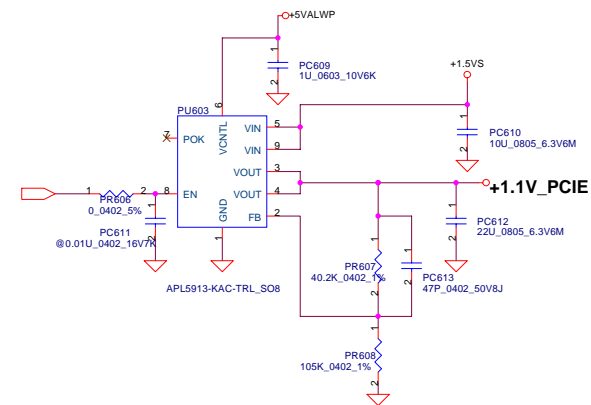
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				Date:	Wednesday, December 26, 2007	Sheet 48 of 58



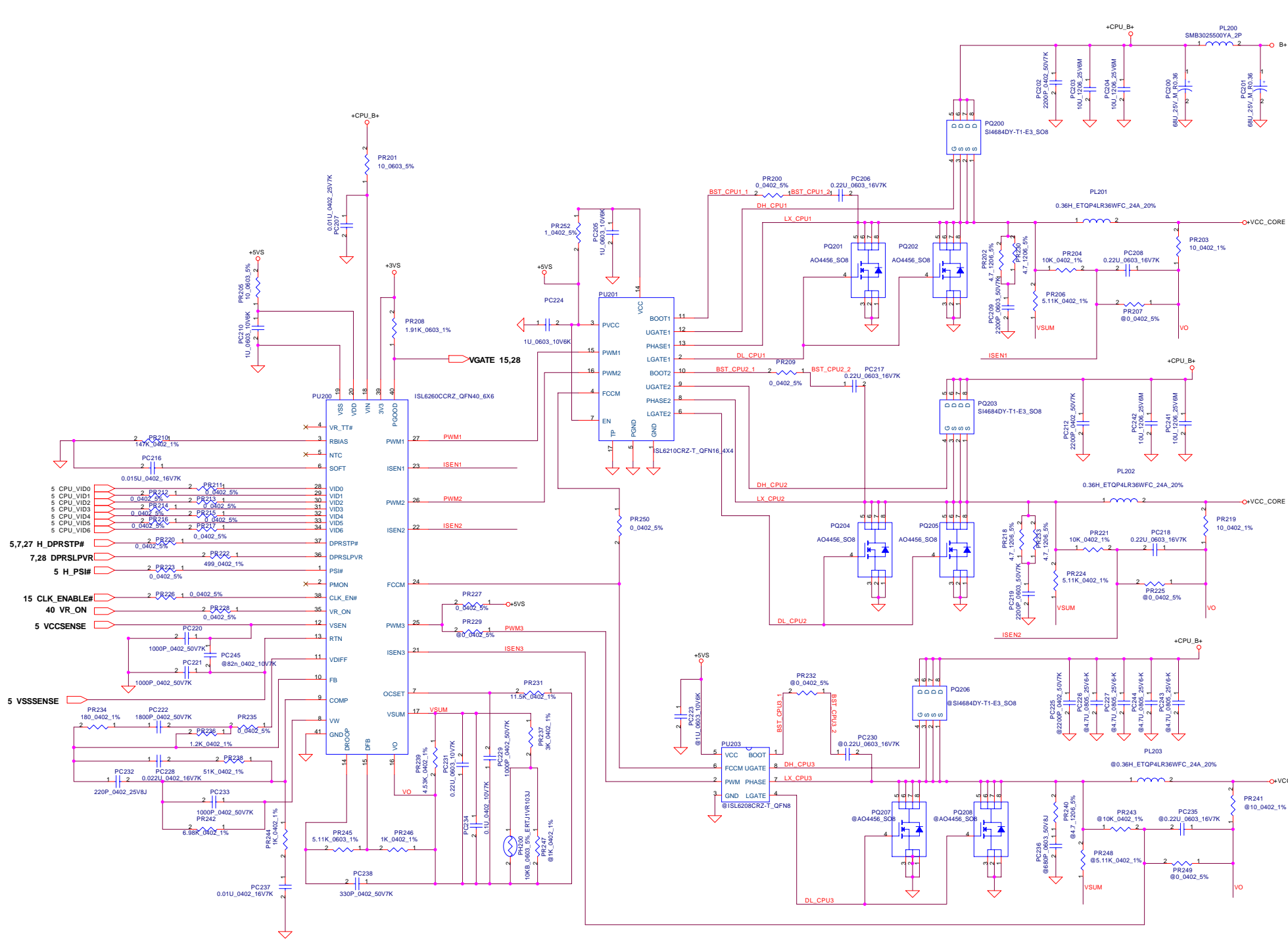
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				Montevina Consumer Discrete	
				Date:	Wednesday, December 26, 2007
				Sheet	49 of 58
				Rev	0.1



32,34,40,43,46,48,49,52 SUSP#



Security Classification	Compal Secret Data		Compal Electronics, Inc. 0.9VSP/2.5VSP/1.2V_PCIE Montevina Consumer Discrete	
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Date:	Wednesday, December 26, 2007	Sheet	50	of 58



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Size	C	Document Number	Montevina Consumer Discrete	
Date:	Wednesday, December 26, 2007	Sheet	51	of 58

Compal Electronics, Inc.

CPU CORE

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut in
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATi M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as luf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2

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				Date: Wednesday, December 26, 2007 Sheet 53 of 58

<2007.10.08>

<2007.10.09>

<2007.10.19>

<2007.10.20>

<2007.10.22>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1	Fix Audio disappear	follow Intel SB design suggestion to separate HDA Bus	27	Add R439, R440, R442, R444	0.2
2		Add to determine board type and project	28	Add R777, R776, R774, R775	0.2
		Meet EC request	28	non-stuff R419, R695	
3	Fix Audio disappear	follow Intel SB design suggestion	29	Change power rail from +1.5v to +3v	0.2
4		meet SW debug request	32	Add Debug CLK and PLT_RST#	0.2
5	Fix Audio disappear	follow Intel HDA bus design for Discrete platform	34	Change codec power rail from +1.5v to +3v	0.2
6	Fix can not power on issue	Meet EC and SPI access sequence	39	change SPI power rail from+3valw to +3VL	0.2
7		Follow Intel design guide	7	Change R30 value	0.2
1	Fix HDMI can not detect	follow Nvidia design request	18	change HDMI I2C channel to I2C B channel	0.2
2		Meet HP request to remove TV	18	Remove TV all components at VGA side	0.2
3		update ODD footprint	30	update JODD footprint	0.2
4	Fix ODD wrong pins	lower system power consumption	33	change Card Reader LED power rail	0.2
5		Meet Sub-woofer pwoer request	37	change D81, D82	0.2
6	Solve EC always damage	Solve EC always damage	40	change D53 direction	0.2
7		Double pull up and pwoer rail is different	41	Remove pull up resistors	0.2
8		lower system power consumption	41	change Cap-lock, HDD LED power rail	0.2
9		Meet HP request to remove TV	42	Remove TV all components at Dock side	0.2
10		lower system power consumption and meet LED status	43	Add +5VS_LED (Inculde DIM function)	0.2
11		solve HDMI pull up	44	update D79 footprint	0.2
1		Meet ME limit area at KBC	27	Change Y4 material	0.2
2		Follow IDT suuggestion	35	change R886 to 1206	0.2
3		Follow Nvidia suggestion	25	Change R193, R196 size to 0603	0.2
1		follow correct power rail	38	change Touch screen power rail	0.2
2		Meet HP request	39	Change ST G-sensor P/N & package	0.2
3		Meet HP request for WLAN &TV slot swap	32	Swapped WLAN and TV all support components	0.2
1		Change LAN chip to meet Energy star spec	31	change LAN brand to Realtek	0.2
2					

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	HW PIR(I)	
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				Custom	Montevina Consumer Discrete
				Date:	Wednesday, December 26, 2007
				Sheet	54 of 58
				Rev	0.1

<2007.10.23>

<2007.10.25>

<2007.10.31>

<2007.11.02>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1	Fix USB loading of SB	follow 14" Blade USB channel design	28	Chnage all USB channel	0.2
			17	Change USB channel of Camera	
			32	Change USB channel of WLAN & TV Tuner & New card	
			38	Change USB channel of Left side, Right side, E-SATA	
			38	Change USB channel of Touch screen, Finger print	
			42	Change USB channel of Dock	
2		Follow JMicro CardReader Vendor Suggestion	33	Change R114 & R1546 value	0.2
3		Solve Speak no sound issue	36	add pullup at HP_DET#	0.2
			36	Change Q203 to N-channel FET	
			34	Change R524 pin2 connect to JACK_DET#	
1		Meet HP request for QC and DC co-lay	4	add GTLREF and XDP circuits	0.2
			5		
			6		
2		Meet Intel request for CLK request	15	Add R127 to meet Intel CLK design	0.2
3		Solve G-sensor LED control	28, 41	change G-sensor LED control to GPIO19 of SB	0.2
4		Follow Capactivity board design	41	change Pin7 & 7 NET	0.2
1			34	Use Audio Codec GPIO5 to shutdown Sub-woofer	
2			40	Connect HDA_RST#_CODEC to EC	
3			34	Separate SPDIF out to VGA and Docking	
1		Common design	16	R204,R205 no stuff	0.3
			17	R642 size to 0805	0.3
			20	R2046,R2047 no stuff	0.3
			33	install R1553	0.3
			40	R616 no stuff	0.3
			40	Change R615 to 8.2k and add R2062	0.3
			40	Change HAD_RST#_CODEC from KBC pin 36 to pin 38	0.3
			41	Install R668, no install R667	0.3
			37	Add R2063	0.3

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				Custom	Montevina Consumer Discrete
Date: Wednesday, December 26, 2007				Sheet	55 of 58

<2007.11.04>

<2007.11.05>

<2007.11.06>

<2007.11.07>

<2007.11.08>

<2007.11.09>

<2007.11.12>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Move resistor from L54086P to MB	41	Add R2064	0.3
2		Change to dual type for layout space	16	Change Q69,Q70 to dual type	0.3
3		Only use LIS302DLTR	39	U77, R2025 no install	0.3
4		Change CIR_IN power rail	40	Connect R642.1 to +5VL	0.3
1		nVIDIA suggestion for NB9M-GS/GE	22	R1005 change to 475 ohm	0.3
2		nVIDIA suggestion -- add Pull up 2.2K on HDMIDAT_VGA and HDMICLK_VGA to +3VS. at VGA side	18	Add R2065,R2066	0.3
1	EMI request	CRT add resistor for EMI	16	Add R2069,R2070,R2071	0.3
2		HP suggestion	34	Change C746,C747,C748,C749 to 1000PF	0.3
3		USB camere power and add GPO pin for shutdown	17	Add PJP5,R2072,R2073	0.3
4		LAN DSM support	31	1. USB camera - SB GPIO20 2. ISOLATE - SB GPIO18 3. LAN OGPIO - SB GPIO14	0.3
5		EC_BEEP	34	Add R2076	0.3
6		G-sensor LED control by SB	41	Delete R668	0.3
1		Modify FPR connector pin assignment	38	Modify JP41 pin assignment	0.3
2		Modify Audio	34 36 37 42	1. Add C2108,C2109,R2080,R2081 2. Add R2082,R2083 3. Change C1008,C1009 to 1UF 4. Delete C976,C977 5. Delete R515,R516,C916 6. Change C982,C980,C984 from 5900p to 0.039u 7. Change C983,C992 from 1000p to 100p 8. Add EC_MUTE# to sub-woofer shutdown pin and R2084	0.3
3		nVIDIA suggestion	20	1. Delete strap pin 2. Change R1020, R1015, R1010 to 475 ohm 3. Swap THERMDN and THERMDP	0.3
1		EMI request	17	Add C2100,C2111	0.3
2		Audio	36 37	Change C970,C971 to 22uF, add C2112, change D38 to dual type	0.3
1		nVIDIA suggestion	19 20	Change HDMI DDC to I2CD R387,R388,R415,R422,R427 -- install Change R415 to 10 ohm and no install Delete R99, Change +IFPC_PLLVDD to +PCIE	0.3
2		JMicron suggestion	33	Do not install R2030 Add D86 for card reader wake up Add SB GPIO22 for wake up event	0.3
1		HP request	4	Add EMC1403 for Qaud core	0.3

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Date: Wednesday, December 26, 2007			Sheet 56 of 58	

Compal Electronics, Inc.

HW PIR(3)

Montevina Consumer Discrete

Sheet 56 of 58

<2007.12.12>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		MV DG for VDDC_QDAC	10	Chagne VCCD_QDAC to +1.5VS	0.4
2		WLAN issue	32	Change XMIT_OFF#,WL_LED# and component to WLAN connector	0.4
3		PCIE issue	28	Swap GLAN and NewCard PCIE port	0.4
4		Modify CardReader LED	33	Use 2N7002 to control LED	0.4
5		KBC	40	Change SMB_EC_DA1,SMB_EC_CK1 power rail from +5VL to +3VL Add C2118 for KBC pin124 Chagne EC_THERM power rail to +3VS	0.4
6		WL_BLUE_LED# issue	41	Add R2089 pull up for WL_BLUE_LED#	0.4
7		Power sequence	43	Add R2099,R2100,C2119 and Q89 change to dual type	0.4
8		DIM_LED	43	Delete Q97B,R211	0.4
9		EC_PME#	40	Change EC_PME# power rail to +3VALW	0.4
10		WLAN issue	28	Add R2101	0.4
11		Change TP power rail	41	Change TP power rail to +5VALW	0.4
12		G-sensor	41	G-sensor -- R2031 change to 470 ohm and pull up to +3VS	0.4
13		For Dock present	42	R1570 change to 22 ohm,R61 change to 2K ohm	0.4
14		Clock generator	15	Add series R2102,R2103 for 27M_SSC and 27M_CLK	0.4
15		HDCP ROM	19	R951 pull up,R959 no install	0.4
16		EMI request	17	C272,C273,C2120 -- 470pF C828,C798 -- 10pF C2111 -- 220pF Add D87	0.4
17		Modify BT/FPR circuit	38		0.4
<2007.12.24> 1		HP request	36 37	Change value	0.4
<2007.12.25> 1		For ENE cap board EMI issue	40	Add R and C	0.4

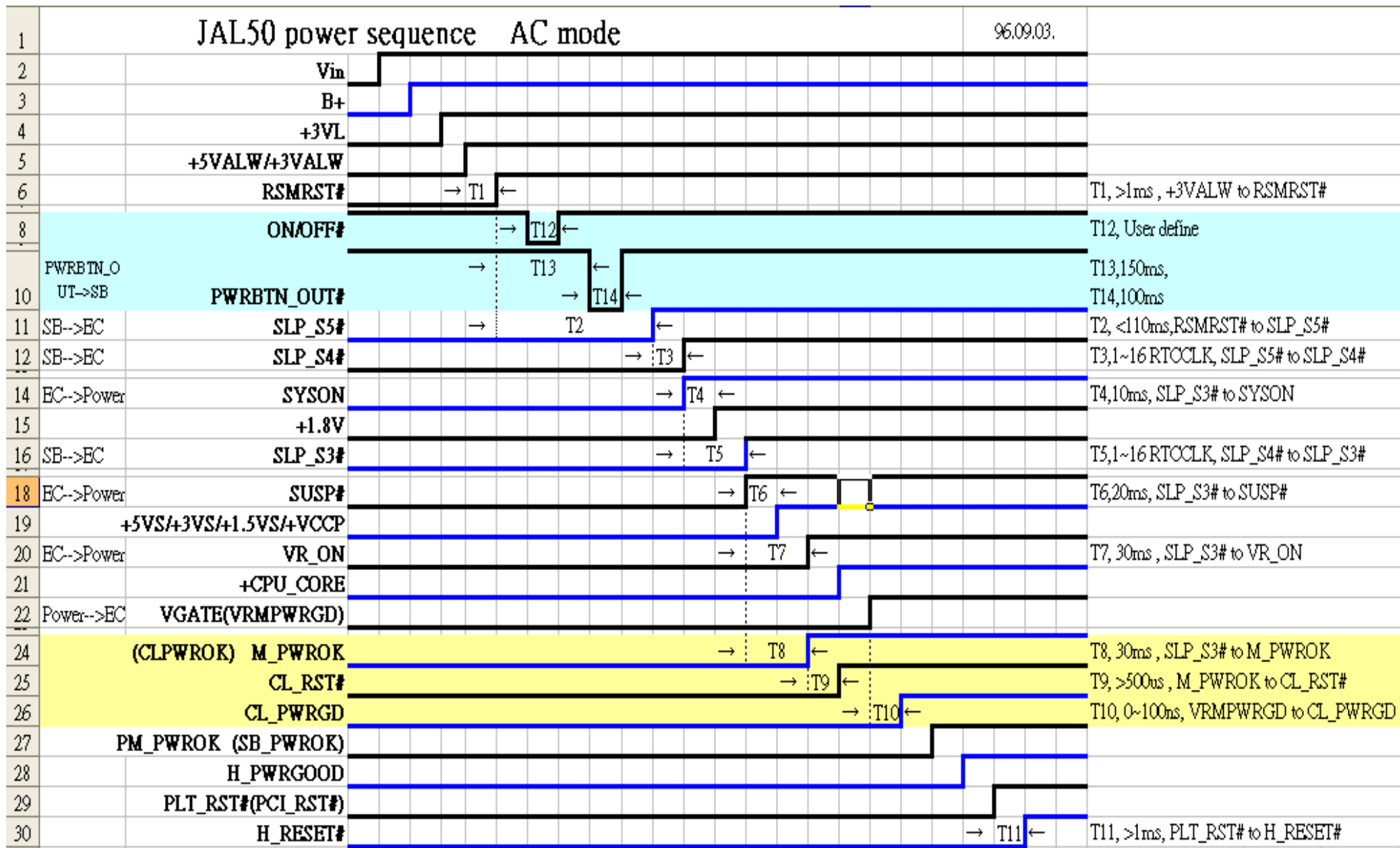
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HW PIR(4)
Montevina Consumer Discrete
Date: Wednesday, December 26, 2007 Sheet 57 of 58



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