TEA1733(L)

GreenChip SMPS control IC

Rev. 01.11 — 10 July 2009 Objective specification

1. General description

The TEA1733 is a low cost Switched Mode Power Supply (SMPS) controller IC intended for flyback topologies.

The TEA1733 operates in fixed frequency mode. To reduce EMI, frequency jitter has been implemented. For Continuous Conduction Mode (CCM) operation, slope compensation is integrated. The controller can be set to accept an over-power situation for a limited amount of time.

Two pins are reserved for protection purposes. Input under and over voltage protection, output over voltage protection and over temperature protection can be implemented with a minimal number of external components.

At low power levels the primary peak current is set to 25% of the maximum peak current and the switching frequency is reduced to limit the switching losses.

The combination of fixed frequency operation at high output power and frequency reduction at low output power provides high efficiency over the total load range.

The TEA1733 enable low cost, highly efficient and reliable supplies for power requirements up to 75 W to be designed easily and with a minimum number of external components.

2. Features

2.1 Features

- SMPS controller IC enabling low cost applications
- Large input voltage range (12V up to 30V)
- Very low supply current during start-up and restart (typ. 10µA)
- Low supply current during normal operation (typ. 500µA without load)
- Over-power compensation
- Adjustable over-power time-out
- Adjustable over-power restart timer
- Fixed switching frequency with frequency jitter to reduce EMI
- Frequency reduction with fixed minimum peak current at low power operation to maintain high efficiency at low output power levels
- Slope compensation for CCM operation
- Low and adjustable over current protection (OCP) trip level
- Soft start

founded by Philips

- Two protection inputs (e.g. for input under voltage and over voltage protection, over temperature protection and output over voltage protection)

3. Applications

- The devices can be used in all applications that require an efficient and cost-effective power supply solution up to 75 W.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1733	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram

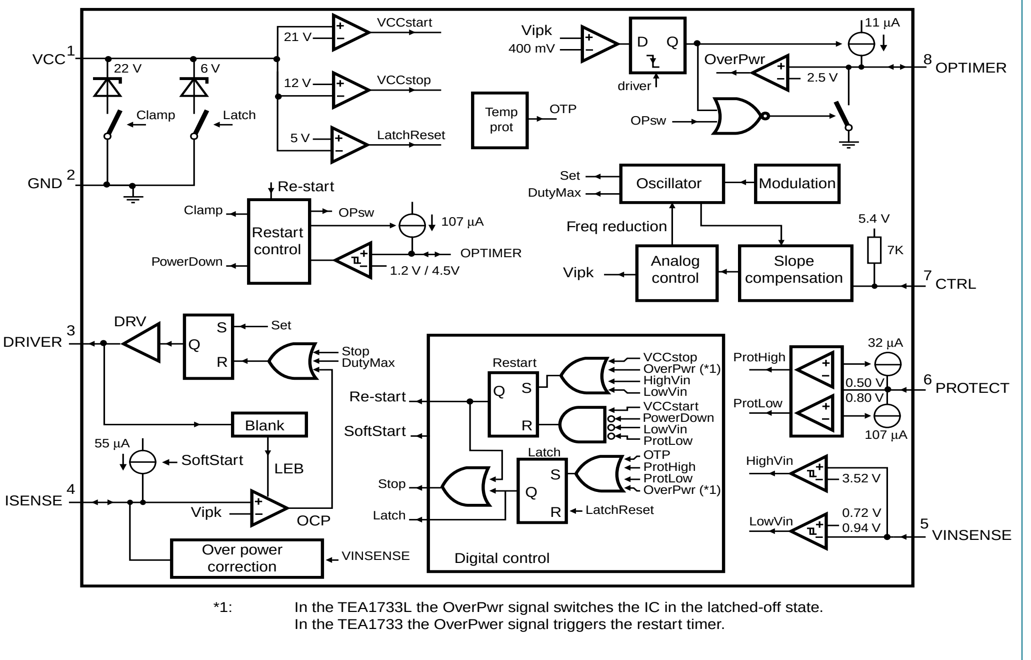


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

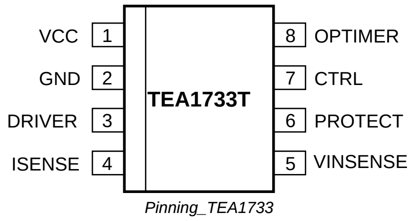


Fig 2. Pin configuration: TEA1733 (SOT96-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VCC	1	supply voltage
GND	2	ground
DRIVER	3	gate driver output
ISENSE	4	current sense input
VINSENSE	5	input voltage protection input
PROTECT	6	general purpose protection input
CTRL	7	duty cycle control input
OPTIMER	8	over-power and restart timer

7. Functional description

7.1 General control

The TEA1733 contains a controller for a flyback circuit. A typical configuration is shown in Figure 3.

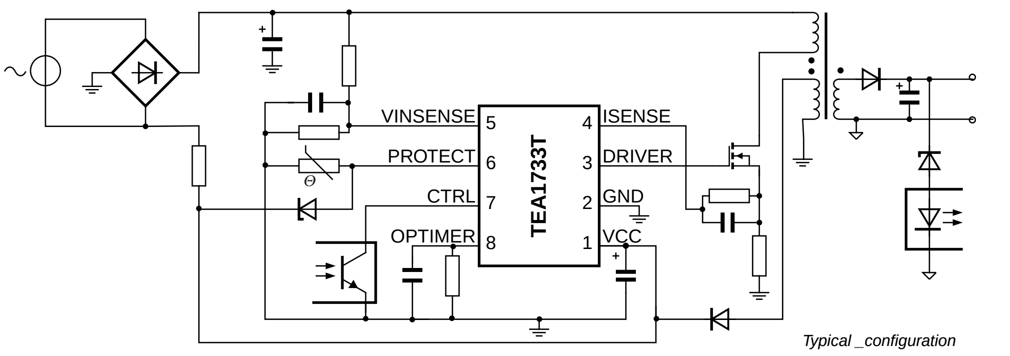


Fig 3. Typical configuration

7.2 Start-up and under voltage lock-out

Initially the capacitor on the VCC pin is charged from the high voltage mains via a resistor.

As long as V_{CC} is below $V_{startup}$, the IC current consumption is low (typ. 10μA). When V_{CC} reaches $V_{startup}$ the IC first waits for the VINSENSE pin to reach the $V_{low(VINSENSE)}$ voltage and for the PROTECT pin to reach the $V_{low(PROTECT)}$ voltage. When both level are reached, the IC charges the ISENSE pin to the $V_{start(soft)}$ level and than starts switching. In a typical application the supply voltage is taken over by the auxiliary winding of the transformer.

If a protection is triggered the controller will stop switching. Dependent on which protection is triggered and dependent on the version of the IC (TEA1733 or TEA1733L) the protection will cause a re-start or will latch the converter in an off-state.

A re-start caused by a protection will charge the OPTIMER pin to 4.5V (typ.) rapidly. The TEA1733 will than enter the power-down mode until the OPTIMER pin is discharged to 1.2V (typ.). During the power-down mode, the IC consumes a very low supply current (10μA typ.) and the VCC pin will be clamped to 22V (typ) by an internal clamp circuit. A restart will be made when the voltage on pin OPTIMER drops below 1.2V (typ.) and the VCC pin voltage is above the VCC start-up voltage.

When a latched protection is triggered, the TEA1733 will enter the power-down mode immediately. The VCC pin will be clamped to a voltage just above the latch protection reset voltage ($V_{reset(Latch)}$+1V) (See Figure 4)

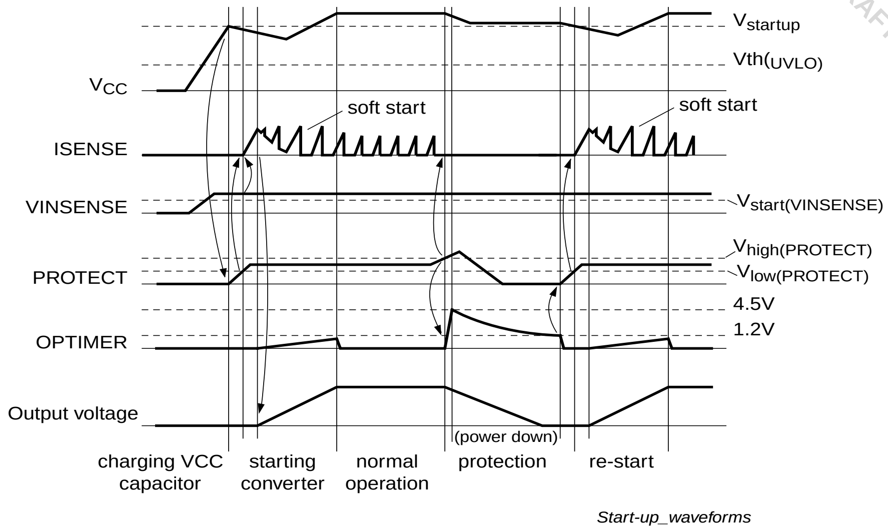


Fig 4. Start-up sequence, normal operation and re-start sequence

When the voltage on pin V_{CC} drops below the under voltage lock-out level during normal operation, the controller stops switching and enters the re-start mode. In the re-start mode the driver output is disabled and the VCC pin voltage is recharged via the resistor to the rectified mains.

7.3 Supply management

All internal reference voltages are derived from a temperature compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature compensated current reference circuit.

7.4 Input voltage detection (VINSENSE pin)

In a typical application the mains input voltage can be detected by the VINSENSE pin. As long as the voltage on VINSENSE has not reached the $V_{start(VINSENSE)}$ voltage (typ. 0.93V), switching is inhibited.

When during operation the VINSENSE voltage drops below $V_{low(VINSENSE)}$ (typ. 0.72V) or exceeds $V_{high(VINSENSE)}$ (typ.3.52V), the converter stops switching and performs a restart.

If the pin is left open or disconnected, the pin is pulled up by the internal 20nA (typ.) current source and subsequently the $V_{high(VINSENSE)}$ level is reached. This will than trigger a restart protection.

An internal clamp of 4.6 volts (typ.) protects this pin from excessive voltages.

7.5 Protection input (PROTECT PIN)

Pin PROTECT is a general purpose input pin, which can be used to switch off the converter (latched protection). The converter is stopped as soon as the voltage on this pin is pulled above $V_{high(PROTECT)}$ (typ. 0.8 V) or below $V_{low(PROTECT)}$ (typ. 0.5 V). A current of 32μA (typ.) is flowing out of the chip when the pin voltage is $V_{low(PROTECT)}$. A current of 107μA (typ.) is flowing into the chip when the pin voltage is $V_{high(PROTECT)}$.

The PROTECT input can be used e.g. for creating an over voltage detection and over temperature protection function.

The pin can be left not connected if it is not used.

An internal clamp of 4.1 volts (typ.) protects this pin from excessive voltages.

7.6 Duty cycle control (CTRL pin)

The output power of the converter is regulated by the CTRL pin. The pin CTRL is connected to an internal voltage source of 5V via an internal resistor (typical resistance is 7kΩ)

The CTRL pin voltage sets the maximum peak current which is measured via the ISENSE pin. (see Section 7.10) At low output power also the switching frequency is reduced. (see Section 7.12)The maximum duty cycle is limited to 72% (typ).

7.7 Slope compensation (CTRL pin)

For continuous conduction mode (CCM) a slope compensation circuit is integrated. The slope compensation guarantees stable operation for duty cycles larger than 50%.

7.8 Over power timer (OPTIMER pin)

If the OPTIMER pin is connected to a capacitor a temporary over-load situation is allowed. If Vocp (see Figure 1) set by the CTRL pin is above 400mV, a current of $I_{OPTIMER}$ (10μA typ.) is sourced from the OPTIMER pin. If the voltage on the OPTIMER pin reaches the $V_{OPTIMER(prot)}$ voltage (2.5V typ.) the over-power protection is triggered. (see Figure 5)

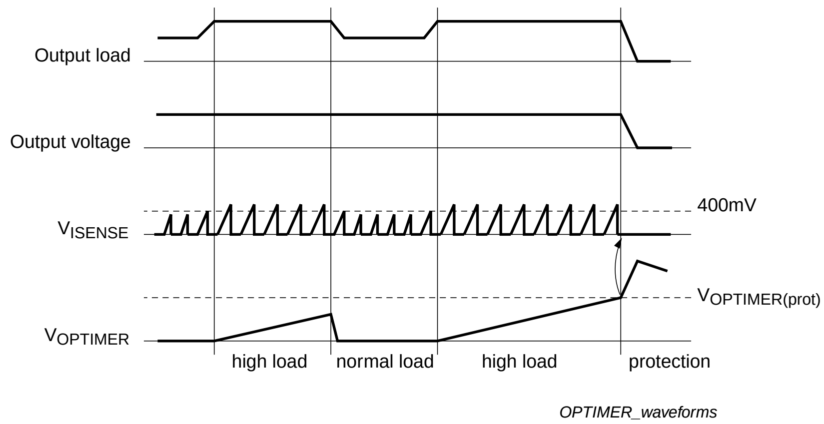


Fig 5. Over power delay

When the $V_{OPTIMER(prot)}$ voltage is reached a restart will be made.

If the over-load is removed before the $V_{OPTIMER(prot)}$ voltage is reached, the converter will continue switching.

7.9 Current mode control (ISENSE pin)

Current mode control is used for its good line regulation.

The primary current is sensed by the ISENSE pin across an external resistor and compared with an internal control voltage.The internal control voltage is proportional to the CTRL pin voltage. (see Figure 6)

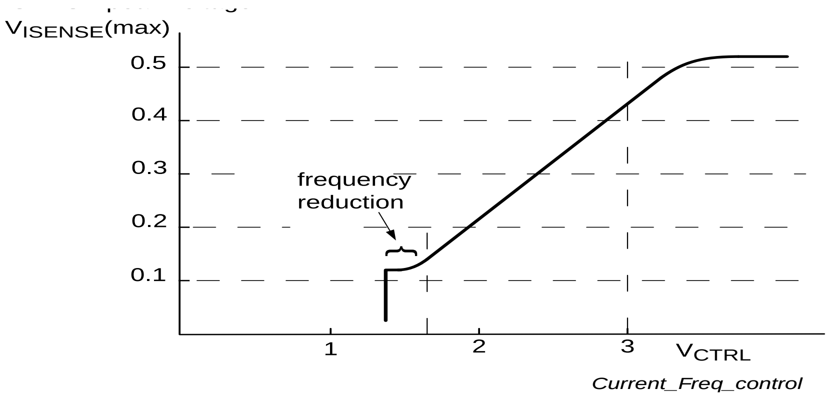


Fig 6. Peak current control

Leading edge blanking is added to prevent false triggering due to the capacitive discharge when switching on the external power switch. (see Figure 7)

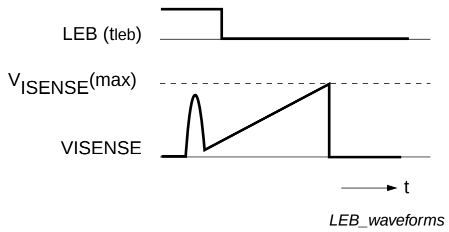


Fig 7. Leading edge blanking

7.10 Over power compensation (VINSENSE and ISENSE pin)

The over power compensation function can be used to realize a maximum output power which is nearly constant over the full input mains.

The over power compensation circuit measures the input voltage via the VINSENSE pin and outputs a current dependent on this voltage on the ISENSE pin. The DC voltage across the soft start resistor will than limit the maximum peak current on the current sense resistor.

At low output power levels the over power compensation circuit is switched off.

See Figure 8.

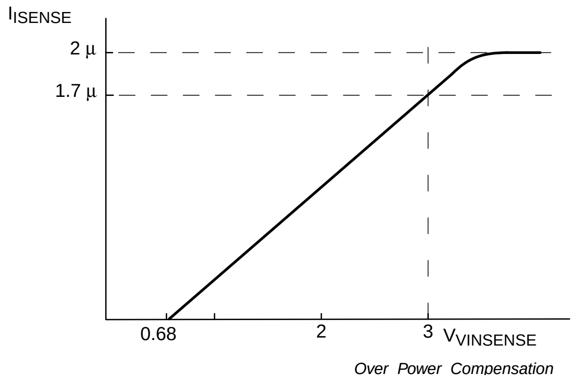


Fig 8. Over power compensation

7.11 Soft start-up (ISENSE pin)

To prevent audible noise during start-up or re-start, a soft start is made. Before the converter (re-)starts, the soft-start capacitor on the ISENSE pin is charged. When the converter (re-) starts switching, the primary peak current increases slowly when the soft start capacitor discharges through the soft start resistor. (see also Figure 4)

The time constant of the soft start can be chosen by setting the soft start capacitor. Also the soft start resistor must be taken into account, but this value is typically defined by the over power compensation. (see Section 7.10)

7.12 Low power operation

In low power operation the switching losses are reduced by lowering the switching frequency. The switching frequency of the converter is reduced while the peak current is set to 25% of the maximum peak current. (see Figure 6 and Figure 9)

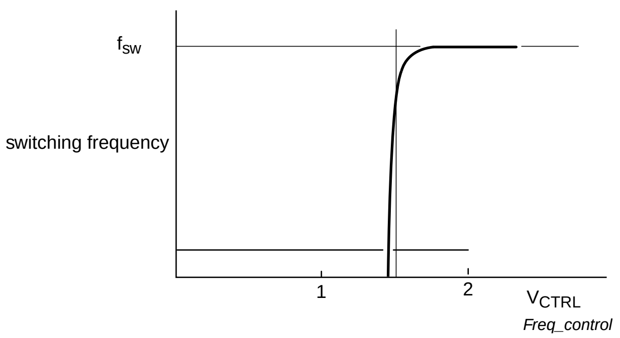


Fig 9. Frequency control

7.13 Driver (pin DRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically –250 mA and a current sink capability of typically 750 mA. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

7.14 Over Temperature Protection (OTP)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the IC stops switching.

OTP is a latched protection. It can be reset by removing the voltage on pin VCC.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage		−0.4	+30	V
$V_{VINSENSE}$	voltage on pin VINSENSE	current limited	−0.4	+5	V
$V_{PROTECT}$	voltage on pin PROTECT	current limited	−0.4	+5	V
V_{CTRL}	voltage on pin CTRL		−0.4	+5	V
$V_{OPTIMER}$	voltage on pin OPTIMER		−0.4	+5	V
V_{ISENSE}	voltage on pin ISENSE	current limited	−0.4	+5	V
Currents					
$I_{VINSENSE}$	current on pin VINSENSE		−1	+10	mA
$I_{PROTECT}$	current on pin PROTECT		−1	+1	mA
I_{CTRL}	current on pin CTRL		−3	0	mA
I_{ISENSE}	current on pin ISENSE		−1	+10	mA
$I_{FBDRIVER}$	current on pin DRIVER	d < 10 %	−0.4	+1	A
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.5	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C
ESD					
V_{ESD}	electrostatic discharge voltage	class 1			
	human body model	[1]	-	2000	V
	machine model	[2]	-	200	V
	charged device model		-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	150	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air; JEDEC test board	79	K/W

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 6); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin VCC)						
$V_{startup}$	start-up voltage		18.6	20.6	22.6	V
$V_{th(UVLO)}$	under voltage lockout threshold voltage		11.2	12.2	13.2	V
$V_{clamp(VCC)}$	Clamp voltage on pin VCC	Activated during restart Activated during latched protection		$V_{startup}$ +1 V_{reset} (latch) +1		V
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	891		0	V
$I_{CC(startup)}$	startup supply current	$V_{CC} < V_{startup}$	51	0	15	µA
$I_{CC(oper)}$	operating supply current	no load on pin DRIVER	0.4	0.5	0.6	mA
$V_{reset\ (latch)}$	latched protection reset voltage		456V			
Input Voltage Sensing (pin VINSENSE)						
$V_{start(VINSENSE)}$	Input voltage detection level		0.89	0.94	0.99	V
$V_{low(VINSENSE)}$	Low input voltage detection level		0.68	0.72	0.76	V
$V_{high(VINSENSE)}$	High input voltage detection level		3.39	3.52	3.65	V
$I_{O(VINSENSE)}$	output current in pin VINSENSE			-20		nA
$V_{clamp(VINSENSE)}$	Clamp voltage on pin VINSENSE	$I_{VINSENSE}$=50µA4		.6		V
Protection input (pin PROTECT)						
$V_{low(PROTECT)}$	low protection voltage		0.47	0.50	0.53	V
$V_{high(PROTECT)}$	high protection voltage		0.75	0.8	0.85	V
$I_{O(PROTECT)}$	output current on pin PROTECT	$V_{VINSENSE}=V_{low(PROTECT)}$	–34	–32	–30	µA
		$V_{VINSENSE}=V_{high(PROTECT)}$	87	107	127	µA
$V_{clamp(PROTECT)}$	Clamp voltage on pin PROTECT	$I_{PROTECT}$=200µA [1]	3.5	4.1	4.7	V

Table 5. Characteristics *...continued*

T_{amb} =2 5 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 6); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Peak current control (pin CTRL)						
V_{CTRL}	voltage on pin CTRL	for minimum flyback peak current	1.5	1.8	2.1	V
		for maximum flyback peak current	3.4	3.9	4.3	V
$R_{int(CTRL)}$	internal resistance on pin CTRL		579k			Ω
$I_{O(CTRL)}$	output current on pin CTRL	V_{CTRL}=1.4V	–0.7	–0.5	–0.3	mA
		V_{CTRL}=3.7V	–0.28	–0.2	–0.12	mA
Pulse width modulator						
f_{osc}	oscillator frequency		62	66.5	71	kHz
f_{mod}	modulator frequency		210	280	350	Hz
$f_{(range)mod}$	frequency modulator range		+/-3	+/-4	+/-5	kHz
δ_{max}	maximum duty cycle		68.5	72	79	%
$V_{start(red)freq}$	frequency reduction start voltage on pin CTRL		1.5	1.8	2.1	V
$V_{\delta(zero)}$	zero duty cycle voltage on pin CTRL		1.25	1.55	1.85	V
Over power protection (pin OPTIMER)						
$V_{OPTIMER(prot)}$	protection voltage on pin OPTIMER		2.4	2.5	2.6	V
$I_{OPTIMER(prot)}$	over-power protection current	no over-power situation	100	150	200	μA
		over-power situation	–12.2	–10.7	–9.2	μA
Re-start timer (pin OPTIMER)						
$V_{OPTIMER(restart)}$	re-start voltage on pin OPTIMER	low level	0.8	1.2	1.6	V
		high level	4.1	4.5	4.9	V
$I_{OPTIMER(restart)}$	re-start current on pin OPTIMER	charging OPTIMER capacitor	–127	–107	–87	μA
		discharging OPTIMER capacitor	–0.1	0	0.1	μA
Current sense (pin ISENSE)						
$V_{sense(max)}$	maximum sense voltage	$\Delta V/\Delta t$=5 0 mV/μs, $V_{VINSENSE}$=0.78V	0.48	0.51	0.54	V
		$\Delta V/\Delta t$=2 00m V/μs $V_{VINSENSE}$=0.78V	0.50	0.53	0.56	V
$V_{sense(max)opp}$	Over power protection maximum sense voltage		370	400	430	mV
$\Delta V_{ISENSE}/\Delta t$	slope compensation voltage on ISENSE pin	17		25	33	mV /μs
$t_{leb(fb)}$	leading edge blanking time		250	300	350	ns
Over power compensation (pin VINSENSE and pin ISENSE)						
$I_{opc(ISENSE)}$	Over power correction current on pin ISENSE	$V_{VINSENSE}$=1V, $V_{sense(max)}$>400mV		0.28		μA

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 6); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{VINSENSE}$=3V $V_{sense(max)}$>400mV		1.7		µA
Soft start (pin ISENSE)						
$I_{start(soft)}$	soft start current		–63	–55	–47	µA
$V_{start(soft)}$	soft start voltage	V_{CTRL}=4V enable voltage		$V_{sense(max)}$		V
$R_{start(soft)}$	soft start resistance		12			kΩ
Driver (pin DRIVER)						
$I_{src(DRIVER)}$	driver source current on pin DRIVER	V_{DRIVER} =2V	-	–0.3	-0.25	A
$I_{sink(DRIVER)}$	driver sink current on pin DRIVER	V_{DRIVER} = 2 V	0.25	0.3	-	A
		V_{DRIVER} = 10 V	0.6	0.75	-	A
$V_{O(DRIVER)max}$	maximum output voltage on pin DRIVER		91	0.5	12	V
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C

[1] The clamp voltage on the PROTECT pin is lowered when the IC is in power down. (latched or restart protection)

11. Application information

A power supply with the TEA1733(L) is a flyback converter operating in continuous conduction mode. See Figure 10.

Capacitor C5 buffers the IC supply voltage, which is powered via R3 for start-up and via the auxiliary winding during normal operation. Sense resistor R9 converts the current through the MOSFET S1 into a voltage at pin 4 (ISENSE). The values of R9 defines the maximum primary peak current in MOSFETS S1.

In the example given, the PROTECT pin (pin 6) is used for over-voltage protection (OVP) and over temperature protection (OTP). The OVP level is set by Z1 to V_{VCC} = 25.8 V, the OTP level is set by NTC resistor R4. The VINSENSE pin (pin 5) is used for mains under voltage lock-out and is set by R1 and R2 to about 80 Vac. The over-power protection time, defined by C4, is set to 60msec.

The restart time, defined by C4 and R8, is set to 0.5 sec.

R6 and C6 define the soft-start time. R5 is added to prevent the soft-start capacitor from being charged during normal operation due to negative voltage spikes across the current sense resistor R9.

C3 is added to reduce the noise on the CTRL pin. R7 reduces the peak current to C5.

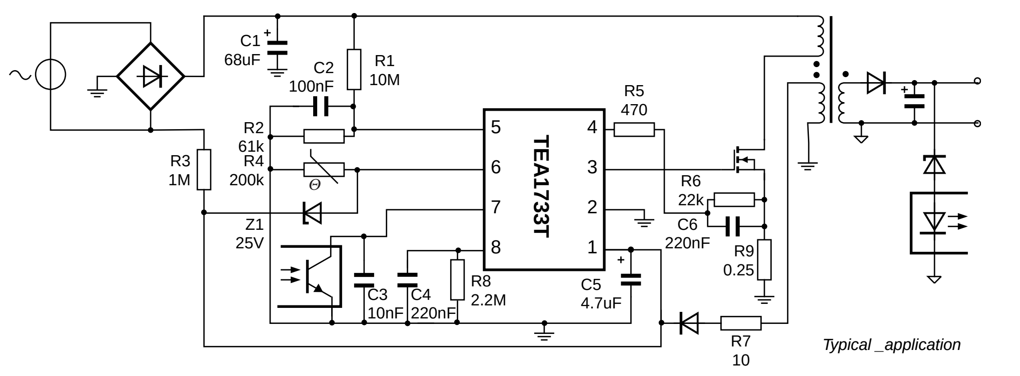


Fig 10. Typical application

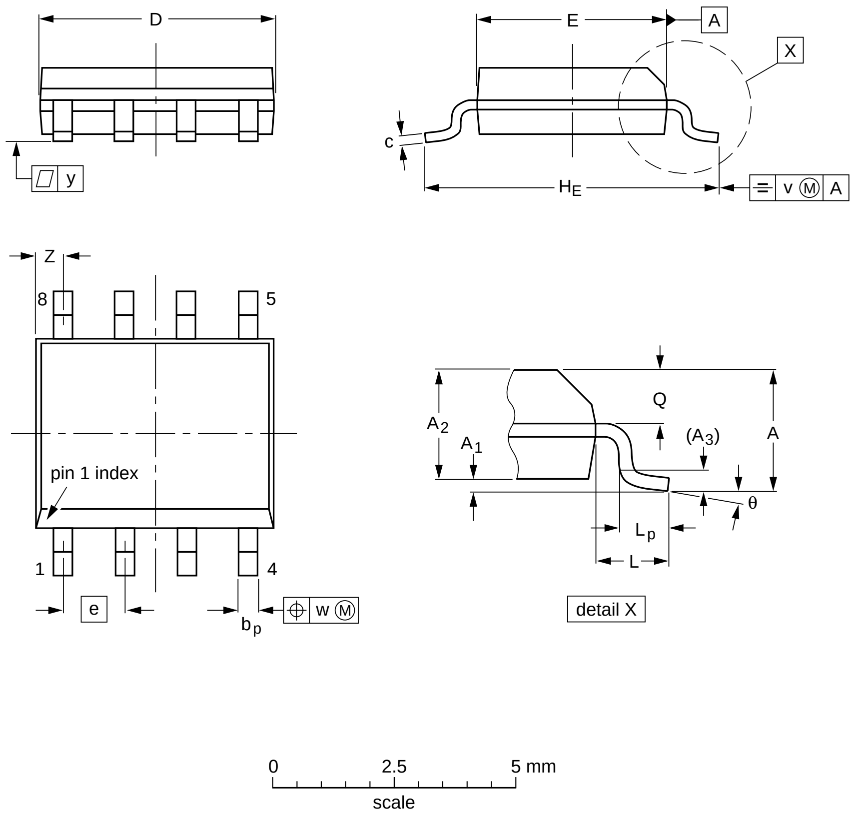
12. Test information

12.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	QZ	v	w	y	(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT109-1 (SO16)

14. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1733_01.11	version 01.11	Objective specification	-	TEA1733_01.10
-	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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