# Green-Mode PWM Controller with Frequency Swapping and Integrated Protections

*Rev. 00*

## General Description

The LD5530 is built-in with several functions, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features more protections like OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the Frequency Swapping function is to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

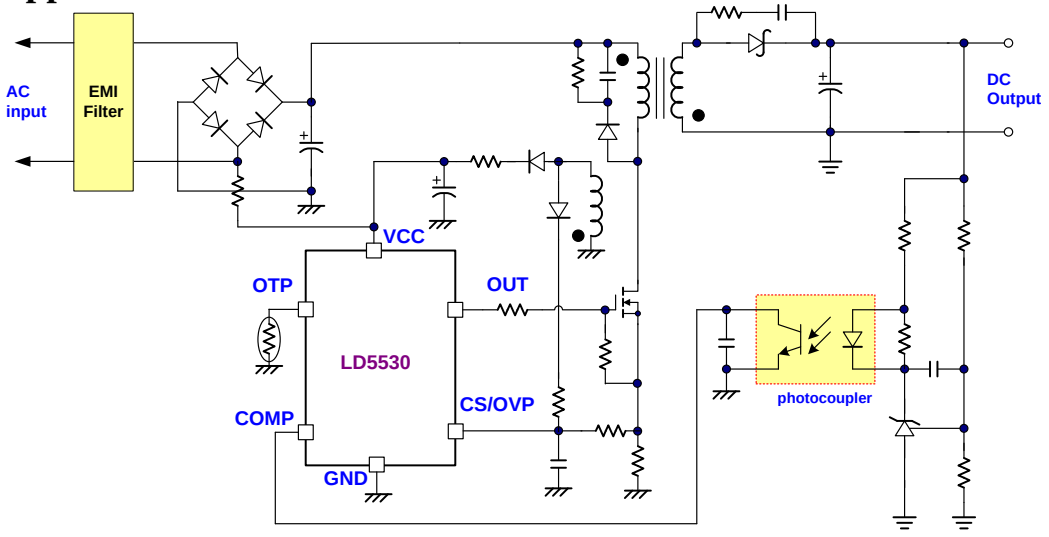
## Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<1μA)
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- Adjustment OVP(Over Voltage Protection) on CS Pin
- Adjustment OCP(Over Current Protection) on CS Pin
- OTP (Over Temperature Protection) through a NTC
- OLP (Over Load Protection)
- 250/-500mA Driving Capability

## Applications

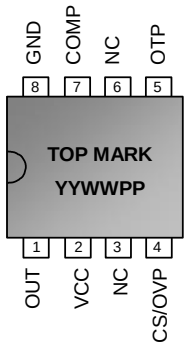
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

## Typical Application

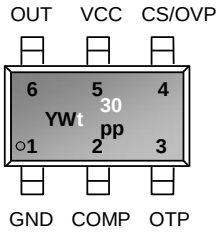


## Pin Configuration

DIP-8 (TOP VIEW)




SOT-26 (TOP VIEW)




YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
t30R : LD5530

## Ordering Information

| Part number | Package | Top Mark | Shipping |
|---|---|---|---|
| LD5530 GL | SOT-26 | YWt/30 | 3000 /tape & reel |
| LD5530 GN | DIP-8 | LD5530 GN | 3600 /tube /Carton |

The LD5530 is ROHS compliant / Green Packaged

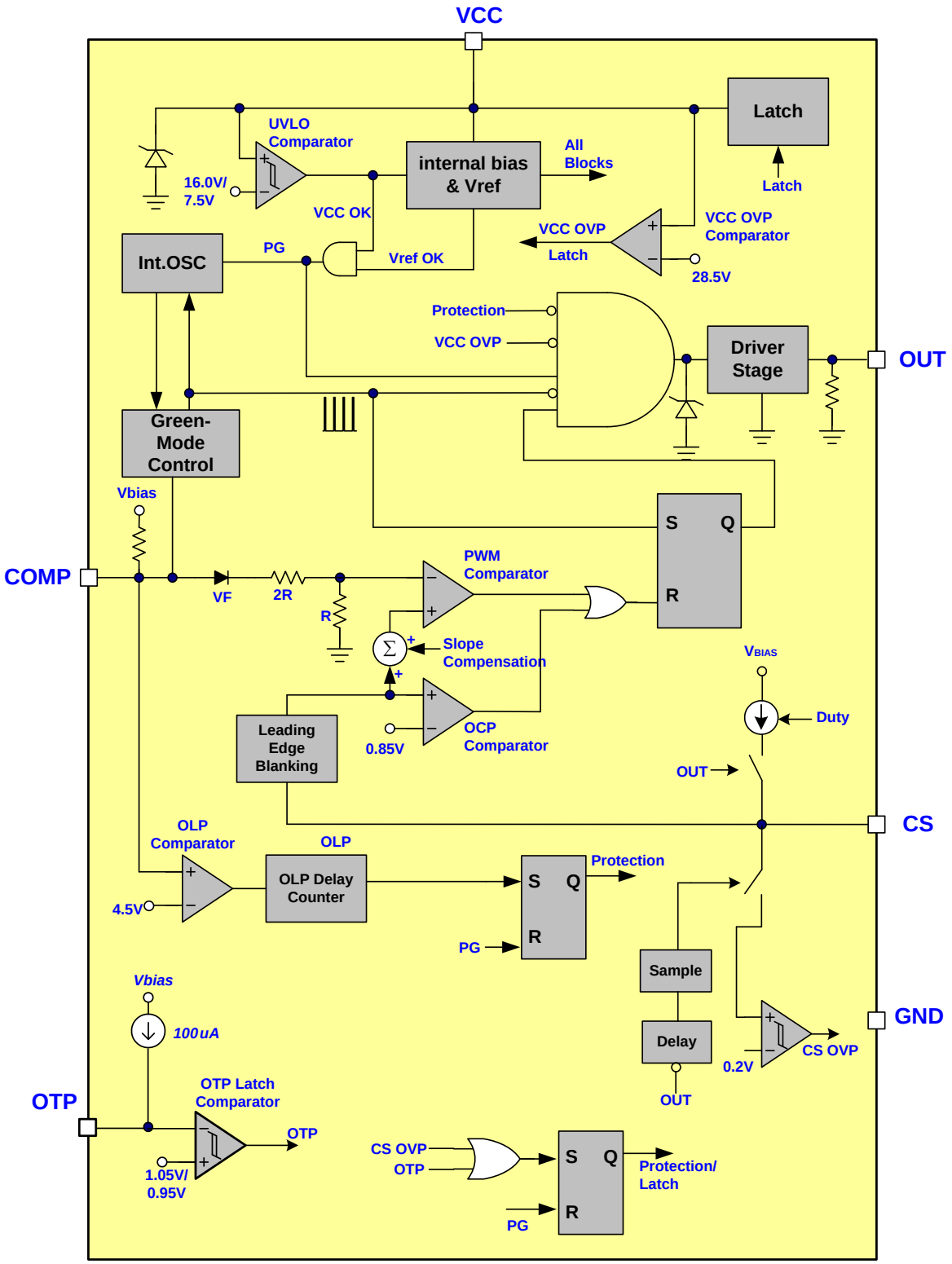
## Protection Mode

| Switching Freq. | OLP | VCC OVP | CS OVP | OTP Pin |
|---|---|---|---|---|
| 65kHz | Auto recovery | Latch | Latch | Latch |

## Pin Descriptions

| SOT-26 | DIP-8 | NAME | FUNCTION |
|---|---|---|---|
| 1 | 8 | GND | Ground |
| 2 | 7 | COMP | Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation. |
| 3 | 5 | OTP | Pull this pin below 0.95V to shut down the controller into latch mode until the AC resumes power-on. Connecting this pin to ground with NTC will achieve OTP protection. Let this pin float or connect a 100kΩ resistor to disable the latch protection. |
| 4 | 4 | CS/OVP | Current sense pin, connect it to sense the MOSFET current. This pin is also connected to an auxiliary winding of the PWM transformer through a resistor and a diode for output over-voltage protection. |
| 5 | 2 | VCC | Supply voltage pin |
| 6 | 1 | OUT | Gate drive output to drive the external MOSFET |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage VCC | -0.3V ~30V |
| COMP, OTP, CS | -0.3V ~6V |
| OUT | -0.3V ~Vcc+0.3V |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | -65°C to 150°C |
| Package Thermal Resistance (SOT-26, $\theta_{JA}$) | 200°C/W |
| Package Thermal Resistance (DIP-8, $\theta_{JA}$) | 100°C/W |
| Power Dissipation (SOT-26, at Ambient Temperature = 85°C) | 200mW |
| Power Dissipation (DIP-8, at Ambient Temperature = 85°C) | 400mW |
| Lead temperature (Soldering, 10sec) | 260°C |
| ESD Voltage Protection, Human Body Model | 2.5 KV |
| ESD Voltage Protection, Machine Model | 250 V |

**Caution:**

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability

## Recommended Operating Conditions

| Item | Min. | Max. | Unit |
|---|---|---|---|
| Operating Ambient Temperature | -40 | 85 | °C |
| Operating Junction Temperature | -40 | 125 | °C |
| Supply VCC Voltage | 8.0 | 26.5 | V |
| VCC Capacitor | 3.3 | 10 | μF |
| Start-up resistor Value (AC Side, Half Wave) | 400K | 2M | Ω |
| Comp Pin Capacitor | 1 | 10 | nF |
| CS Pin Capacitor Value | 47 | 390 | pF |

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, $V_{CC}$=15.0V)

| PARAMETER | CONDITIONS | SYM. | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply Voltage (Vcc Pin)** | | | | | | |
| Startup Current | VCC < UVLO (ON) | $I_{CC-ST}$ | --- | 0.6 | 1 | μA |
| Operating Current (with 1nF load on OUT pin) | $V_{COMP}$=3V | $I_{CC-OP1}$ | 1.7 | 1.85 | 2.1 | mA |
| | $V_{COMP}$=0V | $I_{CC-OP2}$ | 0.53 | 0.65 | 0.77 | mA |
| | OLP Tripped / Auto, OTP=3V | $I_{CC-OPA}$ | 0.48 | 0.52 | 0.64 | mA<br>mA |
| | OTP/OVP Tripped / Latch | $I_{CC-OPL1}$ | 0.70 | 0.83 | 0.98 | mA |
| Latch-Off Release Voltage | | $V_{cc-PDR}$ | 3.7 | 4.3 | 5.1 | V |
| Holding Current | $V_{CC}$=10V (Latched) | $I_{CC-OPL2}$ | 360 | 450 | 540 | μA |
| | $V_{CC}$=Latch-Off Release Voltage+0.2V | $I_{CC-OPL3}$ | 20 | 25 | 29 | μA |
| UVLO (off) | OUT OFF | $V_{CC-OFF}$ | 7.0 | 7.5 | 8.0 | V |
| UVLO (on) | | $V_{CC-ON}$ | 15 | 16 | 17 | V |
| VCC OVP Level | | $V_{CC-OVP}$ | 27.5 | 28.5 | 29.5 | V |
| VCC OVP De-bounce time | * | $T_{D-VCCOVP}$ | --- | 8 | --- | cycle |
| VCC OSCP | COMP > 4.6V | $V_{CC-OSCP}$ | --- | 9 | --- | V |
| VCC OSCP De-bounce Time | | $T_{D-OSCP}$ | --- | 15 | --- | ms |
| **Voltage Feedback (Comp Pin)** | | | | | | |
| Short Circuit Current | $V_{COMP}$=0V | $I_{COMP}$ | 0.10 | 0.125 | 0.15 | mA |
| Open Loop Voltage | COMP pin open | $V_{COMP-OPEN}$ | 4.75 | 5 | 5.25 | V |
| Green Mode Threshold VCOMP | * | $V_G$ | --- | 2.1 | --- | V |
| Zero Duty Threshold VCOMP | | $V_{ZDC}$ | 1.5 | 1.6 | 1.7 | V |
| Zero Duty Hysteresis | | $V_{ZDCH}$ | 70 | 100 | 130 | mV |
| **Current Sensing (CS/OVP pin)** | | | | | | |
| Maximum Input Voltage, $V_{CS\_OFF}$ | | $V_{CS-MAX}$ | 0.837 | 0.85 | 0.863 | V |
| Max. OCP Compensation Current, $I_{OCP}$ | | $I_{OCP}$ | 234 | 240 | 246 | μA |
| Leading Edge Blanking Time, LEB | | $T_{LEB}$ | 250 | 300 | 400 | ns |
| Internal Slope Compensation | *0% to $D_{MAX}$. (Linearly increase) | $V_{SLP-L}$ | --- | 300 | --- | mV |
| Input impedance | * | $Z_{CS}$ | 1 | --- | --- | MΩ |
| Delay to Output | * | $T_{PD}$ | --- | 100 | --- | ns |
| Soft Start Duration | * | $T_{SS}$ | --- | 6.5 | --- | ms |

| PARAMETER | CONDITIONS | SYM. | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Over Voltage Protection (CS/OVP pin)** | | | | | | |
| OVP Trip Current Level | | $V_{CSOVP}$ | 0.186 | 0.2 | 0.214 | V |
| De-bounce Cycle | * | $T_{D-CSOVP}$ | --- | 8 | --- | Cycle |
| **Oscillator for Switching Frequency** | | | | | | |
| Frequency, FREQ | | $F_{SW}$ | 63 | 65 | 67 | kHz |
| Green Mode Frequency, FREQG | | $F_{SW-GREEN}$ | 21.5 | 25 | 28 | kHz |
| Frequency Swapping | $V_{COMP}$>3V | $F_{SW-MOD}$ | --- | ± 5.0 | --- | kHz |
| Temp. Stability | (-20°C ~85°C)* | $F_{SW-TS}$ | 0 | 5 | --- | % |
| Voltage Stability | ($V_{CC}$=11V-25V)* | $F_{SW-VS}$ | 0 | 1 | --- | % |
| **Gate Drive Output (OUT Pin)** | | | | | | |
| Output Low Level | $V_{CC}$=15V, Io=20mA | $V_{OL}$ | --- | --- | 1 | V |
| Output High Level | $V_{CC}$=15V, Io=20mA | $V_{OH}$ | 8 | --- | 15 | V |
| Output High Clamp Level | $V_{CC}$=20V | $V_{O-CLAMP}$ | 13 | 15 | 17 | V |
| Rising Time | Load Capacitance=1000pF* | $T_r$ | --- | 150 | 250 | ns |
| Falling Time | Load Capacitance=1000pF* | $T_f$ | --- | 50 | 75 | ns |
| Max. Duty | | MXD | 71 | 75 | 79 | % |
| **OLP (Over Load Protection)** | | | | | | |
| OLP Trip Level | | $V_{OLP}$ | 4.3 | 4.5 | 4.7 | V |
| OLP Delay Time at start-up | OLP + Soft start* | $T_{D-OLPSS}$ | --- | 71.5 | --- | ms |
| OLP Delay Time after start-up | | $T_{D-OLP}$ | 60 | 65 | 70 | ms |
| **OTP Pin Latch Protection (OTP Pin)** | | | | | | |
| OTP Pin Source Current | | $I_{OTP}$ | 93 | 100 | 107 | μA |
| OTP Turn-On Trip Level | | $V_{OTP-ON}$ | 1.00 | 1.05 | 1.10 | V |
| OTP Turn-Off Trip Level | | $V_{OTP-OFF}$ | 0.9 | 0.95 | 1.0 | V |
| OTP Turn-Off Trip Resistance | =$V_{OTP-OFF}$/$I_{OTP}$* | $R_{OTP}$ | 8.75 | 9.5 | 10.25 | kΩ |
| OTP pin de-bounce time | $V_{COMP}$ > 3V | $T_{D-OTP}$ | 400 | 500 | 600 | μs |
| **Internal OTP Latch Protection** | | | | | | |
| OTP Tripped Level | * | $T_{INOTP}$ | --- | 140 | --- | ℃ |
| OTP Hysteresis | * | $T_{INOTP-HYS}$ | --- | 30 | --- | ℃ |

*: Guaranteed by design.

## Typical Performance Characteristics

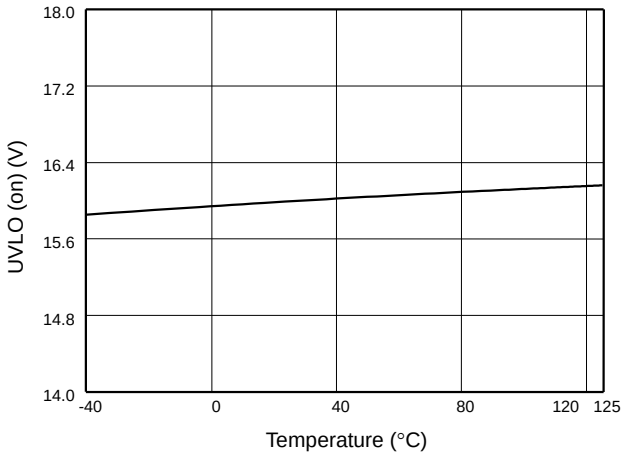



Fig. 1 UVLO (on) vs. Temperature

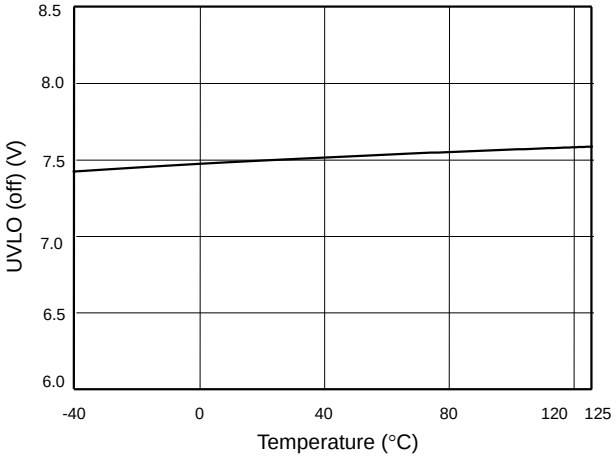



Fig. 2 UVLO (off ) vs. Temperature

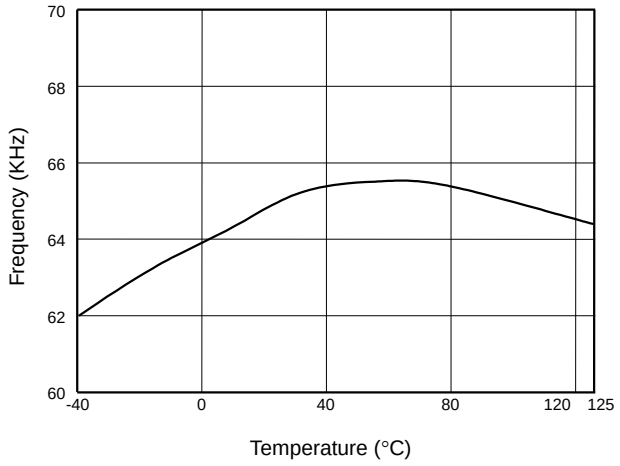



Fig. 3 Frequency vs. Temperature

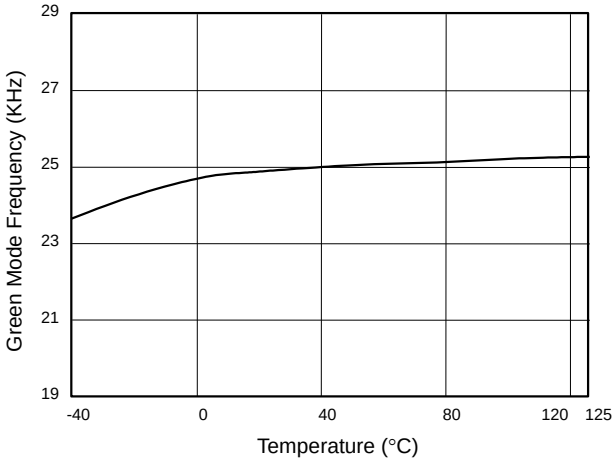



Fig. 4 Green Mode Frequency vs. Temperature

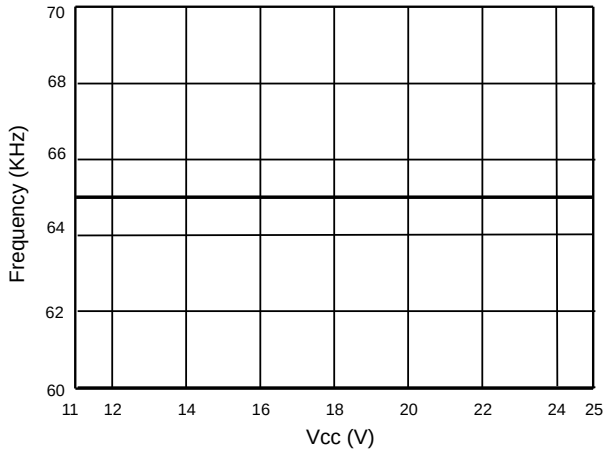



Fig. 5 Frequency vs. Vcc

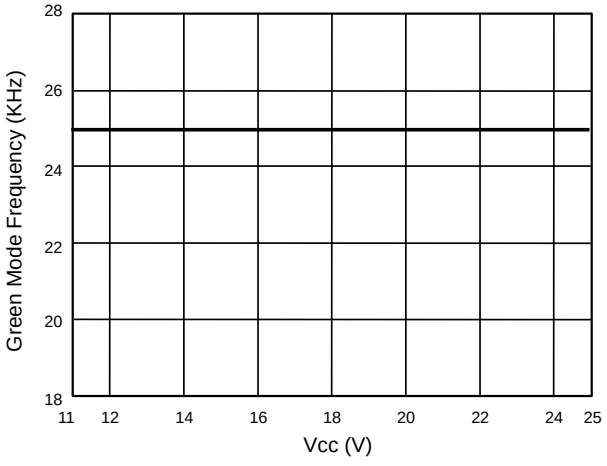



Fig. 6 Green Mode Frequency vs. Vcc

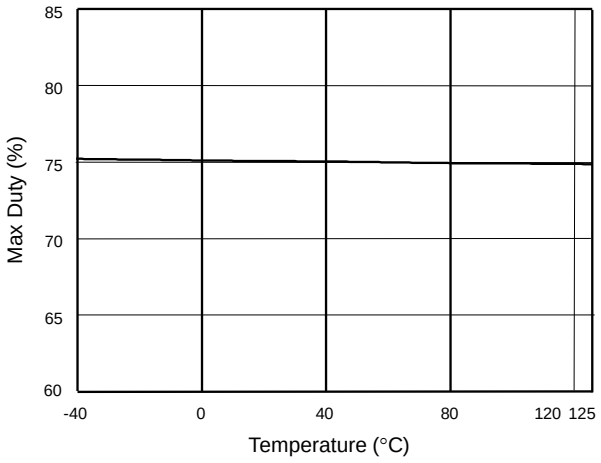



Fig. 7 Max Duty vs. Temperature

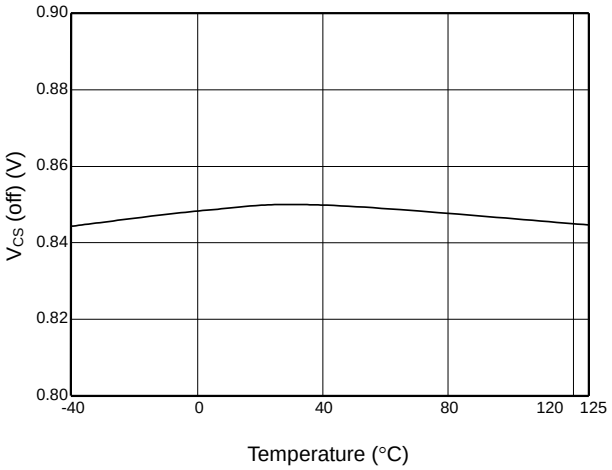



Fig. 8 $V_{CS}$ (off) vs. Temperature

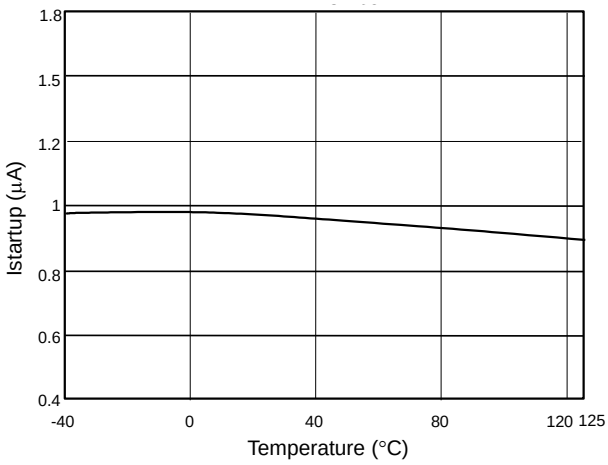



Fig. 9 Startup Current (Istartup) vs. Temperature

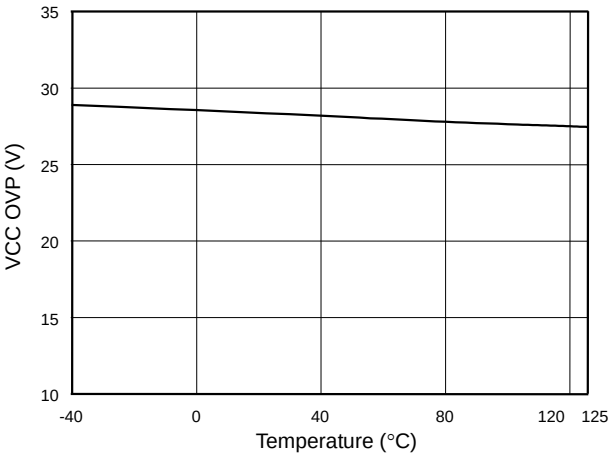



Fig. 10 VCC OVP vs. Temperature

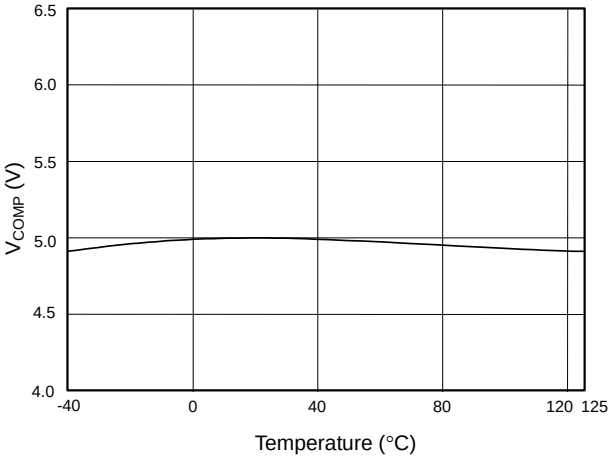



Fig. 11 $V_{COMP}$ open loop voltage vs. Temperature

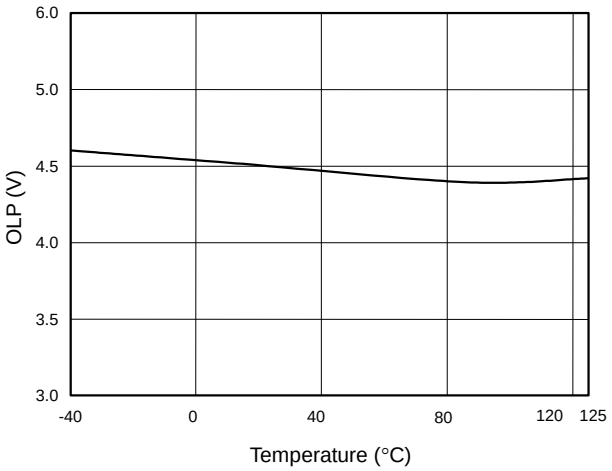



Fig. 12 OLP-Trip Level vs. Temperature

# Application Information

## Operation Overview

The LD5530 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

## Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD5530 PWM controller and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup.

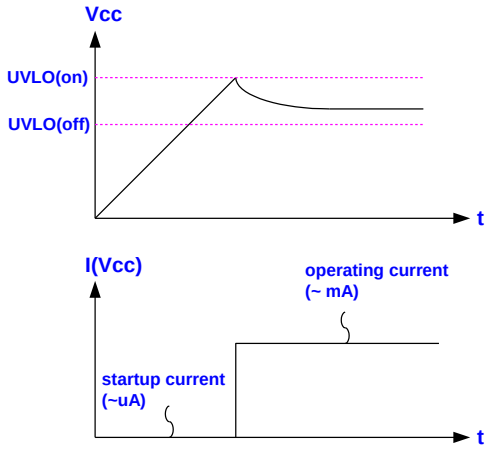



**Fig. 13**

## Startup Current and Startup Circuit

The typical startup circuit to generate $V_{CC}$ of the LD5530 is shown in Fig. 14. During the startup transient, the $V_{CC}$ is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. Once $V_{CC}$ obtain enough voltage to turn on the LD5530 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD5530 is only 1μA.

If a higher resistance value of the R1 is chosen, it will usually take more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

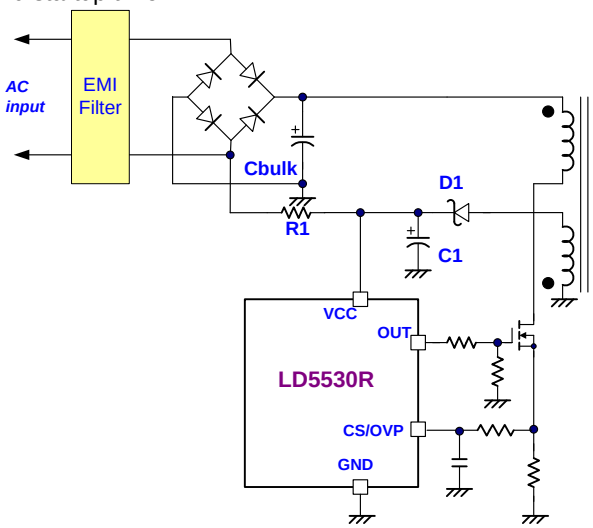



**Fig. 14**

## Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 15, the LD5530 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK\,(MAX)} = \frac{0.85V}{R_S}$$

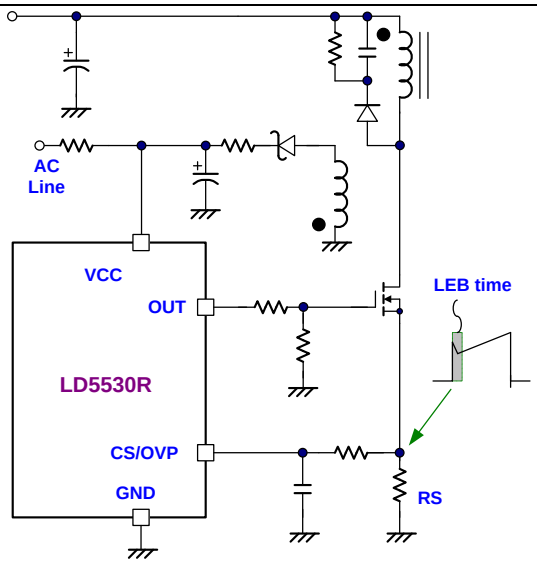



**Fig. 15**

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

## Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 250/-500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5530 is limited to 75% to avoid the transformer saturation.

## Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5530. Similar to UC3842, the LD5530 would carry a diode voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM\ COMPARATOR)} = \frac{R}{R+2R} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally and can be eliminated externally.

## Oscillator and Switching Frequency

The LD5530 is implemented with Frequency Swapping function which helps the power supply designers to both optimize EMI performance and lower system cost. The switching frequency substantially centers at 65KHz, and swap between a range of ±5KHz.

## Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property. Fig. 16 shows the characteristics of the switching frequency vs. the comp pin voltage ($V_{COMP}$)

## On/Off Control

The LD5530 can be turned off by pulling COMP pin lower than 1.6V. The gate output pin of the LD5530 will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

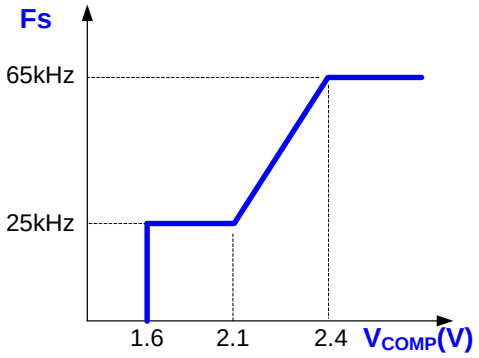



**Fig. 16**

## Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling, when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD5530 since it has integrated it already.

## Adjustable Over Current Compensation (CS/OVP Pin)

In general, the power converter can deliver more current at high input voltage than at low input voltage. To

compensate this, an offset voltage is added to the CS signal by an internal current source ($I_{OCP}$) and an external resistor ($R_{OCP}$) in series between the sense resistor (Rs) and the CS/OVP pin, as shown in Fig. 17. By selecting a proper value of the resistor in series with the CS pin, the amount of compensation can be adjusted. The value of $I_{OCP}$ depends on the duty cycle of OUT pin. The equation of $I_{OCP}$ is decreased as:

$$I_{OCP} = \begin{cases} (0.625 - Duty) \cdot 480uA & (0.125 < Duty < 0.625) \\ 0uA & (Duty \geq 0.625) \\ 240uA & (Duty \leq 0.125) \end{cases}$$

In light load conditions, the offset should be removed since it is in same order of magnitude as the current sense signal. Therefore the compensation current is only fully added when the COMP voltage is higher than 2.9V.

$R_{OCP}$:470Ω~1.2kΩ; $C_{OCP}$:47pF~390pF

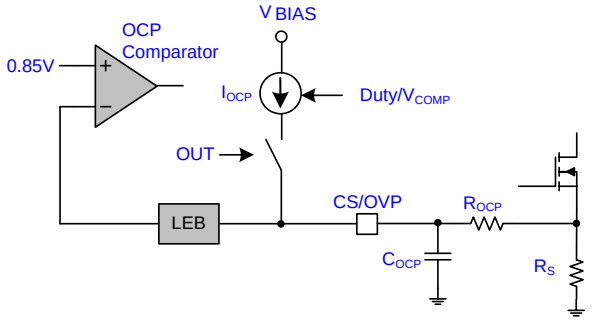



**Fig. 17**

## Output Over Voltage Protection (CS/OVP Pin) - Latch

An output overvoltage protection is implemented in the LD5530, as shown in Fig. 18 and 19. It senses the auxiliary voltage via the divided resistors. The auxiliary winding voltage is reflected from secondary winding and therefore the flat voltage on the CS/OVP pin is proportional to the output voltage. LD5530 can sample this flat voltage level after a delay time to perform output over voltage protection. This delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling voltage level is compared with internal threshold voltage 0.2V. If the sampling voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. However, when typically 8 cycles of subsequent OVP events are detected, the OVP circuit switches the power MOSFET off. As the protection is latch, the converter restarts after the AC is plug out and in.

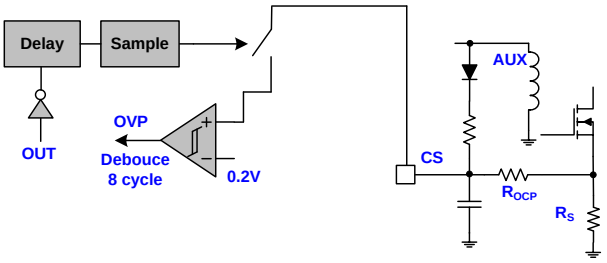



**Fig. 18**

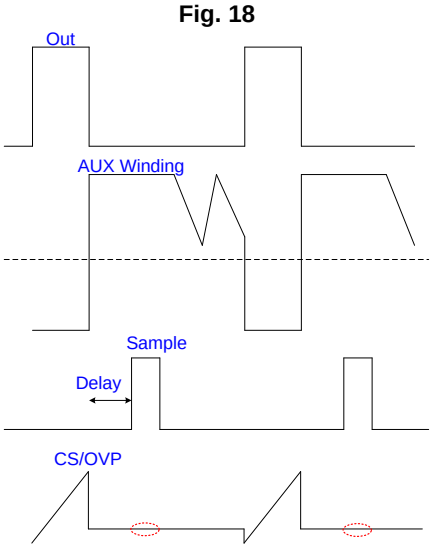



**Fig. 19**

## Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage in over-load condition and short or open-loop condition, the LD5530 is implemented with smart OLP function. It also features auto recovery function; see Fig. 20 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the $V_{COMP}$

ramps up to the OLP threshold of 4.5V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

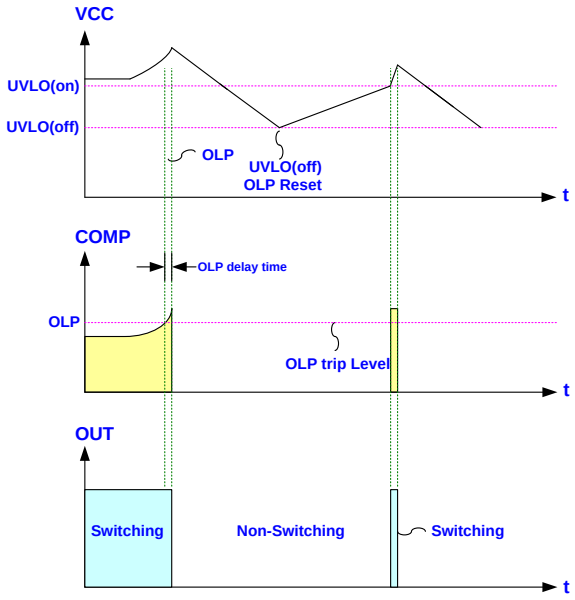



**Fig. 20**

## Over Voltage Protection (OVP) on Vcc - Latch

The Vcc OVP function of LD5530 is in latch mode. As soon as the voltage of the Vcc pin rises above OVP threshold, the output gate drive circuit will be shutdown simultaneous to turn off the power MOSFET. Fig. 21 shows its operation.

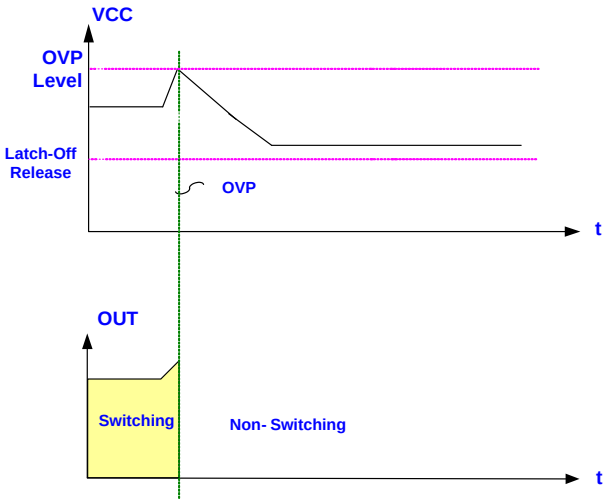



**Fig. 21**

## OTP Pin --- Latched Mode Protection

The OTP circuit is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Once an over-temperature condition is detected, the OTP is enabled to shut down the controller to protect the controller. Typically, a NTC is recommended to connect with OTP pin. The NTC resistance will decrease as the device or ambient in high temperature. The relationship is as below.

$$V_{OTP} = 100\mu A \cdot R_{NTC}$$

When the $V_{OTP}$ is below the defined voltage threshold (typ. 0.95V), LD5530 will shutdown the gate output and latch off the power supply. There are 2 conditions required to restart it successfully. First, cool down the circuit so that NTC resistance will increase and raise $V_{OTP}$ up above 1.05V. Then, remove the AC power cord and re-plug AC power.

## MOSFET Characteristic

The MOSFET is divided into three operation regions, ohmic region, saturation region, and the cut-off region, shown as Fig. 22.

For switching power supply applications, it shall operate in ohmic and cut-off region. Never reach the region of

saturation; it would cause damage for acting beyond the maximum safety operating area. It's necessary to check the characteristic of MOSFET.

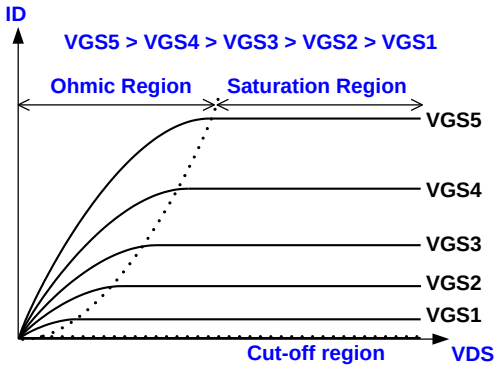


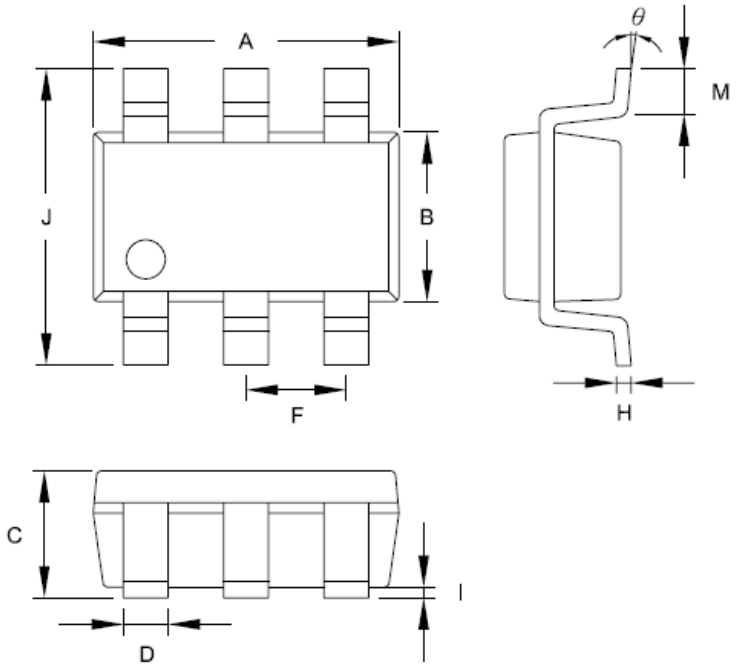

**Fig. 22**

## Output Short Circuit Protection (OSCP) – Auto Recovery

The OSCP function is to prevent the damage from output short circuit. Once the output is shorted, Vo and $V_{CC}$ drop immediately. And according to the close loop control, COMP voltage will pull high in the meanwhile. If the VCOMP pulls high to over 4.5 V for over 15 ms and Vcc drops below 9 V. At this time, the OSCP protection will be triggered and turn off the gate driving.

## Package Information

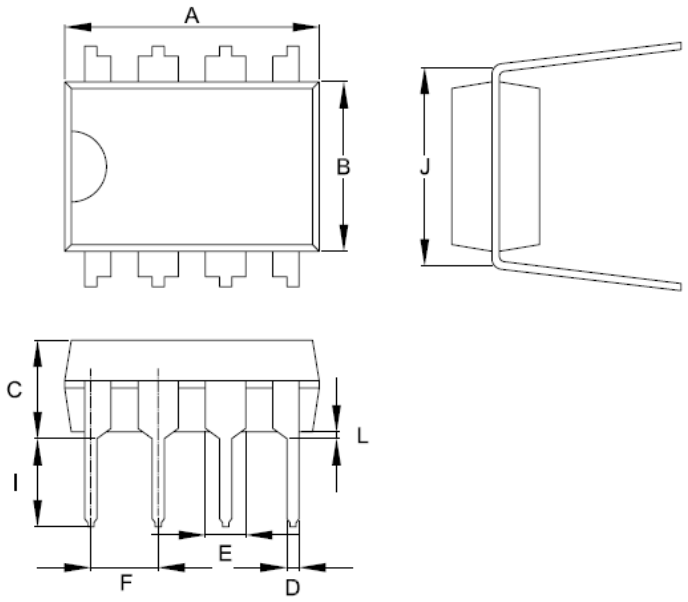
**SOT-26**




| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 2.692 | 3.099 | 0.106 | 0.122 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| C | ------- | 1.450 | ------- | 0.057 |
| D | 0.300 | 0.500 | 0.012 | 0.020 |
| F | 0.95 TYP | | 0.037 TYP | |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| I | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 2.600 | 3.000 | 0.102 | 0.118 |
| M | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 10° | 0° | 10° |

## Package Information

**DIP-8**




| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 9.017 | 10.160 | 0.355 | 0.400 |
| B | 6.096 | 7.112 | 0.240 | 0.280 |
| C | ----- | 5.334 | ------ | 0.210 |
| D | 0.356 | 0.584 | 0.014 | 0.023 |
| E | 1.143 | 1.778 | 0.045 | 0.070 |
| F | 2.337 | 2.743 | 0.092 | 0.108 |
| I | 2.921 | 3.556 | 0.115 | 0.140 |
| J | 7.366 | 8.255 | 0.29 | 0.325 |
| L | 0.381 | ------ | 0.015 | -------- |

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

## Revision History

| Rev. | Date | Change Notice |
|---|---|---|
| 00 | 10/8/2013 | Original Specification. |