

DATA SHEET

TDA1521

TDA1521Q

2 x 12 W hi-fi audio power amplifier

Product specification
File under Integrated Circuits, IC01

July 1994

2 x 12 W hi-fi audio power amplifier**TDA1521
TDA1521Q****GENERAL DESCRIPTION**

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off
(no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA**Stereo applications**

| | | | |
|---|---------------|-------------------------|---------|
| Supply voltage range | V_P | $\pm 7,5$ to $\pm 21,0$ | V |
| Output power at THD = 0,5%, $V_P = \pm 16$ V | P_O | typ. 12 | W |
| Voltage gain | G_v | typ. 30 | dB |
| Gain balance between channels | ΔG_v | typ. 0,2 | dB |
| Ripple rejection | SVRR | typ. 60 | dB |
| Channel separation | α | typ. 70 | dB |
| Noise output voltage | $V_{no(rms)}$ | typ. 70 | μ V |

PACKAGE OUTLINES

TDA1521: 9 leads in-line; plastic power (SOT131); SOT131-1; 1996 August 20.

TDA1521Q: 9 leads SIL-bent-to-DIL; plastic power (SOT157); SOT157-2; 1996 August 20.

2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q

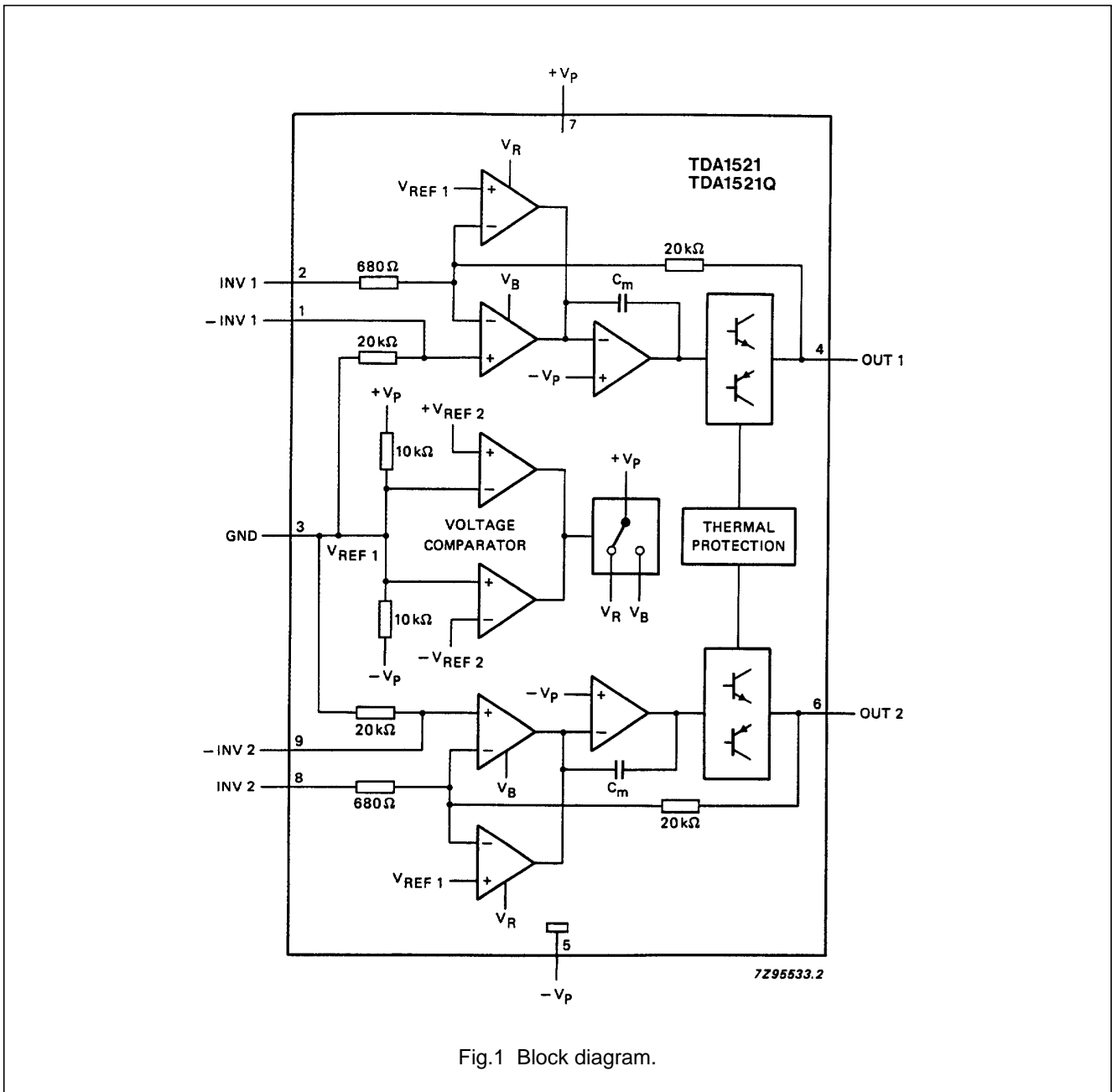


Fig.1 Block diagram.

PINNING

| | | |
|---|-------|---|
| 1 | -INV1 | non-inverting input 1 |
| 2 | INV1 | inverting input 1 |
| 3 | GND | ground (symmetrical) 1/2 V _P (asymmetrical) |
| 4 | OUT1 | output 1 |

| | | |
|---|-----------------|--|
| 5 | -V _P | negative supply (symmetrical) ground (asymmetrical) |
| 6 | OUT2 | output 2 |
| 7 | +V _P | positive supply |
| 8 | INV2 | inverting input 2 |
| 9 | -INV2 | non-inverting input 2 |

2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q**FUNCTIONAL DESCRIPTION**

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2×12 watts (THD = 0,5%) can be delivered into an 8Ω load with a symmetrical power supply of ± 16 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig.13, the $100 \mu\text{F}$ capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150°C allowing safe operation to a maximum junction temperature of 150°C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| PARAMETER | CONDITIONS | SYMBOL | MIN. | MAX. | UNIT |
|--|---|------------------|------|------|------------------|
| Supply voltage | pin 7 | $V_P = V_{7-3}$ | – | +21 | V |
| | pin 5 | $-V_P = V_{5-3}$ | – | –21 | V |
| Non-repetitive peak output current | pins 4 and 6 | I_{OSM} | – | 4 | A |
| Total power dissipation | see Fig.2 | P_{tot} | | | |
| Storage temperature range | | T_{stg} | –55 | +150 | $^\circ\text{C}$ |
| Junction temperature | | T_j | – | 150 | $^\circ\text{C}$ |
| Short-circuit time: outputs short-circuited to ground (full signal drive) | see note symmetrical power supply asymmetrical power supply; $V_P < 32$ V (unloaded); $R_i \geq 4 \Omega$ | t_{sc} | – | 1 | hour |
| | | t_{sc} | – | 1 | hour |

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to $V_P = 28$ V. If the total internal resistance of the supply (R_i) $> 4 \Omega$, the maximum unloaded supply voltage is increased to 32 V.

2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q

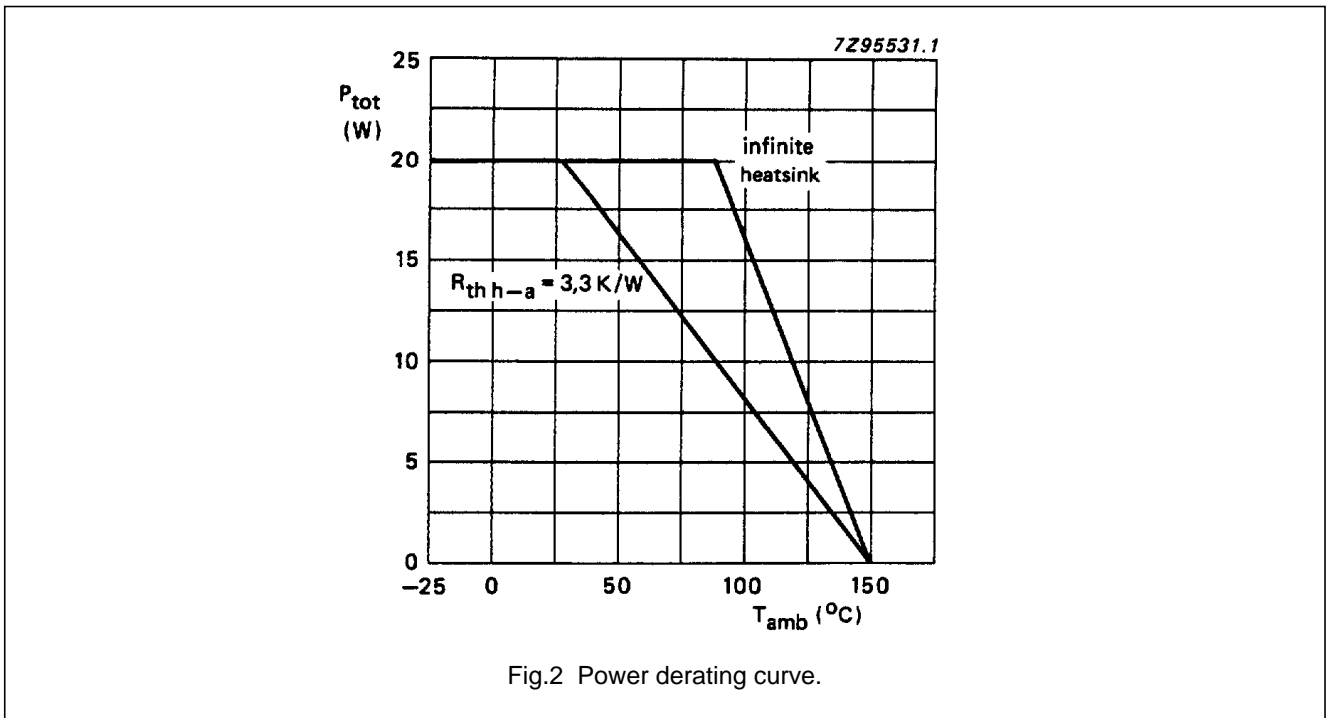


Fig.2 Power derating curve.

THERMAL RESISTANCE

From junction to case

$$R_{th\ j-c} = 2,5 \text{ K/W}$$

HEATSINK DESIGN EXAMPLE

With derating of 2,5 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8 \Omega$ and $V_p = \pm 16$ V, the measured maximum dissipation is 14,6 W; then, for a maximum ambient temperature of 65 °C, the required thermal resistance of the heatsink is

$$R_{th\ h-a} = \frac{150 - 65}{14,6} - 2,5 = 3,3 \text{ K/W}$$

Note: The internal metal block (heatsink) has the same potential as pin 5 ($-V_p$).

2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q

CHARACTERISTICS

| PARAMETER | CONDITIONS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---------------------------|---------------|-----------|--------------|------------|------------|
| Supply voltage range | | | | | | |
| operating mode | | V_P | $\pm 7,5$ | $\pm 16,0$ | $\pm 21,0$ | V |
| input mute mode | | V_P | $\pm 2,0$ | – | $\pm 5,8$ | V |
| Repetitive peak | | | | | | |
| output current | | I_{ORM} | 2,2 | – | – | A |
| Operating mode: symmetrical power supply; test circuit as per Fig.12; $V_P = \pm 16$ V; $R_L = 8$ Ω ; $T_{amb} = 25$ °C; $f = 1$ kHz | | | | | | |
| Total quiescent current | without R_L | I_{tot} | 18 | 40 | 70 | mA |
| Output power | THD = 0,5% | P_O | 10 | 12 | – | W |
| | THD = 10% | P_O | 12 | 15 | – | W |
| Total harmonic distortion | $P_O = 6$ W | THD | – | 0,15 | 0,2 | % |
| Power bandwidth | THD = 0,5% note 1 | B | | 20 to 20k | | Hz |
| Voltage gain | | G_V | 29 | 30 | 31 | dB |
| Gain balance | | ΔG_V | – | 0,2 | 1,0 | dB |
| Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz) | $R_S = 2$ k Ω | $V_{no(rms)}$ | – | 70 | 140 | μ V |
| Input impedance | | $ Z_i $ | 14 | 20 | 26 | k Ω |
| Ripple rejection | note 2 | SVRR | 40 | 60 | – | dB |
| Channel separation | $R_S = 0$ Ω | α | 46 | 70 | – | dB |
| Input bias current | | I_{ib} | – | 0,3 | – | μ A |
| DC output offset voltage | with respect to ground | V_{OFF} | – | 30 | 200 | mV |
| Input mute mode: symmetrical power supply; test circuit as per Fig.12; $V_P = \pm 4$ V; $R_L = 8$ Ω ; $T_{amb} = 25$ °C; $f = 1$ kHz | | | | | | |
| Total quiescent current | without R_L | I_{tot} | 9 | 30 | 40 | mA |
| Output voltage | $V_i = 600$ mV | V_{out} | – | 0,6 | 1,8 | mV |
| Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz) | $R_S = 2$ k Ω | $V_{no(rms)}$ | – | 70 | 140 | μ V |
| Ripple rejection | note 2 | SVRR | 35 | 55 | – | dB |
| DC output offset voltage | with respect to ground | V_{OFF} | – | 40 | 200 | mV |

2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q

| PARAMETER | CONDITIONS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|--------------------------|----------------------|------|-------|------|------------------|
| Operating mode: asymmetrical power supply; test circuit as per Fig.13; $V_S = 24\text{ V}$; $R_L = 8\ \Omega$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$; $f = 1\text{ kHz}$ | | | | | | |
| Total quiescent current | | I_{tot} | 18 | 40 | 70 | mA |
| Output power | THD = 0,5% | P_o | 5 | 6 | – | W |
| | THD = 10% | P_o | 6,5 | 8 | – | W |
| Total harmonic distortion | $P_o = 4\text{ W}$ | THD | – | 0,13 | 0,2 | % |
| Power bandwidth | THD = 0,5% | | | 40 to | | |
| | note 1 | B | | 20k | | Hz |
| Voltage gain | | G_V | 29 | 30 | 31 | dB |
| Gain balance | | ΔG_V | – | 0,2 | 1 | dB |
| Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz) | $R_S = 2\text{ k}\Omega$ | $V_{\text{no(rms)}}$ | – | 70 | 140 | μV |
| Input impedance | | $ Z_i $ | 14 | 20 | 26 | $\text{k}\Omega$ |
| Ripple rejection | | SVRR | 35 | 44 | – | dB |
| Channel separation | $R_S = 0\ \Omega$ | α | – | 45 | – | dB |

Notes

1. Power bandwidth at P_o max –3 dB.
2. Ripple rejection at $R_S = 0\ \Omega$, $f = 100\text{ Hz}$ to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

2 x 12 W hi-fi audio power amplifier

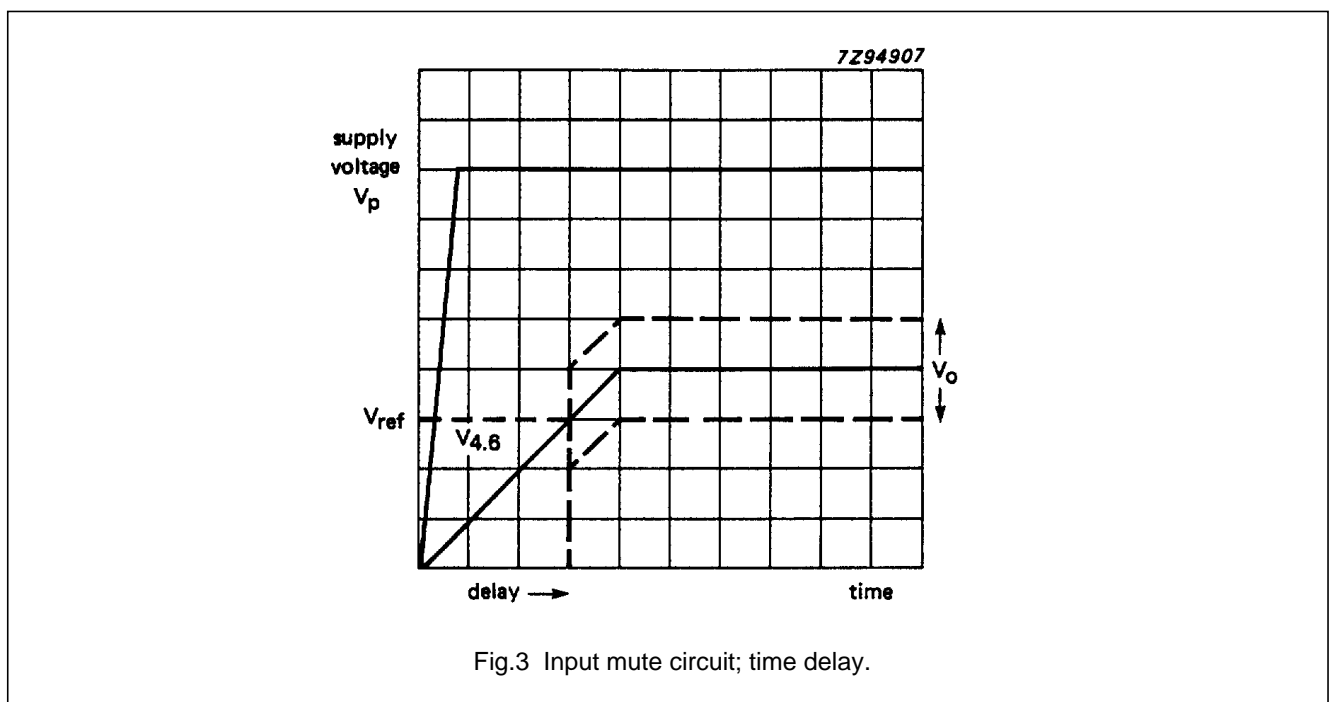
TDA1521
TDA1521Q

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the 1/2 supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μ F capacitor.

During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig.3).



2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q

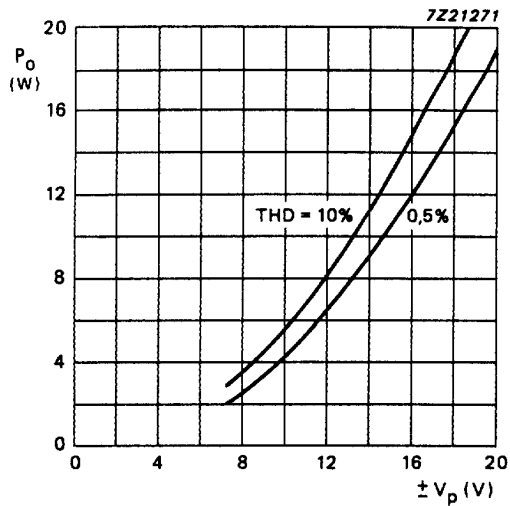


Fig.4 Output power as a function of supply voltage; symmetrical supply; $R_L = 8 \Omega$; $f = 1 \text{ kHz}$.

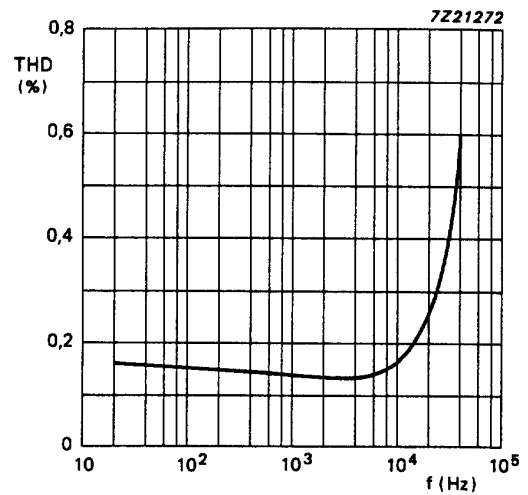


Fig.5 Distortion as a function of frequency; symmetrical supply; $V_P = \pm 16 \text{ V}$; $R_L = 8 \Omega$; $P_o = 6 \text{ W}$.

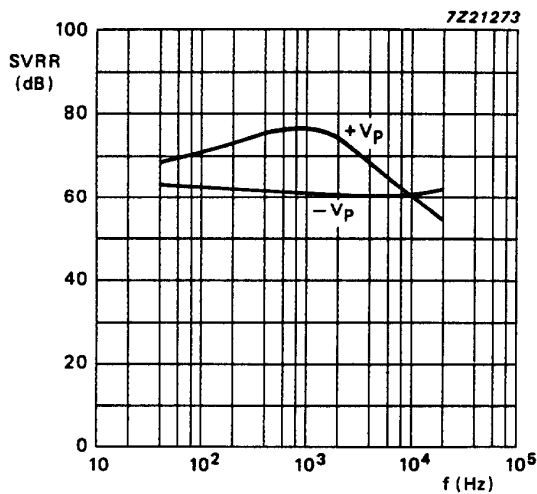


Fig.6 Supply voltage ripple rejection; symmetrical supply; $V_P = \pm 16 \text{ V}$; $V_{RR} = 200 \text{ mV}$.

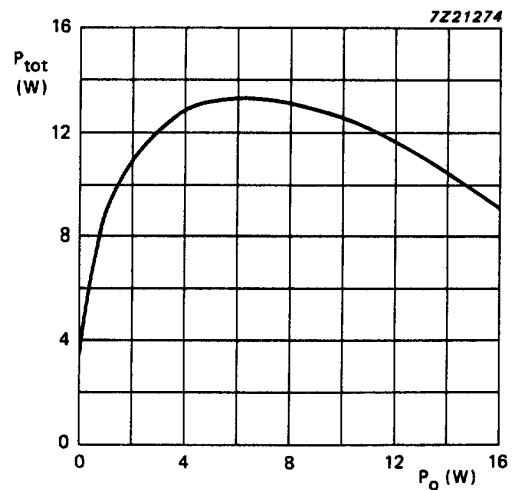


Fig.7 Power dissipation as a function of output power; symmetrical supply; $V_P = \pm 16 \text{ V}$; $R_L = 8 \Omega$; $f = 1 \text{ kHz}$.

2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q

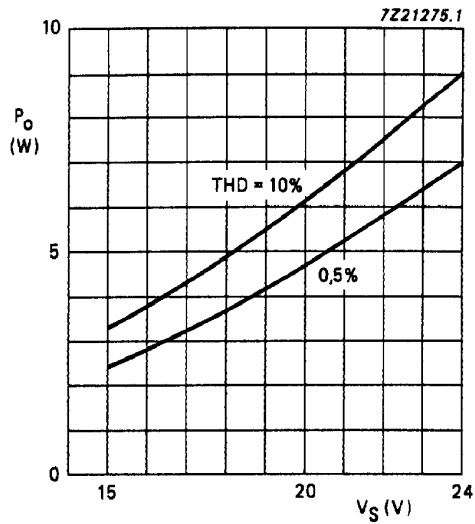


Fig.8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8 \Omega$; $f = 1$ kHz.

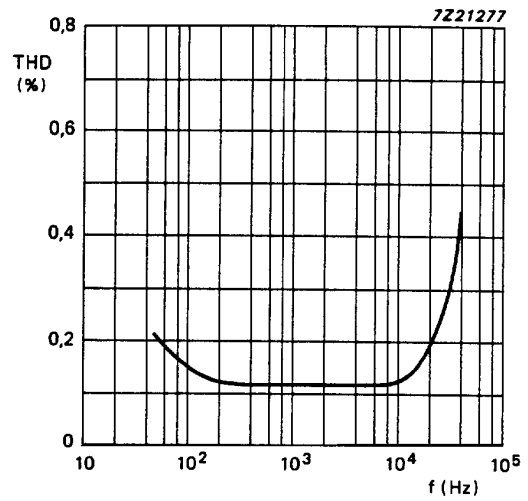


Fig.9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8 \Omega$; $P_o = 4$ W.

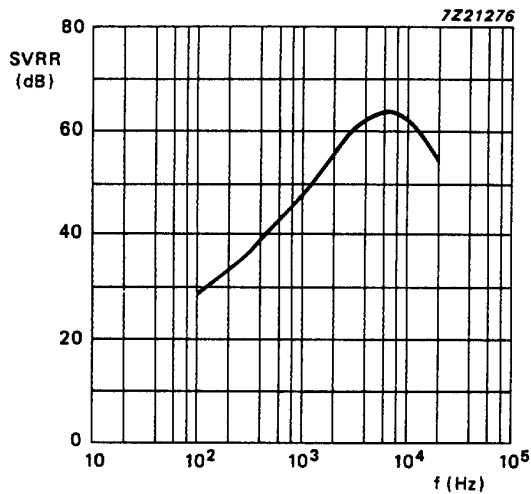


Fig.10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mV.

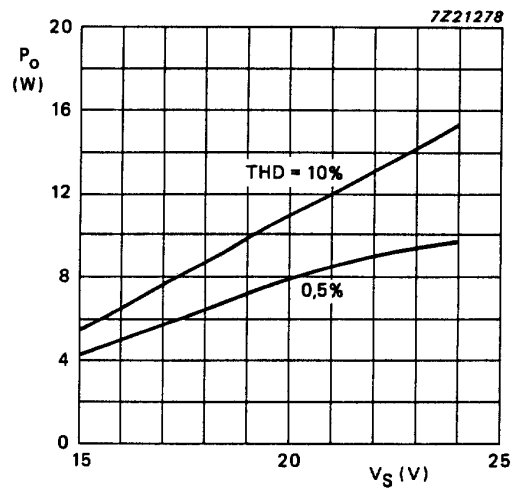
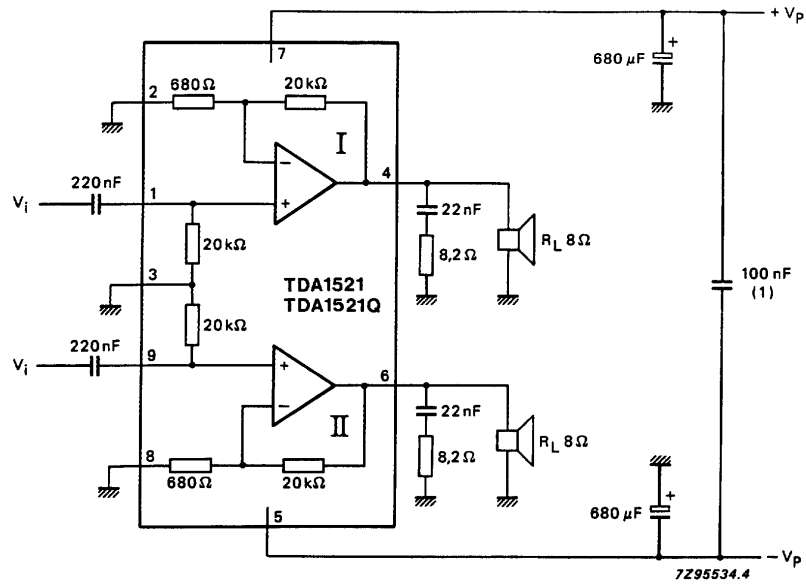


Fig.11 Output power as a function of supply voltage; asymmetrical supply; $R_L = 4 \Omega$; $f = 1$ kHz.

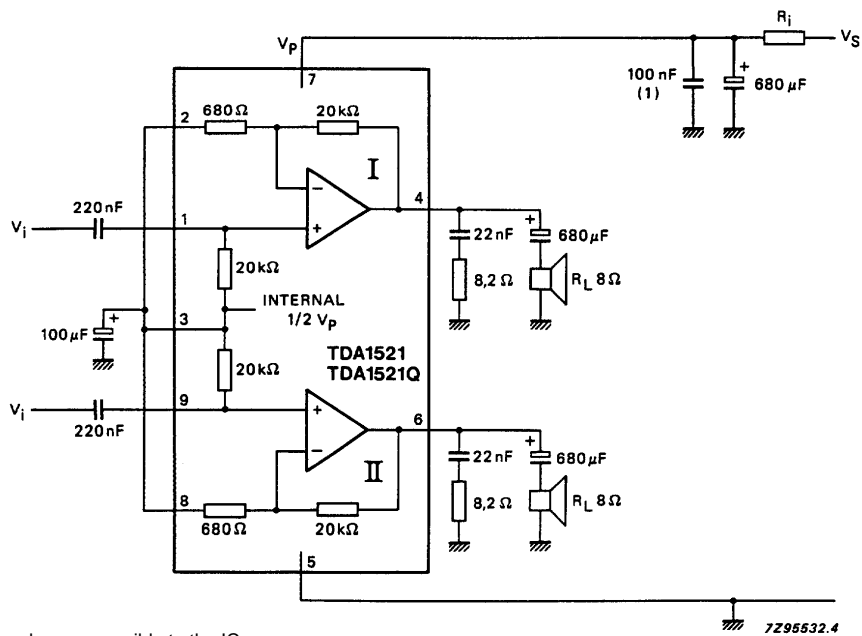
2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q



(1) To be connected as close as possible to the IC

Fig.12 Test and application circuit; symmetrical power supply.



(1) To be connected as close as possible to the IC

Fig.13 Test and application circuit; asymmetrical power supply.

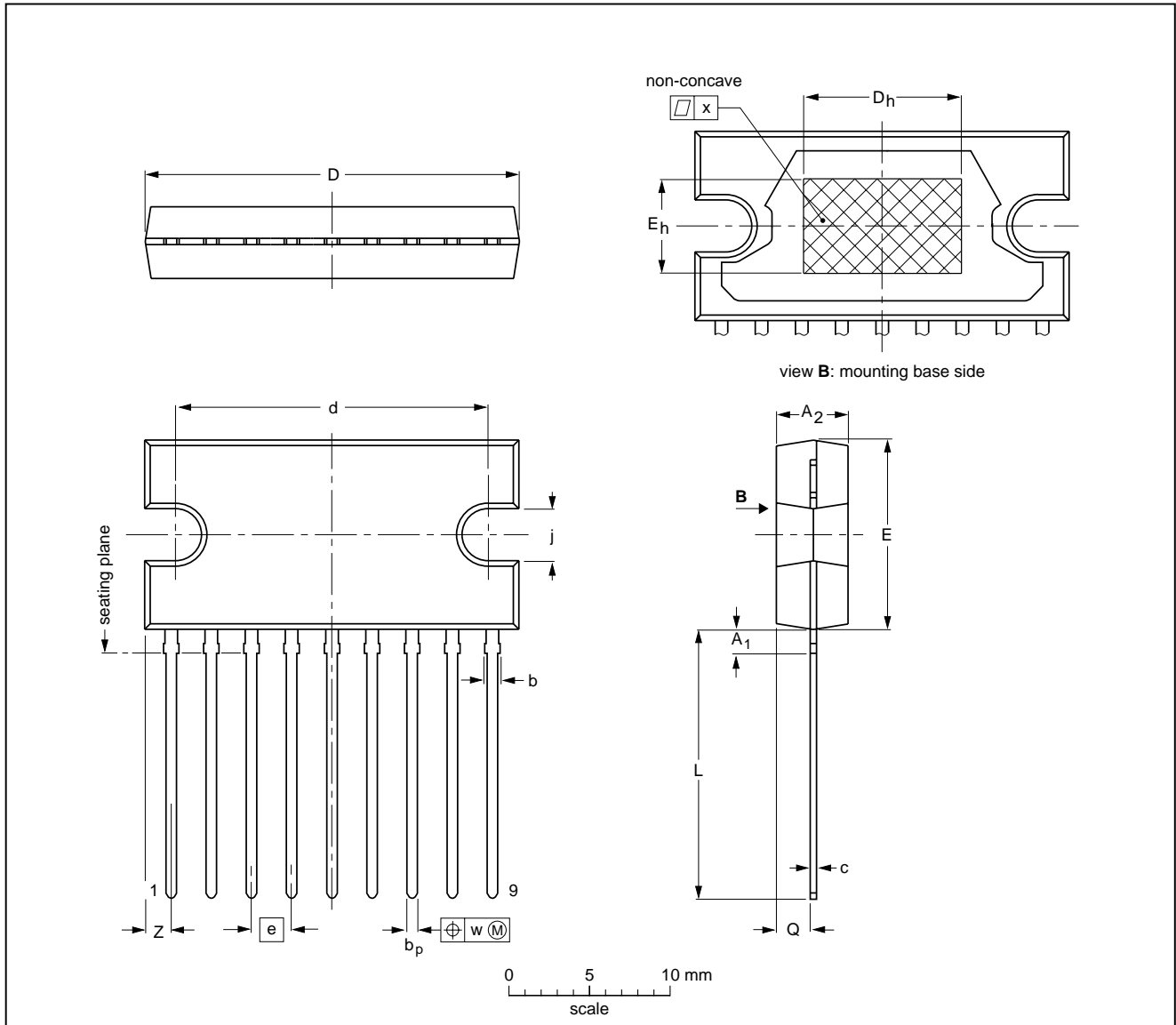
2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q

PACKAGE OUTLINES

SIL9P: plastic single in-line power package; 9 leads

SOT131-2



DIMENSIONS (mm are the original dimensions)

| UNIT | A ₁ max. | A ₂ | b max. | b _p | c | D ⁽¹⁾ | d | D _h | E ⁽¹⁾ | e | E _h | j | L | Q | w | x | Z ⁽¹⁾ |
|------|------------------------|----------------|-----------|----------------|--------------|------------------|--------------|----------------|------------------|------|----------------|------------|--------------|------------|------|------|------------------|
| mm | 2.0 | 4.6 4.2 | 1.1 | 0.75 0.60 | 0.48 0.38 | 24.0 23.6 | 20.0 19.6 | 10 | 12.2 11.8 | 2.54 | 6 | 3.4 3.1 | 17.2 16.5 | 2.1 1.8 | 0.25 | 0.03 | 2.00 1.45 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

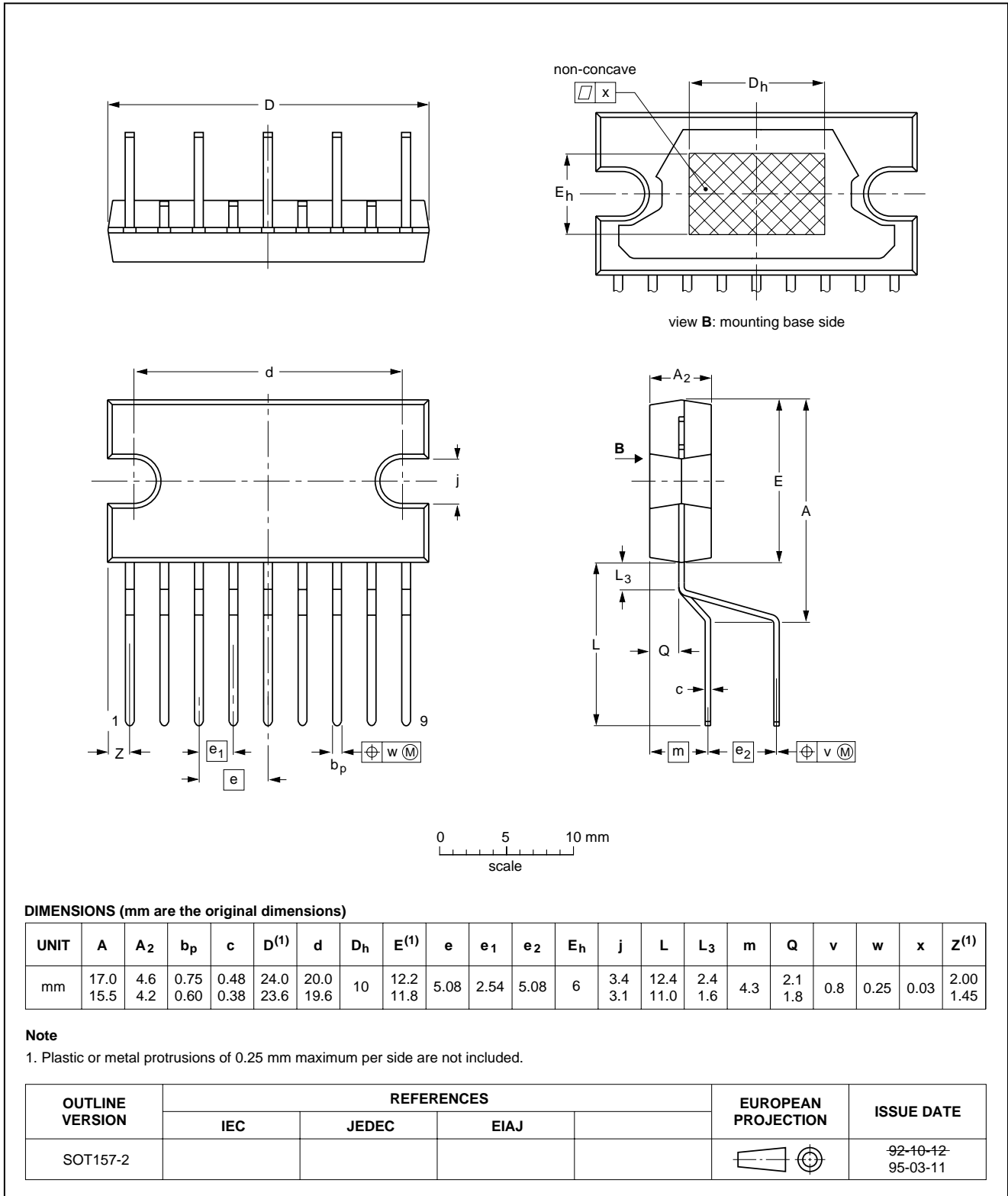
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|------|--|------------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT131-2 | | | | | | 92-11-17 95-03-11 |

2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12 mm)

SOT157-2



2 x 12 W hi-fi audio power amplifier

TDA1521
TDA1521Q**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

LIFE SUPPORT APPLICATIONS

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