Qualcomm Technologies, Inc.

PM8994/PM8996 Power Management IC

Device Specification

LM80-P2751-5 Rev. C

February 15, 2018

For additional information or to submit technical questions, go to
https://www.96boards.org/product/dragonboard820c

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Revision history

Revision	Date	Description
A	November 2015	Initial release
B	May 2016	Updated to match the source document
C	February 2018	Updated the document as per the new branding guidelines

Contents

Tables

Figures

1 Introduction

1.1 Documentation overview

This document contains a description of the chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE: Enabling some features may require additional licensing fees.

Technical information for the PM8994/PM8996 Power Management IC device is primarily covered by the documents listed in Table 1-1. These documents should be studied for a thorough understanding of the IC and its applications. The Released PM8994/PM8996 Power Management IC documents are posted here: https://discuss.96boards.org/c/products/dragonboard820c and are available for download.

Table 1-1 Primary PM8994/PM8996 device documentation

Document number	Title/description
LM80-P02751-5 (this document)	*PM8994/PM8996 Power Management IC Device Specification* Provides all PM8994/PM8996 electrical and mechanical specifications. Additional material includes pad assignment definitions, shipping, storage, and handling instructions, PCB mounting guidelines, and part reliability. This document can be used by company purchasing departments to facilitate procurement.
LM80-P02751-10	*PM8994/PM8996 Power Management IC Device Revision Guide* Provides a history of PM8994/PM8996 device revisions. This document explains how to identify the various IC revisions and discusses known issues (or bugs) for each revision and how to work around them.

1.2 Document updates

See the Revision history for details on the changes included in this revision.

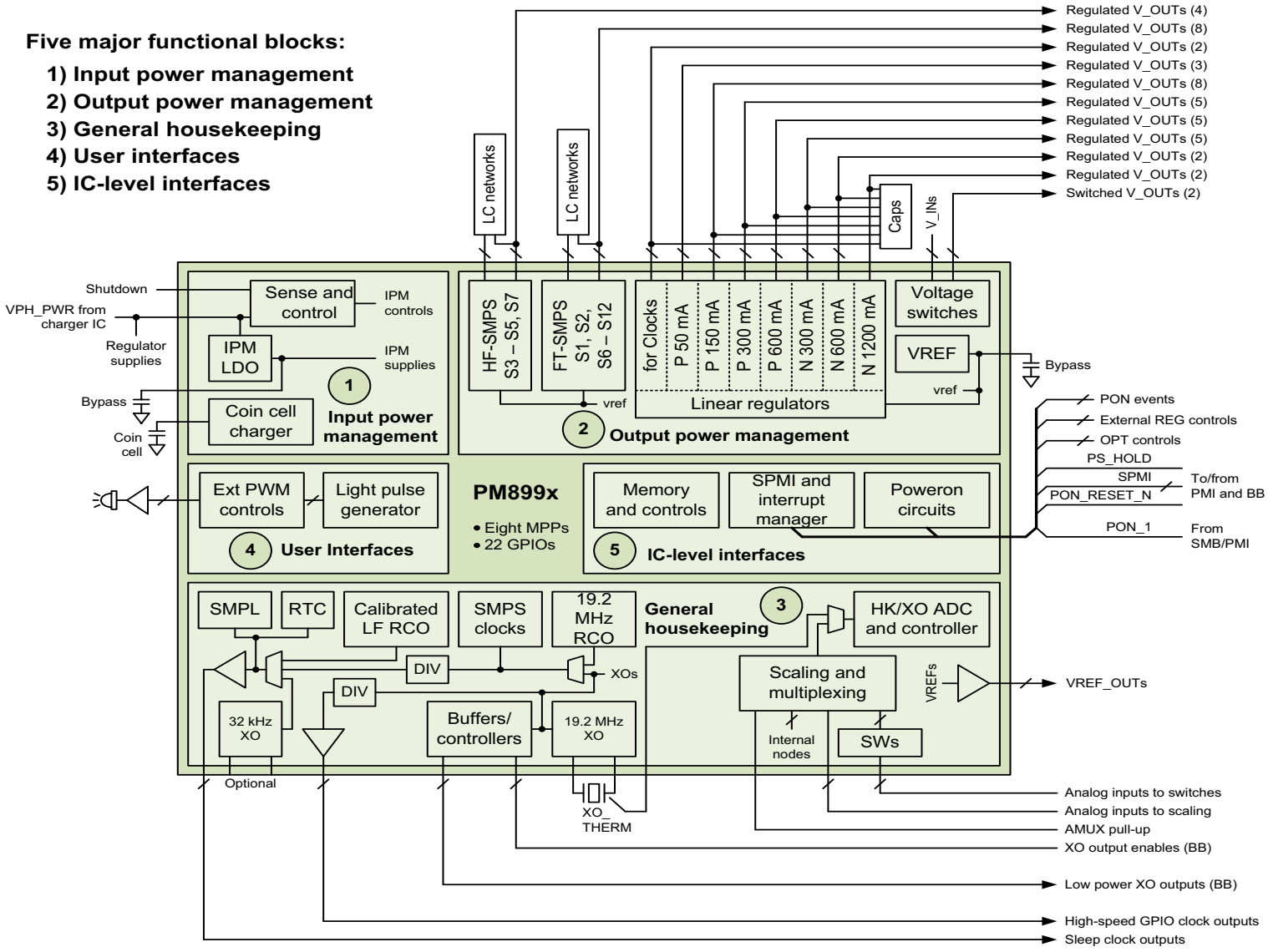


Figure 1-2 High-level PM8994/PM8996 functional block diagram

1.3 PM8994/PM8996 features

NOTE: Some hardware features integrated within the PM8994/PM8996 device must be enabled through the IC software. See the latest version of the applicable software release notes to identify the enabled PMIC features.

1.3.1 Summary of PM8994/PM8996 features

Table 1-1 lists the PM8994/PM8996 device features and Table 1-2 lists the IEC pads.

Table 1-1 PM8994/PM8996 features

Feature	PM8994/PM8996 capability
Input power management	
Coin cell or capacitor backup	Keep-alive power source; orchestrated charging
Output voltage regulation	
Switched-mode power supplies HF-SMPS FT-SMPS	 Four - two at 2.0 A, two at 3.5 A Eight at 4.0 A each
Low-dropout linear regulators	32 total: NMOS at 1.2 A (two), 600 mA (two), 300 mA (five); PMOS at 600 mA (five), 300 mA (five), 150 mA (eight), 50 mA (three), and two for clocks
Pseudo-capless LDO designs	24 of 32 LDOs
Voltage switches	Suitable for power gating external circuitry: two at 1.8 V
General housekeeping	
On-chip ADC	Shared housekeeping (HK) and XO support
Analog multiplexing for ADC HK inputs XO input	 Many internal nodes and external inputs, including configurable MPPs Dedicated pad (XO_THERM)
Over-temperature protection	Multistage smart thermal control
19.2 MHz oscillator support	XO (with on-chip ADC)
XO controller and XO outputs	Five sets: two low-noise outputs (RF), and two low-power outputs (BB), one low-noise BB output
Differential XO clock output	One
Special purpose clock outputs	Sleep clock; 19.2, 9.6, 4.8, 2.4, and 1.2 MHz, including low-power mode 2.4 MHz for MP3; four high-speed GPIOs for fast clocks
Real time clock	RTC clock circuits and alarms
User interfaces	
Current drivers	Even number MPPs can be configured for current sinks, up to 40 mA in 5 mA steps Odd number MPPs can be configured for output voltage buffers
Light pulse generators	Six channels

Table 1-1 PM8994/PM8996 features (cont.)

Feature	PM8994/PM8996 capability
Controls for external current drivers	Up to six PWM outputs via GPIOs
IC-level interfaces	
Primary status and control	Two-line SPMI
Interrupt managers	Supported by SPMI
Optional hardware configurations	OPT bits select hardware configuration
Power sequencing	Poweron, power-off, and soft resets
Configurable I/Os	
MPPs	Eight; configurable as digital inputs or outputs, level-translating bidirectional I/Os, analog multiplexer inputs, or VREF analog outputs Even number MPPs can be configured for current sinks, up to 40 mA in 5 mA steps Odd number MPPs can be configured for output voltage buffers
GPIO pads	22; configurable as digital inputs or outputs or level-translating I/Os; all are much faster than MPPs; four special high-speed GPIOs for clock outputs
Packages	
PM8994/PM8996	225-pad WLNSP; 6.21 × 6.16 × 0.55 mm

Table 1-2 IEC pads

IEC 61000-4-2 for device pad name	Test method and evaluation of results
AMUX_1	Level 4: ± 8 kV contact
RESIN_N	Evaluation of results: No physical damage; loss of function or degradation of performance which is not recoverable, owing damage to hardware. Until IEC test results are available at CS and system-level testing is done by customers, Qualcomm Technologies, Inc. (QTI) recommends the external IEC-ESD component. KPD_PWR_N is not considered an IEC pad anymore. Therefore, QTI recommends that an external IEC-ESD component be used on KPD_PWR_N for ESD protection.

1.4 Acronyms, abbreviations, and terms

Table 1-3 defines terms and acronyms used throughout this document.

Table 1-3 Terms and acronyms

Term or acronym	Definition
ADC	Analog-to-digital converter
AFR	Average failure rate
AMC	Autonomous mode control
AMUX	Analog multiplexer
API	Application programming interface
APC	Autonomous phase control
AR	Area ratio
ATC	Auto-trickle charger
BB	Baseband
BB_CLK	Baseband clock
CDM	Charged device model
CMC	Current mode control
CSI	Camera serial interface
DPPM	Defective parts per million
DSI	Display serial interface
EBI	External bus interface
EEPROM	Electrically erasable programmable read-only memory
ELFR	Early life failure rate
eMMC	Embedded multimedia card
ESR	Effective series resistance
FES	Front-end server
FT-SMPS	Fast transient SMPS
GND	Ground
GPIO	General-purpose input/output
GSM	Global system for mobile communications
HBM	Human body model
HF-SMPS	High frequency SMPS
HK	Housekeeping
HKADC	Housekeeping analog-to-digital converter
ID	Identification
LDO	Low dropout (linear regulator)
Li	Lithium
LPDDR	Low-power DDR

Table 1-3 Terms and acronyms (cont.)

Term or acronym	Definition
LPG	Light pulse generator
LPM	Low-power mode
LVS	Low voltage switches
MHL	Mobile high-definition link
MIPI	Mobile industry processor interface
MMC	Multimedia card
MPP	Multipurpose pad
MRT	Moisture resistance test
MSL	Moisture sensitivity level
MTTF	Mean time to failure
Mux	Multiplexer
NMOS	N-channel metal-oxide semiconductor
NPM	New power management
NSP	Nanoscale package
NSMD	Non-solder-mask-defined
OPT	Option pad
OTG	On-the-go
PCB	Printed circuit board
PFM	Pulse frequency modulation
PLL	Phase locked loop
PM	Power management
PMI	Power management interface
PMIC	Power management integrated circuit
PMOS	P-channel metal-oxide semiconductor
PWB	Printed wiring board
PWM	Pulse-width modulation
PSRR	Power supply rejection ratio
QTI	Qualcomm® Technologies, Inc
RC	Resistance capacitance
RCO	RC oscillator
RF	Radio frequency
RFIC	Radio frequency integrated circuit
RoHS	Restriction of hazardous substances
RTC	Real time clock
RUIM	Removable user identity module
SAT	Semiconductor assembly and test

Table 1-3 Terms and acronyms (cont.)

Term or acronym	Definition
SCSS	Sensor core subsystem
SMIC	Silicon reliability results
SMPL	Sudden momentary power loss
SMPS	Switched-mode power supply (DC-to-DC converter)
SMT	Surface mount technology
SPMI	Serial power management interface
SSC	SMPS step control
SVS	Static voltage scaling
TCXO	Temperature-compensated crystal oscillator
UART	Universal asynchronous receiver/transmitter
UFS	Universal Flash Storage
UICC	Universal integrated circuit card
UIM	User-identity module
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
UVLO	Undervoltage lockout
VCO	Voltage-controlled oscillator
VCTCXO	Voltage-controlled, temperature-controlled, oscillator
VDD	Supply voltage - negative
VREF	Voltage reference
WCD	Wireless connectivity device
WLNSP	Wafer-level NSP
XO	Crystal oscillator
XTAL	Crystal

2 Pad definitions

2.1 Pad assignments

The PM8994/PM8996 device is available in the 225 WLNSP – see Section 4.1 for package details. A high-level view of the pad assignments is shown in Figure 2-1.

1 GND_ S5	2 GND_ S5	3 VDD_ L1	4 VREG _L1	5 VREG _L26	6 XTAL_ 19M_OUT	7 XTAL_ 19M_IN	8 VREG_ RF_CLK	9 VREG _L9	10 VREG _L22	11 VREG _L18	12 VREG _L10	13 VREG _L6	14 GND_ S4	15 GND_ S4
16 VSW _S5	17 VREG _S5	18 VREG _L2	19 VDD_L2_ 26_28	20 VDD_L8_ 16_30	21 VREG _L30	22 BB_ CLK1_EN	23 VREG_ XO	24 VDD_ L5_7	25 VDD_L9_ 10_18_22	26 GPIO _04	27 VREG _L12	28 VREG _S4	29 VSW _S4	30 VSW _S4
31 VDD _S5	32 VDD_ L3_11	33 VREG _L11	34 VREG _L28	35 VREG _L16	36 VREG _L8	37 VREG _L14	38 GND_ XO	39 MPP _03	40 GPIO _08	41 GPIO _03	42 GPIO _02	43 VDD_L6_ 12_32	44 VIN_ LVS1_2	45 VDD _S4
46 GND_ S3	47 GND_ S3	48 VREG _L3	49 AMUX_5	50 AMUX_0	51 GND_ CLKS_XO	52 VREG _L15	53 RF_ CLK2	54 BB_ CLK1	55 MPP _04	56 VDD_ L25	57 VREG _L32	58 VOUT _LVS1	59 VDD _S7	60 VDD _S7
61 VSW _S3	62 VSW _S3	63 VDD _SNS	64 VREG _S3	65 AMUX_1	66 VREF_ XO_THM	67 VDD_ L14_15	68 RF_ CLK1	69 LN_BB _CLK	70 BB_ CLK2	71 VREG _L25	72 SLEEP_ CLK	73 VOUT _LVS2	74 VSW _S7	75 VSW _S7
76 VDD _S3	77 VDD _S3	78 VDD_L4_ 27_31	79 AMUX_ HW_ID	80 AMUX_2	81 GND_ XOADC	82 GND	83 GND_ RF	84 GND	85 MPP _02	86 GPIO _07	87 VREG _S7	88 GPIO _01	89 GND_ S7	90 GND_ S7
91 VDD_ S1	92 VDD_ S1	93 VREG _L27	94 AMUX_4	95 VREG _L31	96 XO_ THERM	97 GND	98 GND	99 GND	100 SPMI _DATA	101 SPMI _CLK	102 GPIO _06	103 VREG _S12	104 GPIO _05	105 VDD _S12
106 VSW _S1	107 VSW _S1	108 VREG _L4	109 VREG _S1	110 AMUX_ PU1	111 AMUX_3	112 GND	113 GND	114 GND	115 PS_HOLD	116 MPP _01	117 AVDD_ BYP	118 VPH_ PWR	119 VSW _S12	120 VSW _S12
121 GND_ S1	122 GND_ S1	123 VREF_ NEG_S1	124 VREG _S6	125 OPT_1	126 GPIO _22	127 GND	128 GND	129 GND	130 KPD_ PWR_N	131 RESIN_N	132 DVDD_ BYP	133 VREF_ NEG_S2_12	134 GND_ S12	135 GND_ S12
136 VDD _S6	137 VDD _S6	138 VREF_ NEG_S6	139 VREF _EBI1 _DQ	140 GND _REF	141 GPIO _21	142 GPIO _20	143 GPIO _16	144 GPIO _12	145 MPP _08	146 GND	147 VREG _S2	148 SHDN_N	149 VDD _S2	150 VDD _S2
151 VSW _S6	152 VSW _S6	153 VREF _EBI0 _CA	154 VCOIN	155 VDD_ APQ_IO	156 REF_ BYP	157 GPIO _19	158 GPIO _15	159 GPIO _11	160 MPP _07	161 MPP _05	162 PON_ RESET_N	163 VCTRL	164 VSW _S2	165 VSW _S2
166 GND_ S6	167 GND_ S6	168 VREF _EBI1 _CA	169 VREF _DDR	170 OPT_2	171 VREG _S11	172 GPIO _18	173 VREG _S10	174 GPIO _10	175 VREG _S9	176 VREG _S8	177 PON_1	178 VREG _L13	179 GND_ S2	180 GND_ S2
181 VREG _L20	182 VREG _L17	183 VREG _L29	184 VREF _EBI0 _DQ	185 VPH_ PWR_2	186 VREF_NEG _S8_9_ 10_11	187 GPIO _17	188 GPIO _14	189 GPIO _13	190 GPIO _09	191 CBL_ PWR_N	192 MPP _06	193 VREG _L24	194 VDD_ L13_19 _23_24	195 VREG _L19
196 VDD_ L20_21	197 VDD_ L17_29	198 VDD_ S11	199 VSW _S11	200 GND_ S11	201 VDD_ S10	202 VSW _S10	203 GND_ S10	204 VDD_ S9	205 VSW _S9	206 GND_ S9	207 VDD _S8	208 VSW _S8	209 GND_ S8	210 VREG _L23
211 VDD_ L20_21	212 VREG _L21	213 VDD_ S11	214 VSW _S11	215 GND_ S11	216 VDD_ S10	217 VSW _S10	218 GND_ S10	219 VDD_ S9	220 VSW _S9	221 GND_ S9	222 VDD _S8	223 VSW _S8	224 GND_ S8	225 GND

Input power management | Output power management | General housekeeping | User interfaces | IC-level interfaces | MPPs and GPIOs | No connection | Power | Ground

Figure 2-1 PM8994/PM8996 pad assignments (top view)

2.2 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
PI	Power input; a pad that handles 10 mA or more of current flow into the device
PO	Power output; a pad that handles 10 mA or more of current flow out of the device
Z	High-impedance (Hi-Z) output
GNDP	Power ground; a pad that handles 10 mA or more of current flow returning to ground. Layout considerations must be made for these pads.
GNDC	Common ground; a pad that does not handle a significant amount of current flow, typically used for grounding digital circuits and substrates.

2.3 Pad descriptions

Table 2-2 Pad description tables

Function	PM8994/PM8996 device
Input power management	Table 2-3
Output power management	Table 2-4
General housekeeping	Table 2-5
User interface	Table 2-6
IC-level interfaces	Table 2-7
Configurable I/Os	Table 2-8
Summary of power supply pads	Table 2-9
Summary of ground pads	Table 2-10

Table 2-3 Pad descriptions – Input power management functions

Pad #	Pad name and/or function	Pad type [1]	Functional description
Input power sources			
118	VPH_PWR	PI	System input power node generated by either the charger or battery
185	VPH_PWR_2	PI	Second system input power node generated by either the charger or battery

Table 2-3 Pad descriptions – Input power management functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
Coin cell or keep-alive battery			
154	VCOIN	AI, AO	Coin cell battery or backup battery charger supply and input. Last remaining available source to maintain xVdd backed registers.

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pad descriptions – Output power management functions

Pad #	Pad name and/or function	Pad type [1]	Functional description
High-frequency buck SMPS circuits			
61, 62	VSW_S3	PO	S3 SMPS switch node
64	VREG_S3	AI	S3 SMPS sense input
76, 77	VDD_S3	PI	S2 SMPS supply power input
46, 47	GND_S3	GNDP	S3 SMPS power ground
29, 30	VSW_S4	PO	S4 SMPS switch node
28	VREG_S4	AI	S4 SMPS sense input
45	VDD_S4	PI	S4 SMPS supply power input
14, 15	GND_S4	GNDP	S4 SMPS power ground
16	VSW_S5	PO	S5 SMPS switch node
17	VREG_S5	AI	S5 SMPS sense input
31	VDD_S5	PI	S5 SMPS supply power input
1, 2	GND_S5	GNDP	S5 SMPS power ground
74, 75	VSW_S7	PO	S7 SMPS switch node
87	VREG_S7	AI	S7 SMPS sense input
59, 60	VDD_S7	PI	S7 SMPS supply power input
89, 90	GND_S7	GNDP	S7 SMPS power ground
Fast transient buck SMPS circuits			
106, 107	VSW_S1	PO	S1 SMPS switch node
109	VREG_S1	AI	S1 SMPS sense input
123	VREF_NEG_S1	AI	S1 SMPS ground sense, route as differential pair with VREG_S1
91, 92	VDD_S1	PI	S1 SMPS supply power input
121, 122	GND_S1	GNDP	S1 SMPS power ground
164, 165	VSW_S2	PO	S2 SMPS switch node
147	VREG_S2	AI	S2 SMPS sense input
149, 150	VDD_S2	PI	S2 SMPS supply power input
179, 180	GND_S2	GNDP	S2 SMPS power ground
151, 152	VSW_S6	PO	S6 SMPS switch node

Table 2-4 Pad descriptions – Output power management functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
124	VREG_S6	AI	S6 SMPS sense input
138	VREF_NEG_S6	AI	S6 SMPS ground sense, route as differential pair with VREG_S6
136, 137	VDD_S6	PI	S6 SMPS supply power input
166, 167	GND_S6	GNDP	S6 SMPS power ground
208, 223	VSW_S8	PO	S8 SMPS switch node
176	VREG_S8	AI	S8 SMPS sense input
207, 222	VDD_S8	PI	S8 SMPS supply power input
209, 224	GND_S8	GNDP	S8 SMPS power ground
205, 220	VSW_S9	PO	S9 SMPS switch node
175	VREG_S9	AI	S9 SMPS sense input
204, 219	VDD_S9	PI	S9 SMPS supply power input
206, 221	GND_S9	GNDP	S9 SMPS power ground
202, 217	VSW_S10	PO	S10 SMPS switch node
173	VREG_S10	AI	S10 SMPS sense input
201, 216	VDD_S10	PI	S10 SMPS supply power input
203, 218	GND_S10	GNDP	S10 SMPS power ground
199, 214	VSW_S11	PO	S11 SMPS switch node
171	VREG_S11	AI	S11 SMPS sense input
186	VREF_NEG_S8_S9_ S10_S11	AI	S8 SMPS, S9 SMPS, S10 SMPS, and S11 SMPS ground sense
198, 213	VDD_S11	PI	S11 SMPS supply power input
200, 215	GND_S11	GNDP	S11 SMPS power ground
119, 120	VSW_S12	PO	S12 SMPS switch node
103	VREG_S12	AI	S12 SMPS sense input
133	VREF_NEG_S2_S12	AI	S2 SMPS and S12 SMPS ground sense
105	VDD_S12	PI	S12 SMPS supply power input
134, 135	GND_S12	GNDP	S12 SMPS power ground
Low dropout regulator (LDO) circuits			
4	VREG_L1	PO	L1 LDO regulated output
18	VREG_L2	PO	L2 LDO regulated output
48	VREG_L3	PO	L3 LDO regulated output
108	VREG_L4	PO	L4 LDO regulated output
8	VREG_RF_CLK	PO	L5 LDO RF clock regulated output and load capacitor connection
13	VREG_L6	PO	L6 LDO regulated output
23	VREG_XO	PO	L7 LDO XO circuit regulated output and load capacitor connection

Table 2-4 Pad descriptions – Output power management functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
36	VREG_L8	PO	L8 LDO regulated output
9	VREG_L9	PO	L9 LDO regulated output
12	VREG_L10	PO	L10 LDO regulated output
33	VREG_L11	PO	L11 LDO regulated output
27	VREG_L12	PO	L12 LDO regulated output
178	VREG_L13	PO	L13 LDO regulated output
37	VREG_L14	PO	L14 LDO regulated output
52	VREG_L15	PO	L15 LDO regulated output
35	VREG_L16	PO	L16 LDO regulated output
182	VREG_L17	PO	L17 LDO regulated output
11	VREG_L18	PO	L18 LDO regulated output
195	VREG_L19	PO	L19 LDO regulated output
181	VREG_L20	PO	L20 LDO regulated output
212	VREG_L21	PO	L21 LDO regulated output
10	VREG_L22	PO	L22 LDO regulated output
210	VREG_L23	PO	L23 LDO regulated output
193	VREG_L24	PO	L24 LDO regulated output
71	VREG_L25	PO	L25 LDO regulated output
5	VREG_L26	PO	L26 LDO regulated output
93	VREG_L27	PO	L27 LDO regulated output
34	VREG_L28	PO	L28 LDO regulated output
183	VREG_L29	PO	L29 LDO regulated output
21	VREG_L30	PO	L30 LDO regulated output
95	VREG_L31	PO	L31 LDO regulated output
57	VREG_L32	PO	L32 LDO regulated output
3	VDD_L1	PI	L1 LDO input supply sourced from S1 SMPS of PMI8994/PMI8996
19	VDD_L2_26_28	PI	L2, L26, and L28 LDO supply input sourced from S3 SMPS
32	VDD_L3_11	PI	L3 LDO and L11 LDO input supply sourced from S3 SMPS
78	VDD_L4_27_31	PI	L4, L27, and L31 LDO input supply sourced from S3 SMPS
24	VDD_L5_7	PI	L5 and L7 LDO input sourced from SMPS S5 used to power low-noise output buffers and XO circuits respectively
43	VDD_L6_12_32	PI	L6, L12, and L32 LDO supply input sourced from S5 SMPS
20	VDD_L8_16_30	PI	L8, L16, and L30 LDO input supply sourced from VPH_PWR
25	VDD_L9_10_18_22	PI	L9, L10, L18, and L22 LDO input supply sourced from VPH_PWR or boost/bypass

Table 2-4 Pad descriptions – Output power management functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
194	VDD_L13_19_23_24	PI	L13, L19, L23, and L24 LDO input supply sourced from VPH_PWR or boost/bypass
67	VDD_L14_15	PI	L14 and L15 LDO input supply sourced from SMPS S5
197	VDD_L17_29	PI	L17 and L29 LDO input supply sourced from VPH_PWR or boost/bypass
196, 211	VDD_L20_21	PI	L20 and L21 LDO supply input sourced from VPH_PWR or boost/bypass
56	VDD_L25	PI	L25 LDO input supply sourced from SMPS S5
Low voltage switches LVS circuits			
44	VIN_LVS1_2	PI	LVS1 low voltage switch and LVS2 low voltage switch supply input sourced from SMPS S4
58	VOUT_LVS1	PO	LVS1 low voltage switch supply output
44	VIN_LVS1_2	PI	LVS1 low voltage switch and LVS2 low voltage switch supply input sourced from SMPS S4
73	VOUT_LVS2	PO	LVS2 low voltage switch supply output

1. See Table 2-1 for parameter and acronym definitions.

Table 2-5 Pad descriptions – General housekeeping functions

Pad #	Pad name and/or function	Pad type [1]	Functional description
HK ADC and analog multiplexer circuits			
96	XO_THERM	AI	XO thermistor resistor divider input
66	VREF_XO_THM	AO	XO thermistor reference voltage connection
79	AMUX_HW_ID	AI	Hardware Revision ID analog input which customers can use to distinguish between their various hardware
50	AMUX_0	AI	AMUX input #0 connected with AMUX channel #57 typically used for thermistor readings
65	AMUX_1	AI	Analog multiplexer (AMUX) input #1 connected with AMUX channel #51 typically used for thermistor readings
80	AMUX_2	AI	AMUX input #2 connected with AMUX channel #52 typically used for thermistor readings
111	AMUX_3	AI	AMUX input #3 connected with AMUX channel #53 typically used for thermistor readings
94	AMUX_4	AI	AMUX input #4 connected with AMUX channel #55 typically used for thermistor readings
49	AMUX_5	AI	AMUX input #5 connected with AMUX channel #56 typically used for thermistor readings
110	AMUX_PU1	AI	AMUX pull up supply input
81	GND_XOADC	GNDP	XO ADC reference ground which should be routed as a thin trace to the XO ground island along with a connection to the main ground plane where there are minimal temperature transients

Table 2-5 Pad descriptions – General housekeeping functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
63	VDD_SNS	AI	VPH_PWR voltage sense input
Sleep clock circuits			
72	SLEEP_CLK	DO	32 kHz sleep clock output to the APQ chipset
19.2 MHz XO and clock buffer circuits			
7	XTAL_19M_IN	AI	19.2 MHz crystal oscillator (XO) input
6	XTAL_19M_OUT	AO	19.2 MHz crystal oscillator (XO) output
68	RF_CLK1	DO	19.2 MHz RF (low noise) XO clock buffer output (1 of 2)
53	RF_CLK2	DO	19.2 MHz RF (low noise) XO clock buffer output (2 of 2)
69	LN_BB_CLK	DO	19.2 MHz baseband (low noise) XO buffer clock output
54	BB_CLK1	DO	19.2 MHz baseband (low power) XO clock buffer output (1 of 2)
70	BB_CLK2	DO	19.2 MHz baseband (low power) XO clock buffer output (2 of 2)
22	BB_CLK1_EN	DI	Hardware control enable for BB_CLK1 buffer when this pad is driven HIGH by the APQ for CXO
38	GND_XO	GNDP	Exclusive ground for 19.2 MHz XTAL circuits which connects directly to the main ground plane through a single dedicated via; this ground pad should not be shared with any other ground pads
83	GND_RF	GNDP	Exclusive ground for all 19.2 MHz clock buffers which connects directly to the main ground plane through a single dedicated via; this ground pad should not be shared with any other ground pads
51	GND_CLKS_XO	GNDP	Exclusive ground for clock XO module shielding which connects directly to the main ground plane through a single dedicated via; this ground pad should not be shared with any other ground pads
PMIC power infrastructure			
117	AVDD_BYP	AO	Bypass capacitor connection for internal aVdd regulator (1.875 V) used to power internal analog infrastructures
132	DVDD_BYP	AO	Bypass capacitor connection for internal dVdd regulator (1.8 V) used to power internal digital infrastructures
156	REF_BYP	AO	Bypass capacitor for dedicated master bandgap regulator; this LDO must only be used for the master bandgap and must not be used as a general LDO output
140	GND_REF	GNDP	Dedicated master bandgap ground reference connection; should be isolated from all other grounds – pad should be connected directly to REF_BYP capacitor ground and main ground plane

1. See Table 2-1 for parameter and acronym definitions.

Table 2-6 Pad descriptions – User interface functions

Pad #	Pad name	Pad type	Functional description
GPIO assignments for user interface functions [1]			
MPP assignments for user interface functions [2]			

1. GPIOs are used for user interface functions as identified in Table 2-8 and are not repeated here. To assign a GPIO a particular function, identify all the application's requirements and map each GPIO to its function – carefully avoiding assignment conflicts. Table 2-8 lists all GPIOs.
2. MPPs are used for user interface functions as identified in Table 2-8 and are not repeated here. To assign an MPP a particular function, identify all the application's requirements and map each MPP to its function – carefully avoiding assignment conflicts. Table 2-8 lists all MPPs.

Table 2-7 Pad descriptions – IC-level interface functions

Pad #	Pad name and/or function	Pad type [1]	Functional description
Option hardware configuration control			
125	OPT_1	DI	Option hardware configuration control pad (1 of 2) where depending on its voltage level (VDD/GND/Hi-Z) will define specific characteristics for the PMIC such as its poweron sequence
170	OPT_2	DI	Option hardware configuration control pad (2 of 2) where depending on its voltage level (VDD/GND/Hi-Z) will define specific characteristics for the PMIC
Poweron/poweroff/reset control			
130	KPD_PWR_N	DI	Input pad generally connected to a keypad poweron button and when grounded will initiate the poweron sequence. Can also be configured for generating a Stage 2 and/or Stage 3 reset if held at a logic LOW for longer durations. Pulled up internally to 1.8 V via dVdd regulator. Cmax = 10 pF
191	CBL_PWR_N	DI	Alternate input pad which can be used to initiate the poweron sequence when grounded; pulled up internally to 1.8 V via dVdd regulator. Cmax = 10 pF
177	PON_1	DI	Poweron input pad when transitioning from LOW to HIGH will initiate the poweron sequence from the PM8994/PM8996 device Cmax = 10 pF
148	SHDN_N	DI	Power-off input pad when transitioning from HIGH to LOW will initiate the power off sequence from the PM8994/PM8996 device Cmax = 10 pF
131	RESIN_N	DI	Input pad used for generating a Stage 2 and/or Stage 3 reset when held logic LOW Cmax = 10 pF
115	PS_HOLD	DI	Power supply hold control input Cmax = 10 pF This signal's main purpose is to tell the PM8994/PM8996 device to keep its power supplies on, and it can initiate a reset or power down when asserted LOW

Table 2-7 Pad descriptions – IC-level interface functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
162	PON_RESET_N	DO	Poweron reset output signal (active LOW) which is deasserted to take the APQ device out of reset after the PMIC poweron sequence has completed and asserted when a reset or shutdown commences Cmax = 10 pF
System power management interface (SPMI) signals			
101	SPMI_CLK	DI	System power management interface communication bus clock signal
100	SPMI_DATA	DI, DO	System power management interface communication bus data signal
Wi-Fi core voltage control			
163	VCTRL	DI	Control pad used to inform the PMIC to change Wi-Fi core voltages for going in and out of retention
Digital I/O input supply			
155	VDD_APQ_IO	PI	1.8 V input supply power for digital I/Os to/from the APQ device; connected externally to S4 SMPS output (VREG_S4)
DDR memory reference outputs			
169	VREF_DDR	AI	Reference voltage input for LPDDR memory
153	VREF_EBI0_CA	AO	Reference voltage supply for EBI0 memory CA
184	VREF_EBI0_DQ	AO	Reference voltage supply for EBI0 memory DQ
168	VREF_EBI1_CA	AO	Reference voltage supply for EBI1 memory CA
139	VREF_EBI1_DQ	AO	Reference voltage supply for EBI1 memory DQ

1. See Table 2-1 for parameter and acronym definitions.

Table 2-8 Pad descriptions – Configurable input/output functions

Pad #	Pad name	Alt function	Pad type [1]	Functional description
Predefined MPP functions – available only at the assigned MPPs				
116	MPP_01		AI, AO, DI, DO	MPP configurable for variety of applications
		VREF_PADS	AO	Analog output for APQ 3 V pad bandgap voltage reference (VREF_PADS)
85	MPP_02		AI, DI, DO	MPP configurable for variety of applications
		US_EURO_HS_SEL	AI	US or Europe headset select
39	MPP_03		AI, AO, DI, DO	MPP configurable for variety of applications
		VREF_DAC	AO	Analog output for APQ WWAN DAC voltage reference
55	MPP_04		AI, DI, DO	MPP configurable for variety of applications
		HDMI_EN	DO	HDMI enable
161	MPP_05		AI, AO, DI, DO	MPP configurable for variety of applications
		SPKR_BOOST_EN	DO	5 V boost enable for stereo speaker
192	MPP_06		AI, AO, DI, DO	MPP configurable for variety of applications
		ENET_RST_N	DO	Ethernet reset
160	MPP_07		AI, AO, DI, DO	MPP configurable for variety of applications
145	MPP_08		AI, AO, DI, DO	MPP configurable for variety of applications
		PRIVACY_LED	DI	Privacy LED current sink
Predefined GPIO functions – available only at the assigned GPIOs				
88	GPIO_01	–	DI, DO	Configurable GPIO for a variety of applications
42	GPIO_02	–	DI, DO	Configurable GPIO for a variety of applications
41	GPIO_03	–	DI, DO	Configurable GPIO for a variety of applications
26	GPIO_04		DO, DI	Configurable GPIO for a variety of applications
		LPG_DRV1	DO	Light pulse generator channel output #1
104	GPIO_05		DO, DI	Configurable GPIO for a variety of applications
		LPG_DRV2	DO	Light pulse generator channel output #2
102	GPIO_06		DO, DI	Configurable GPIO for a variety of applications
		BAT_ALARM_IN	DI	Battery alarm input (digital input) with no BUA pad option
86	GPIO_07		DO, DI	Configurable GPIO for a variety of applications
		LPG_DRV3	DO	Light pulse generator channel output #3
40	GPIO_08		DO, DI	Configurable GPIO for a variety of applications
		LPG_DRV4	DO	Light pulse generator channel output #4

Table 2-8 Pad descriptions – Configurable input/output functions (cont.)

Pad #	Pad name	Alt function	Pad type [1]	Functional description
190	GPIO_09		DO, DI	Configurable GPIO for a variety of applications
		LPG_DRV5	DO	Light pulse generator channel output #5
174	GPIO_10		DO, DI	Configurable GPIO for a variety of applications
		LPG_DRV6	DO	Light pulse generator channel output #6
		BB_CLK2_EN	DI	BB_CLK2 buffer enable (digital input)
189	GPIO_13		DO, DI	Configurable GPIO for a variety of applications
		LN_BBCLK_EN	DI	LN_BB_CLK buffer enable (digital input)
188	GPIO_14		DO, DI	Configurable GPIO for a variety of applications
		CHGR_INT	DI	Interrupt from external charger
158	GPIO_15		DO, DI	Configurable GPIO for a variety of applications; also capable of providing 19.2 MHz divide by clock signals and 32 kHz sleep clock signals
		DIV_CLK1	DO	Divided clock frequency output #1
		SLEEP_CLK2	DO	Alternate sleep clock output #2
143	GPIO_16		DO, DI	Configurable GPIO for a variety of applications; also capable of providing 19.2 MHz divide by clock signals and 32 kHz sleep clock signals
		DIV_CLK2	DO	Divided clock frequency output #2
		SLEEP_CLK3	DO	Alternate sleep clock output #3
187	GPIO_17		DO, DI	Configurable GPIO for a variety of applications; also capable of providing 19.2 MHz divide by clock signals and 32 kHz sleep clock signals
		DIV_CLK3	DO	Divided clock frequency output #3
		SLEEP_CLK4	DO	Alternate sleep clock output #4
172	GPIO_18		DO, DI	Configurable GPIO for a variety of applications; also capable of providing 19.2 MHz divide by clock signals and 32 kHz sleep clock signals
		DIV_CLK3	DO	Divided clock frequency output #3
		SLEEP_CLK5	DO	Alternate sleep clock output #5
157	GPIO_19		DO, DI	Configurable GPIO for a variety of applications
		EXT_REG_EN1	DO	External regulator enable 1 (VPH_PWR)
142	GPIO_20		DO, DI	Configurable GPIO for a variety of applications
		PMI_SPON	DO	Configured as a digital input for the PMI8994/PMI8996 device to instruct the PM8994/PM8996 device to continue secondary poweron sequence

Table 2-8 Pad descriptions – Configurable input/output functions (cont.)

Pad #	Pad name	Alt function	Pad type [1]	Functional description
141	GPIO_21		DO, DI	Configurable GPIO for a variety of applications
		BAT_ALARM_OUT	DO	Battery alarm output for the battery UICC alarm (BUA) function; it is a bidirectional pad that can be used for the APQ device to communicate with the PM8994/PM8996 device to disable UIM LDOs
		BAT_ALARM_IN	DI	Battery alarm input for the PMI8994/PMI8996 device BUA pad option (digital input)
126	GPIO_22	–	DO, DI	Configurable GPIO for a variety of applications

1. See Table 2-1 for parameter and acronym definitions.

NOTE All GPIOs default to digital input with 10 µA pull-down at powerup. During poweron, the PBS programs GPIO_9 and GPIO_19 as digital output at 1.8 V, and GPIO_17 and GPIO_18 as an alternative sleep clock.

All MPPs default to their Hi-Z state at powerup. During poweron, the PBS programs MPP_01 as an analog output at 1.25 V that is used as reference for the APQ and MPP_07 as a digital output at 1.8 V.

NOTE Configure unused MPPs as 0 mA current sinks (Hi-Z) and GPIOs as digital inputs with their internal pull-downs enabled.

Table 2-9 Pad descriptions – Input DC power pads summary

Pad #	Pad name	Pad type [1]	Functional description
118	VPH_PWR	PI	System input power node generated by either the charger or battery
185	VPH_PWR_2	PI	Second system input power node generated by either the charger or battery
3	VDD_L1	PI	L1 LDO input supply sourced from S3 SMPS
19	VDD_L2_26_28	PI	L2 LDO, L26 LDO, and L28 LDO supply input sourced from S3 SMPS
32	VDD_L3_11	PI	L3 LDO and L11 LDO input supply sourced from S3 SMPS
78	VDD_L4_27_31	PI	L4 LDO, L27 LDO, and L31 LDO input supply sourced from S3 SMPS
24	VDD_L5_7	PI	L5 LDO and L7 LDO input sourced from SMPS S5 used to power low-noise output buffers and XO circuits respectively
43	VDD_L6_12_32	PI	L6 LDO, L12 LDO, and L32 LDO supply input sourced from S5 SMPS
20	VDD_L8_16_30	PI	L8 LDO, L16 LDO, and L30 LDO input supply sourced from VPH_PWR
25	VDD_L9_10_18_22	PI	L9 LDO, L10 LDO, L18 LDO, and L22 LDO input supply sourced from VPH_PWR or boost/bypass
194	VDD_L13_19_23_24	PI	L13 LDO, L19 LDO, L23 LDO, and L24 LDO input supply sourced from VPH_PWR or boost/bypass
67	VDD_L14_15	PI	L14 LDO and L15 LDO input supply sourced from SMPS S5

Table 2-9 Pad descriptions – Input DC power pads summary (cont.)

Pad #	Pad name	Pad type [1]	Functional description
197	VDD_L17_29	PI	L17 LDO and L29 LDO input supply sourced from VPH_PWR or boost/bypass
196, 211	VDD_L20_21	PI	L20 LDO and L21 LDO supply input sourced from VPH_PWR or boost/bypass
56	VDD_L25	PI	L25 LDO input supply
155	VDD_APQ_IO	PI	1.8 V input supply

1. See Table 2-1 for parameter and acronym definitions.

Table 2-10 Pad descriptions – Ground pads summary

Pad #	Pad name	Pad type [1]	Functional description
82, 84, 97, 98, 99, 112, 113, 114, 127, 128, 129, 146, 225	GND	GNDC	Command ground for all non-specialized circuits
121, 122	GND_S1	GNDP	S1 SMPS power ground
179, 180	GND_S2	GNDP	S2 SMPS power ground
46, 47	GND_S3	GNDP	S3 SMPS power ground
14, 15	GND_S4	GNDP	S4 SMPS power ground
1, 2	GND_S5	GNDP	S5 SMPS power ground
166, 167	GND_S6	GNDP	S6 SMPS power ground
89, 90	GND_S7	GNDP	S7 SMPS power ground
209, 224	GND_S8	GNDP	S8 SMPS power ground
206, 221	GND_S9	GNDP	S9 SMPS power ground
203, 218	GND_S10	GNDP	S10 SMPS power ground
200, 215	GND_S11	GNDP	S11 SMPS power ground
134, 135	GND_S12	GNDP	S12 SMPS power ground
81	GND_XOADC	GNDP	XO ADC reference ground which should be routed as a thin trace to the XO ground island along with a connection to the main ground plane where there are minimal temperature transients
38	GND_XO	GNDP	Exclusive ground for 19.2 MHz XTAL circuits which connects directly to the main ground plane through a single dedicated via; this ground pad should not be shared with any other ground pads
83	GND	GNDP	Exclusive ground for all 19.2 MHz clock buffers which connects directly to the main ground plane through a single dedicated via; this ground pad should not be shared with any other ground pads
51	GND_CLKS_XO	GNDP	Connects directly to the main ground plane through a single dedicated via; this ground pad should not be shared with any other ground pads.

Table 2-10 Pad descriptions – Ground pads summary (cont.)

Pad #	Pad name	Pad type [1]	Functional description
140	GND_REF	GNDP	Dedicated master bandgap ground reference connection; should be isolated from all other grounds – pad should be connected directly to REF_BYP capacitor ground and main ground plane
Remote negative feedback pads			
123	VREF_NEG_S1	AI	S1 SMPS ground sense; route as differential pair with VREG_S1
133	VREF_NEG_S2_ S12	AI	S2 SMPS and S12 SMPS ground sense
138	VREF_NEG_S6	AI	S6 SMPS ground sense; route as differential pair with VREG_S6
186	VREF_NEG_S8_ S9_S10_S11	AI	S8 SMPS, S9 SMPS, S10 SMPS, and S11 SMPS ground sense

1. See Table 2-1 for parameter and acronym definitions.

Table 2-11 Pad descriptions: no connection, do not connect, and reserved pads

Pad #	Pad name	Pad type	Functional description
159	GPIO_11	DNC	Do not connect; connected internally; do not connect externally.
144	GPIO_12	DNC	Do not connect; connected internally; do not connect externally.

3 Electrical specifications

3.1 Absolute maximum ratings

Operating the PM8994/PM8996 device under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Power supply and related sense voltages				
VPH_PWR, VPH_PWR_2	Handset power-supply voltage	-0.5	+6.0	V
VDD_xx	PMIC power-supply voltages not listed elsewhere (steady state)	-0.5	+6.0	V
	Transient (< 10 ms)	-0.5	+7.0	V
Signal pads				
V_IN	Voltage on any non-power-supply pad [1]	-0.5	V_{XX} + 0.5	V
ESD protection and thermal conditions – see Section 7.1.				

1. V_{XX} is the supply voltage associated with the input or output pad to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature (Table 3-2). The PM8994/PM8996 device meets all performance specifications listed in Section 3.3 through Section 3.11 when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ	Max	Units
Power-supply and related sense voltages					
VPH_PWR, VPH_PWR_2	Handset power-supply voltage [1]	2.5	3.6	4.8	V
VDD_APQ_IO	Pad voltage for digital I/Os to/from the IC	1.75	–	1.85	V

Table 3-2 Operating conditions (cont.)

Parameter		Min	Typ	Max	Units
VDD_xx	PMIC power-supply voltages not listed elsewhere [1]	2.5 [3]	3.6	4.8	V
VCOIN	Coin-cell voltage	2.0	3.0	3.25	V
Signal pads					
V_IN	Voltage on any non-power-supply pad [2]	0	–	V_{XX} + 0.5	V
Thermal conditions					
T_A	Ambient temperature	-30	+25	+85	°C
T_J	Junction temperature	-30	+25	+125	°C

1. Specified range accommodates low-voltage lithium batteries on the low end, and high-voltage lithium batteries on the high end.
2. V_{XX} is the supply voltage associated with the input or output pad to which the test voltage is applied.
3. Except the subregulated LDOs because they follow the voltage that is supplied by the switching regulators.

3.3 DC power consumption

This section specifies DC power-supply currents for the various IC operating modes (Table 3-3 and Table 3-4). Typical currents are based on IC operation at room temperature (+25°C) using default parameter settings.

Table 3-3 PM8994 DC power-supply currents

Parameter		Comments	Min	Typ	Max	Units
I_BAT1	Supply current, active mode [1]	–	–	3.65	4.2	mA
I_BAT2	Supply current, sleep mode [2]	–				
	19.2 MHz XO clock		–	272	326	µA
I_BAT3	Supply current, off mode [3]	–	–	7.6	18	µA
I_COIN	Coin-cell supply current, off mode [4]					
	XTAL off		–	5.4	8	µA
	RC calibration	Average current	–	6.3	9	µA

1. I_BAT1 is the total supply current from the main battery with the PMIC on, crystal oscillators on, BB_CLK1 and LN_BB_CLK on at 19.2 MHz, driving no load, and these voltage regulators on with no load at the following: VREG_S1 = 1.0 V, VREG_S2 = 1.0 V, VREG_S3 = 1.3 V, VREG_S4 = 1.8 V, VREG_S5 = 2.15 V, VREG_S6 = 1.0 V, VREG_S12 = 1.11 V, VREG_L12 = 1.8 V, VREG_L13 = 2.95 V, VREG_L20 = 2.95 V, VREG_L21 = 2.95 V, VREG_L24 = 3.075 V, VREG_L26 = 0.9875 V, VREG_L28 = 1.0 V, VREG_L31 = 1.2 V MPP1 = 1.25 V (analog out), and VREF_LPDDR_CA = 0.5 * (VREF_DDR).
2. I_BAT2 is the total supply current from the main battery with the PMIC on, either the 32 kHz XTAL oscillator or the XO oscillator on, these voltage regulators on with no load and low-power mode enabled: VREG_S1 = 1.0 V, VREG_S2 = 1.8 V, VREG_S3 = 1.3 V, VREG_S4 = 1.8 V, VREG_S5 = 2.15 V, VREG_S12 = 1.11 V, and MPP1 = 1.1 V (digital out). All other regulators are off, XO buffer off, and all CLK_EN signals are low. MBG is in low-power mode.
3. I_BAT3 is the total supply current from the main battery with the PMIC off and the 32 kHz crystal oscillator on. This only applies from -30°C to +60°C.

4. I_COIN is the total supply current from a 3.0 V coin cell with the PMIC off and the following conditions:
   – 32 kHz crystal oscillator off (only applies from -30°C to +60°C).
   – 32 kHz crystal oscillator off and RC calibration enabled with nominal settings (only applies from -30°C to +60°C, and does not include the peak currents when RC calibration is performed).

Table 3-4 PM8996 DC power-supply currents

Parameter		Comments	Min	Typ	Max	Units
I_BAT1	Supply current, active mode [1]	–	–	7.9	8.3	mA
I_BAT2	Supply current, sleep mode [2]	–				
	19.2 MHz XO clock		–	350	370	µA
I_BAT3	Supply current, off mode [3]	–	–	8.6	20	µA
I_COIN	Coin-cell supply current, off mode [4]					
	XTAL off		–	5.4	8	µA
	RC calibration	Average current	–	6.3	9	µA

1. I_BAT1 is the total supply current from the main battery with the PMIC on, crystal oscillators on, BB_CLK1 and LN_BB_CLK on at 19.2 MHz, driving no load, and these voltage regulators on with no load at the following: VREG_S1_S6 = 0.8 V, VREG_S2 = 0.95 V, VREG_S3 = 1.3 V, VREG_S4 = 1.8 V, VREG_S5 = 2.15 V, VREG_S8 = 0.8 V, VREG_S12 = 1.125 V, VREG_L2 = 1.225 V, VREG_L3 = 0.85 V, VREG_L12 = 1.8 V, VREG_L13 = 2.95 V, VREG_L20 = 2.95 V, VREG_L21 = 2.95 V, VREG_L24 = 3.075 V, VREG_L25 = 1.2 V, VREG_L28 = 1.0 V, VREG_L30 = 1.8 V, MPP1 = 1.25 V (analog out).
2. I_BAT2 is the total supply current from the main battery with the PMIC on, XO oscillator on, these voltage regulators on with no load and low-power mode enabled: VREG_S1_S6 = 0.8 V, VREG_S2 = 0.95 V, VREG_S3 = 1.3 V, VREG_S4 = 1.8 V, VREG_S5 = 2.15 V, VREG_S8 = 0.8 V, VREG_S12 = 1.125 V, VREG_L3 = 0.85 V, VREG_L25 = 1.2 V, and VREG_L30 = 1.8 V. All other regulators are off, XO buffer off, and all CLK_EN signals are low. MBG is in low-power mode.
3. I_BAT3 is the total supply current from the main battery with the PMIC off. This only applies from -35°C to +65°C.
4. I_COIN is the total supply current from a 3.0 V coin cell with the PMIC off. This only applies from -30°C to +60°C, and does not include the peak currents when RC calibration is performed.

3.4 Digital logic characteristics

PM8994/PM8996 digital I/O characteristics such as voltage levels, current levels, and capacitance are specified in Table 3-5.

Table 3-5 Digital I/O characteristics

Parameter		Comments [4]	Min	Typ	Max	Units
V_{IH}	High-level input voltage	–	0.65 × V_{IO}	–	V_{IO} + 0.3	V
V_{IL}	Low-level input voltage	–	-0.3	–	0.35 · V_{IO}	V
V_{SHYS}	Schmitt hysteresis voltage	–	15	–	–	mV
I_L	Input leakage current [1]	V_{IO} = max, V_{IN} = 0 V to V_{IO}	-0.20	–	0.20	µA
V_{OH}	High-level output voltage	I_{out} = I_{OH}	V_{IO} - 0.45	–	V_{IO}	V
V_{OL}	Low-level output voltage	I_{out} = I_{OL}	0	–	0.45	V
I_{OH}	High-level output current [2]	V_{out} = V_{OH}	3	–	–	mA
I_{OL}	Low-level output current [2]	V_{out} = V_{OL}	–	–	-3	mA

Table 3-5 Digital I/O characteristics (cont.)

Parameter		Comments [4]	Min	Typ	Max	Units
I_{OH_XO}	High-level output current [2]	XO digital clock outputs only	6	–	–	mA
I_{OL_XO}	Low-level output current [2]	XO digital clock outputs only	–	–	-6	mA
C_{IN}	Input capacitance [3]	–	–	–	5	pF

1. MPP and GPIO pads comply with the input leakage specification only when configured as a digital input or set to the tri-state mode.
2. Output current specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pads (such as MPP and GPIO pads).
3. Input capacitance is guaranteed by design, but is not 100% tested.
4. V_{IO} is the supply voltage for the PM IC interface (most PMIC digital I/Os).

3.5 Input power management

All parameters associated with input power management functions are specified in this section.

3.5.1 Coin-cell charging

Coin-cell charging is enabled through software control and powered from VBAT. The on-chip charger is implemented using a programmable voltage source and a programmable series resistor. Coin-cell charging performance is specified in Table 3-6.

Table 3-6 Coin-cell charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
Target regulator voltage [1]	V_{IN} > 3.3 V, I_{CHG} = 100 µA	2.50	3.10	3.20	V
Target series resistance [2]	–	800	–	2100	Ω
Coin-cell charger voltage error	I_{CHG} = 0 µA	-5	–	+5	%
Coin-cell charger resistor error	–	-20	–	+20	%
Dropout voltage [3]	I_{CHG} = 2 mA	–	–	200	mV
Ground current, charger enabled	PMIC = off; VCOIN = open				
VBAT = 3.6 V, T = 27ºC		–	4.5	–	µA
VBAT = 2.5–5.5 V		–	–	8	µA

1. Valid regulator voltage settings are 2.5, 3.0, 3.1, and 3.2 V.
2. Valid series resistor settings are 800, 1200, 1700, and 2100 Ω.
3. Set the input voltage (VBAT) to 3.5 V. Note the charger output voltage; call this value V_0. Decrease the input voltage until the regulated output voltage (V_1) drops 100 mV ($V_1 = V_0 – 0.1$ V). The voltage drop across the regulator under this condition is the dropout voltage ($V_{dropout}$ = VBAT – V_1).

3.6 Output power management

Output power management circuits include:

- Bandgap voltage reference circuit

- High-frequency switched-mode power supply (HF-SMPS) circuits
- Generation 2.5 fast-transient SMPS (FT-SMPS) circuits
- LDO linear regulators
- Voltage switches

The PM8994/PM8996 device is supplemented by the PMI8994/PMI8996 device to provide all the regulated voltages needed for most wireless handset applications. Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, to support power-management sequencing, and to meet different voltage-level requirements.

A total of 44 programmable voltage regulators are provided by the PM8994/PM8996 device, with all outputs derived from a common bandgap reference circuit. Each regulator can be set to a low-power mode for power savings.

A high-level summary of all regulators and their intended uses is presented on the subsequent pages.

Table 3-7 PM8994 regulators and their intended uses

Function	Circuit type	Default voltage (V) [2]	Specified range (V) [3]	Programmable range (V)	Rated current (mA)	Default on	Input source	Expected use
S1	FT-SMPS	1.000	0.375–1.125	0.375–1.275	4000	Y		APQ digital core
S6	FT-SMPS	1.000	0.375–1.125	0.375–1.275	4000	Y		
S2	FT-SMPS	1.110	0.5875–1.125	0.375–1.275	4000	Y		APQ memory
S12	FT-SMPS	1.110	0.5875–1.125	0.375–1.275	4000	Y		
S3	HF-SMPS	1.300	0.375–1.400	0.375–3.050	3500	Y		LDOs 2, 3, 4, 11, 26, 27, 28, and 31 for subregulation
S4 [1]	HF-SMPS	1.800	1.700–1.950	0.375–3.050	2000	Y		Most digital I/Os, APQ pad groups 3 and 7, RF, LVS, audio switches, connectivity, LPDDR, eMMC, EEPROM, UFS, sensors, MHL, displays, and home key
S5	HF-SMPS	2.150	1.700–2.300	0.375–3.050	2000	Y		Audio buck and LDOs 5, 6, 7, 12, 14, 15, 25, and 32 for sub-regulation
S7	HF-SMPS	1.000	0.375–1.125	0.375–3.050	3500	N		
S8	FT-SMPS	1.000	0.375–1.125	0.375–1.275	4000	Y		APQ APC0
S9	FT-SMPS	1.000	0.375–1.125	0.375–1.275	4000	N		APQ APC1
S10	FT-SMPS	1.000	0.375–1.125	0.375–1.275	4000	N		
S11	FT-SMPS	1.000	0.375–1.125	0.375–1.275	4000	N		
L1	NMOS LDO	1.000	0.900–1.300	0.375–1.525	1200	N		RFICs
L2	NMOS LDO	1.225	0.950–1.300	0.750–1.525	300	N		MIPI CSI and DSI
L3	NMOS LDO	1.200	0.900–1.300	0.375–1.525	1200	N		Camera
L4	NMOS LDO	1.225	0.950–1.430	0.750–1.525	300	N		APQ analog low-V
L5	Low-noise LDO	1.740	1.700–1.950	1.380–2.220	On-chip only	N		Internally used by PMIC
L6	PMOS LDO	1.800	1.150–3.600	0.750–4.900	150	N		USB
L7	Low-noise LDO	1.740	1.700–1.950	1.380–2.220	On-chip only	N		Internally used by PMIC
L8	PMOS LDO	1.800	1.700–1.950	0.750–4.900	50	N		PMIC XO/HK ADC
L9	PMOS LDO	1.80 or 2.95	1.620–3.600	0.750–4.900	150	N		Pad group 5
L10	PMOS LDO	1.80 or 2.95	1.620–3.600	0.750–4.900	150	N		Pad group 6
L11	NMOS LDO	1.200	0.950–1.430	0.750–1.525	300	N		Audio core, analog

Table 3-7 PM8994 regulators and their intended uses (cont.)

Function	Circuit type	Default voltage (V) [2]	Specified range (V) [3]	Programmable range (V)	Rated current (mA)	Default on	Input source	Expected use
L12 [1]	PMOS LDO	1.800	1.620–3.600	0.750–4.900	300	Y		APQ CXO, pad groups 9 and 11, APQ PCIe, UFS, HDMI and PLLs; display I/Os, BB clock outputs (including LN_BB_CLK)
L13	PMOS LDO	1.80 or 2.95	1.620–3.600	0.750–4.900	150	Y		APQ pad group 2 SDC
L14	PMOS LDO	1.800	1.620–3.600	0.750–4.900	150	N		Available
L15	PMOS LDO	1.850	1.620–3.300	0.750–4.900	300	N		APQ analog – high V
L16	PMOS LDO	2.700	2.560–3.600	0.750–4.900	150	N		QTI front-end
L17	PMOS LDO	2.700	1.620–3.600	0.750–4.900	300	N		Camera – analog
L18	PMOS LDO	2.850	1.620–3.600	0.750–4.900	300	N		Sensors
L19	PMOS LDO	2.800	1.620–3.600	0.750–4.900	600	N		QTI front-end
L20	PMOS LDO	2.950	1.620–3.600	0.750–4.900	600	Y		eMMC memory, UFS
L21	PMOS LDO	2.950	1.620–3.600	0.750–4.900	800	Y		SD/MMC card
L22	PMOS LDO	3.000	1.620–3.600	0.750–4.900	150	N		DSI, touchscreen
L23	PMOS LDO	2.800	1.620–3.600	0.750–4.900	600	N		Camera – analog
L24	PMOS LDO	3.075	1.620–3.600	0.750–4.900	150	Y		USB
L25	PMOS LDO	1.000	0.950–1.300	0.750–4.900	600	N		Available
L26	NMOS LDO	0.988	0.380–1.300	0.375–1.525	600	Y		EBI
L27	NMOS LDO	1.050	0.950–1.300	0.750–1.525	300	N		Camera
L28	NMOS LDO	1.000	0.950–1.300	0.750–1.525	300	Y		APQ PCIe, UFS, and PLLs
L29	PMOS LDO	2.800	1.620–3.600	0.750–4.900	300	N		Camera – analog
L30	PMOS LDO	1.800	1.700–3.600	0.750–4.900	50	Y		Wireless connectivity
L31	NMOS LDO	1.200	0.550–1.300	0.375–1.525	600	Y		APQ pad group 10 UFS and UFS
L32	PMOS LDO	1.800	1.700–3.600	0.750–4.900	50	N		GPS eLNA
LVS1	Low-V switch	–	1.700–1.950	–	300	N		Cameras
LVS2	Low-V switch	–	1.700–1.950	–	100	N		Sensors; touchscreen

1. S4 and L12 power internal circuits that are limited to 1.8 V operation; they should not exceed the maximum stated in their programmable ranges. They are used as the internal dVdd source after powerup; its programmed voltage should not be changed, and it should not be turned off.
2. All regulators have default voltage settings, whether they default on or not; the voltage and state depends upon the programmable boot sequencer (PBS) configuration.
3. The specified voltage range is the programmed range for which performance is guaranteed to meet all specs. For usage outside this range, submit a case to QTI for approval.

Table 3-8 PM8996 regulators and their intended uses

Function	Circuit type	Default voltage (V) [2]	Specified range (V) [3]	Programmable range (V)	Rated current (mA) [4]	Default on	Expected use
S1	FT-SMPS	0.800	0.375–1.125	0.375–1.275	4000	Y	APQ digital core
S6	FT-SMPS	0.800	0.375–1.125	0.375–1.275	4000	Y	
S2	FT-SMPS	0.95	0.5875–1.125	0.375–1.275	4000	Y	APQ memory
S12	FT-SMPS	1.125	0.5875–1.125	0.375–1.275	4000	Y	LPDDR4
S3	HF-SMPS	1.300	0.375–1.400	0.375–3.050	3500 [4]	Y	LDOs 2, 3, 4, 11, 26, 27, 28, and 31 for subregulation
S4 [1]	HF-SMPS	1.800	1.700–1.950	0.375–3.050	2000 [4]	Y	Most digital I/Os, APQ always on pad groups 3 and pad group 7, RF, LVS, audio switches, connectivity, LPDDR, eMMC, EEPROM, UFS, sensors, MHL, displays, and home key
S5	HF-SMPS	2.150	1.700–2.300	0.375–3.050	2000 [4]	Y	Audio buck and LDOs 5, 6, 7, 12, 14, 15, 25, and 32 for sub-regulation
S7	HF-SMPS	0.800	0.375–1.125	0.375–3.050	3500 [4]	N	
S8	FT-SMPS	0.800	0.375–1.125	0.375–1.275	4000	Y	EBI
S9	FT-SMPS	0.800	0.375–1.125	0.375–1.275	4000	Y	APQ APC
S10	FT-SMPS	0.800	0.375–1.125	0.375–1.275	4000	Y	
S11	FT-SMPS	0.800	0.375–1.125	0.375–1.275	4000	Y	
L1	NMOS LDO	1.000	0.900–1.300	0.375–1.525	1200	N	RFICs
L2	NMOS LDO	1.225	0.950–1.300	0.750–1.525	300	Y	MIPI CSI, DSI, and PLL
L3	NMOS LDO	0.850	0.380–1.300	0.375–1.525	1200	N	Available
L4	NMOS LDO	1.225	0.950–1.430	0.750–1.525	300	N	APQ analog low-V
L5	Low-noise LDO	1.740	1.700–1.950	1.380–2.220	On-chip only	N	Internally used by PMIC
L6	PMOS LDO	1.200	1.150–3.600	0.750–4.900	150	N	WCD
L7	Low-noise LDO	1.740	1.700–1.950	1.380–2.220	On-chip only	N	Internally used by PMIC
L8	PMOS LDO	1.800	1.700–1.950	0.750–4.900	50	N	PMIC XO/HK ADC
L9	PMOS LDO	1.80 or 2.95	1.620–3.600	0.750–4.900	150	N	Pad group 5
L10	PMOS LDO	1.80 or 2.95	1.620–3.600	0.750–4.900	150	N	Pad group 6
L11	NMOS LDO	1.150	0.950–1.430	0.750–1.525	300	N	Available
L12 1	PMOS LDO	1.800	1.620–3.600	0.750–4.900	300	Y	APQ CXO, pad groups 9 and 11, APQ PCIe, UFS, HDMI and PLLs; display I/Os, and BB clock outputs (including LN_BB_CLK)
L13	PMOS LDO	1.80 or 2.95	1.620–3.600	0.750–4.900	150	Y	APQ pad group 2 SDC

Table 3-8 PM8996 regulators and their intended uses (cont.)

Function	Circuit type	Default voltage (V) [2]	Specified range (V) [3]	Programmable range (V)	Rated current (mA) [4]	Default on	Expected use
L14	PMOS LDO	1.800	1.620–3.600	0.750–4.900	150	N	APQ analog – high V
L15	PMOS LDO	1.850	1.620–3.300	0.750–4.900	300	N	APQ analog – high V
L16	PMOS LDO	2.700	2.560–3.600	0.750–4.900	150	N	QTI front-end
L17	PMOS LDO	2.500	1.620–3.600	0.750–4.900	300	N	Camera – analog
L18	PMOS LDO	2.850	1.620–3.600	0.750–4.900	300	N	RF antenna switches
L19	PMOS LDO	2.800	1.620–3.600	0.750–4.900	600	N	Sensors
L20	PMOS LDO	2.950	1.620–3.600	0.750–4.900	600	Y	eMMC memory, UFS
L21	PMOS LDO	2.950	1.620–3.600	0.750–4.900	800	Y	SD/MMC card
L22	PMOS LDO	3.000	1.620–3.600	0.750–4.900	150	N	DSI, touchscreen
L23	PMOS LDO	2.800	1.620–3.600	0.750–4.900	600	N	Camera – analog
L24	PMOS LDO	3.075	1.620–3.600	0.750–4.900	150	Y	USB
L25	PMOS LDO	1.200	0.950–1.300	0.750–4.900	600	Y	UFS
L26	NMOS LDO	0.800	0.380–1.300	0.375–1.525	600	N	SCSS core
L27	NMOS LDO	1.000	0.950–1.300	0.750–1.525	300	N	Available
L28	NMOS LDO	1.000	0.885–0.955	0.750–1.525	300	Y	APQ PCIe, UFS, and PLLs
L29	PMOS LDO	2.800	1.620–3.600	0.750–4.900	300	N	Camera – analog
L30	PMOS LDO	1.800	1.700–3.600	0.750–4.900	50	Y	Wireless connectivity
L31	NMOS LDO	1.200	0.550–1.300	0.375–1.525	600	N	SCSS memory
L32	PMOS LDO	1.800	1.700–3.600	0.750–4.900	50	N	GPS eLNA
LVS1	Low-V switch	–	1.700–1.950	–	300	N	Cameras
LVS2	Low-V switch	–	1.700–1.950	–	100	N	Sensors; touchscreen

1. S4 and L12 are power internal circuits that are limited to 1.8 V operation; they should not exceed the maximum stated in their programmable ranges. They are used as the internal dVdd source after power-up; its programmed voltage should not be changed, and it should not be turned off.
2. All regulators have default voltage settings, whether they default on or not; the voltage and state depends upon the programmable boot sequencer (PBS) configuration.
3. The specified voltage range is the programmed range for which performance is guaranteed to meet all specifications. For usage outside this range, submit a case to QTI for approval.
4. HF-bucks are reconfigured in SBL to provide lower current than the rated current. This cannot be changed by customers.

3.6.1 Reference circuit

All PMIC regulator circuits, and some other internal circuits, are driven by a common, on-chip voltage reference circuit. An on-chip series resistor supplements an off-chip 0.1 µF bypass capacitor at the REF_BYP pad to create a lowpass function that filters the reference voltage distributed throughout the device.

NOTE: Do not load the REF_BYP pad. Use an MPP configured as an analog output if the reference voltage is needed off-chip.

Applicable voltage reference performance specifications are given in Table 3-9.

Table 3-9 Voltage reference performance specifications

Parameter	Comments	Min	Typ	Max	Units
Nominal internal VREF	At REF_BYP pad	–	1.250	–	V
Output voltage deviations					
Normal operation	Over temperature only, -20 to +120ºC	-0.32	–	+0.32	%
Normal operation	All operating conditions	-0.50	–	+0.50	%
Sleep mode	All operating conditions	-1.00	–	+1.00	%

3.6.2 HF-SMPS

The PM8994/PM8996 device includes four high-frequency switched-mode power supply (HF-SMPS) circuits. They support PWM and PFM modes, and the automatic transition between PWM and PFM modes, depending on the load current. Pertinent performance specifications are given in Table 3-10.

Table 3-10 HF-SMPS performance specifications

Parameter	Comments [1, 2]	Min	Typ	Max	Units
Output voltage ranges	Programmable range				
25 mV steps		1.550	–	3.1250	V
12.5 mV steps		0.375	–	1.5625	V
Rated load current (I_rated)	Continuous current delivery				
PWM mode	SMPS4 and SMPS5	2000	–	–	mA
	SMPS3 and SMPS7	3500			
PFM mode		200	–	–	mA
Peak inductor current limit (OCP)	VREG pad shorted; I_limit set via SPMI	0.7 × I_limit	I_limit	1.3 × I_limit	mA
Overall output error	Voltage error, load and line regulation, plus temperature and process variations				
PWM mode	V_out > 1.0 V, I_rated /2	-2	–	2	%
	V_out < 1.0 V, I_rated /2	-20	–	20	mV
PFM mode	V_out > 1.0 V, I_rated /2	-2	–	4	%
	V_out < 1.0 V, I_rated /2	-20	–	40	mV
Temperature coefficient	–	–	–	±100	ppm/°C

Table 3-10 HF-SMPS performance specifications (cont.)

Parameter	Comments [1, 2]	Min	Typ	Max	Units
Enable settling time	From enable to within 1% of final value	–	5	20	ms
Enable overshoot	Slow start, no load	–	–	70	mV
Pull-down impedance	–	–	25	–	Ω
Voltage step settling time per LSB	To within 1% of final value	–	–	10	µs
Response to load transitions					
V_out ≥ 1.8 V, V_in ≥ 3.0 V	Load step: 300 mA	-40	–	70	mV
V_out ≥ 1.8 V, V_in ≥ 3.1 V	Load step: 400 mA	-50	–	70	mV
V_out < 1.8 V, V_in ≥ 3.0 V	Load step: 400 mA	-40	–	70	mV
Response to PWM/PFM and PFM/PWM transitions	20 mA load	-40	–	70	mV
Output ripple voltage	Tested at the switching frequency				
PWM pulse-skipping mode	40 mA load; 20 MHz measurement bandwidth	–	20	40	mVpp
PWM non-pulse-skipping mode	I_rated; 20 MHz measurement bandwidth	–	10	20	mVpp
PFM mode	20 mA load; 20 MHz measurement bandwidth	–	–	50	mVpp
Load regulation	V_in ≥ V_out + 1 V; I_load = 0.01 × I_rated to I_rated	–	–	0.25	%
Line regulation	V_in = 3.2–4.2 V; I_load = 100 mA	–	–	0.25	%/V
Power-supply ripple rejection	PSRR				
50 Hz–1 kHz		40	–	–	dB
1–100 kHz		20	–	–	dB
100 kHz–1 MHz		30	–	–	dB
Output noise	–				
F < 5 kHz		–	-101	–	dBm/Hz
F = 5–10 kHz		–	-106	–	dBm/Hz
F = 10–500 kHz		–	-106	–	dBm/Hz
F = 500–1 MHz		–	-116	–	dBm/Hz
F > 2 MHz		–	-116	–	dBm/Hz
Ground current	No load				
PWM mode		–	550	750	µA
PFM mode (auto)		–	50	70	µA
PFM mode (manual)		–	20	30	µA

1. All specifications apply over the device's operating conditions, load current range, and capacitor ESR range, unless noted otherwise.
2. Performance characteristics that may degrade if the rated output current is exceeded:
   • Voltage error • Efficiency • Output ripple voltage

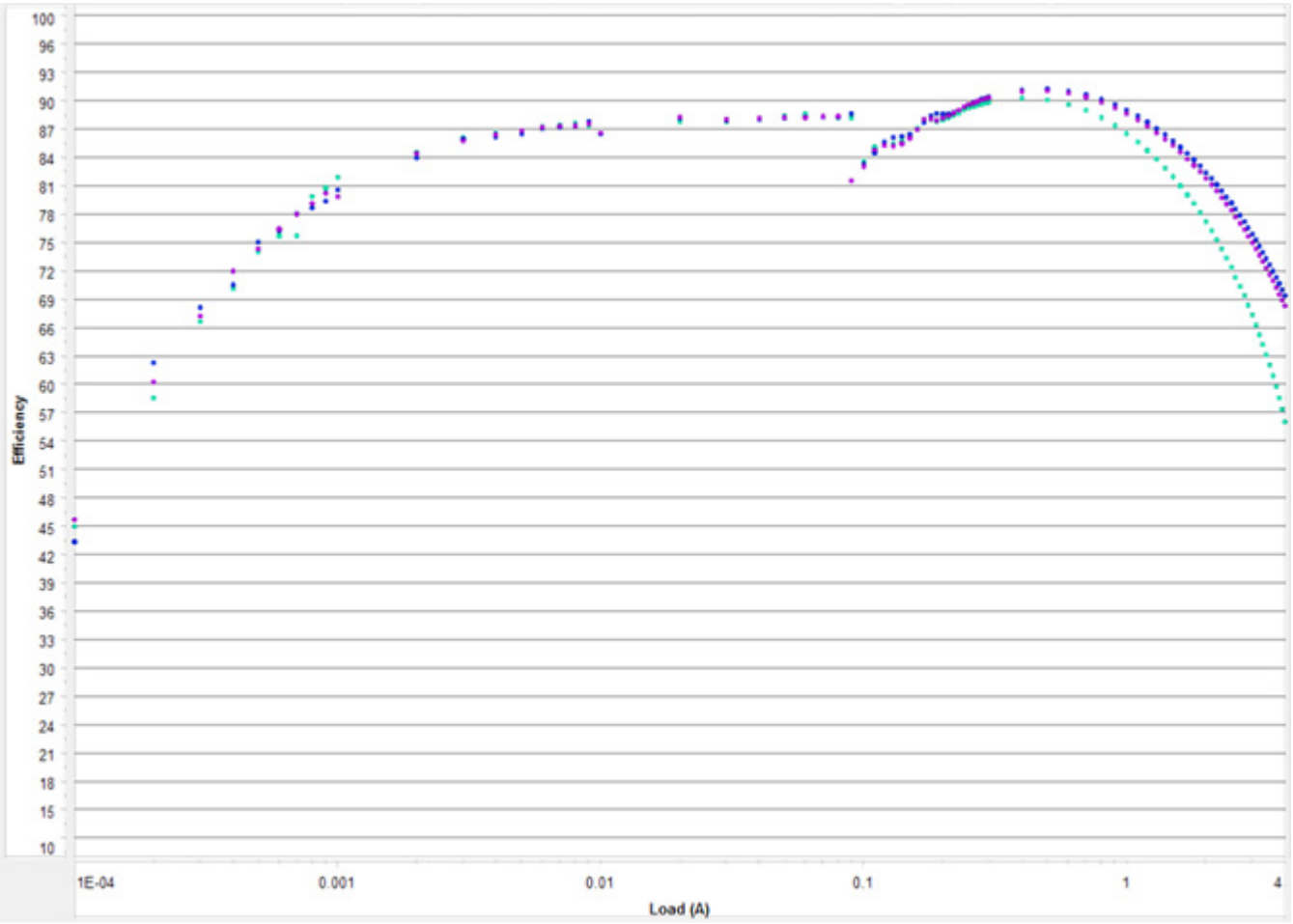


Figure 3-1 PM8994/PM8996 S3A efficiency plot on three devices (VBAT = 3.8 V and Vout = 1.8 V)

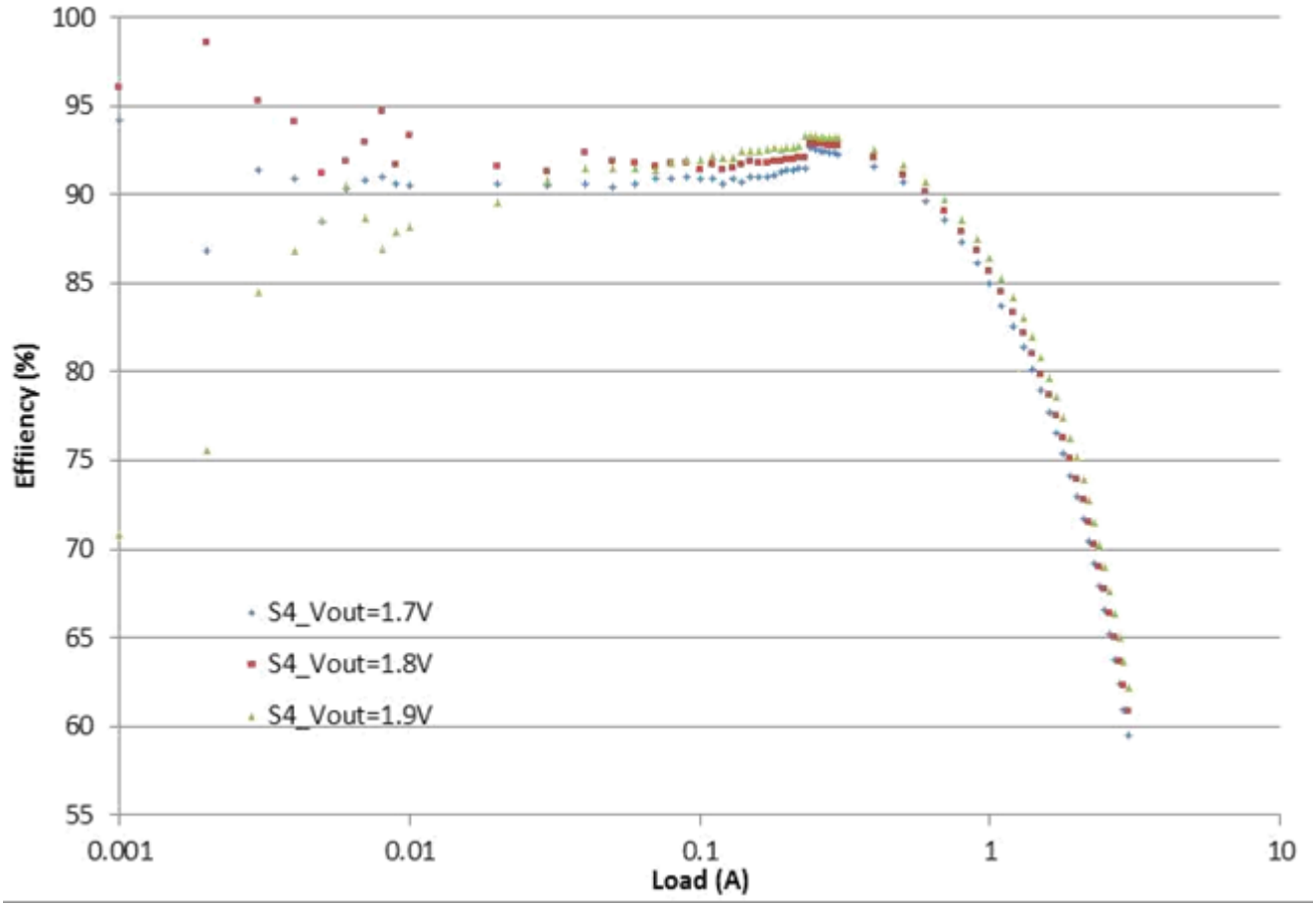


Figure 3-2 PM8994/PM8996 S4A efficiency plot under three voltage output conditions (VBAT = 3.7 V)

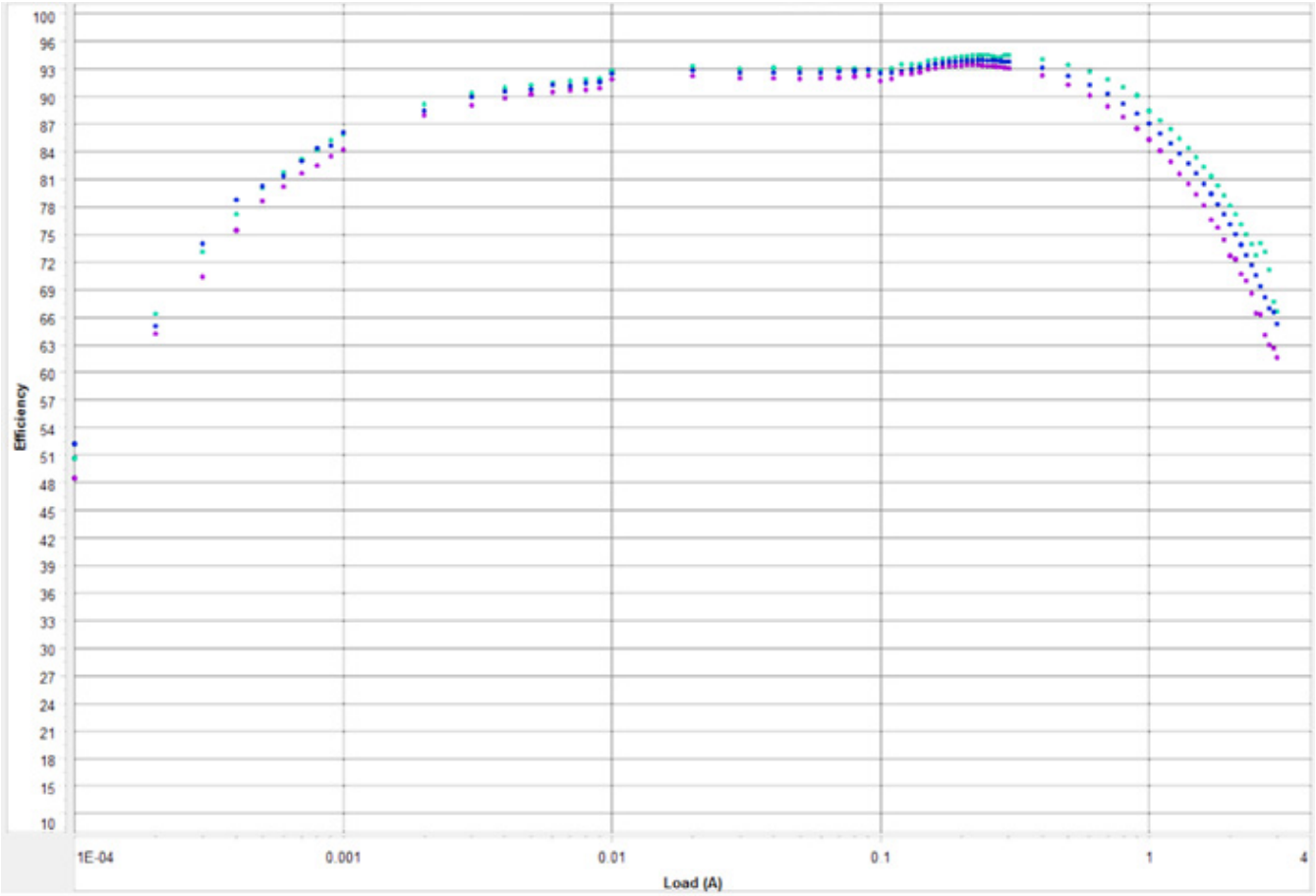


Figure 3-3 PM8994/PM8996 S5A efficiency plot on three devices (VBAT = 3.8 V and Vout = 2.15 V)

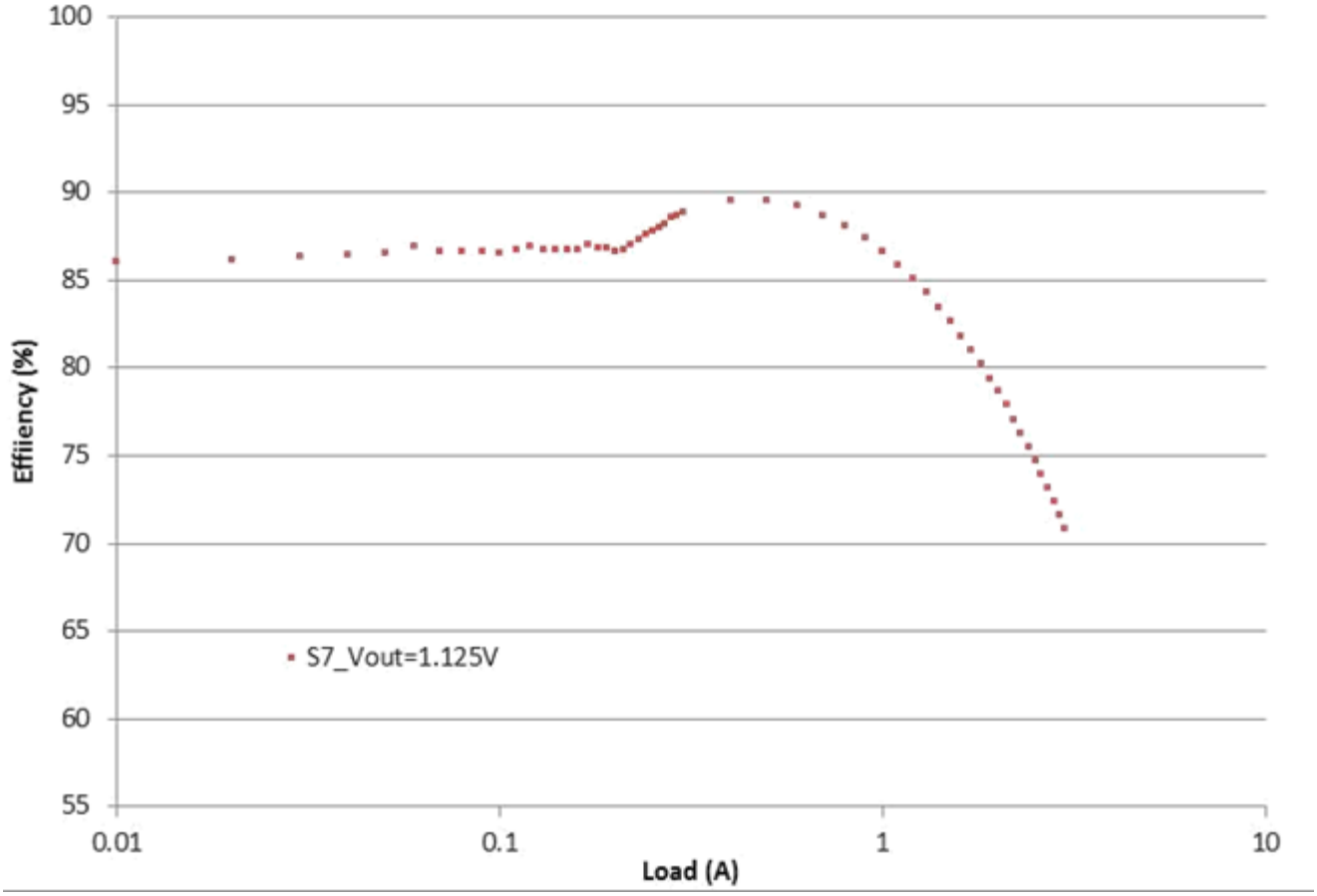


Figure 3-4 PM8994/PM8996 S7A efficiency plot (VBAT = 3.7 V and Vout = 1.125 V)

3.6.3 FT-SMPS

The PM8994/PM8996 device includes eight FT-SMPS circuits. For more information, see Table 3-7 and Table 3-8 for the regulator usages.

All FT-SMPS circuits can be combined for multi-phase operation. PWM, PFM, and Pulse skipping modes are supported. New features introduced in the FT-SMPS are autonomous phase control (APC) and autonomous mode control (AMC). APC is where in multi-phase operation, the phase count is autonomously managed in the hardware to select the appropriate number of phases for optimal efficiency based on the operative load current. AMC is where hardware manages the selection of PWM or PFM mode based on the operative load current. Pertinent **target** performance specifications are given in Table 3-11.

Table 3-11 FT-SMPS performance specifications

Parameter	Comments [1, 2, 3]	Min	Typ	Max	Units
General characteristics					
Output voltage range	■ LV range ■ MV range	0.350 0.700	– –	1.350 2.200	V V
VSW absolute maximum DC voltage [4]	DC condition only	-0.5	–	6	V
CMC NPM or AMC NPM (any number of phases)					
Rated load current	I_rated per phase	4.0	–	–	A
DC output voltage accuracy	Including MBG, make tolerance, line and load regulation, and temperature (-30°C to 125°C) ■ VREG ≥ 0.8 ■ VREG < 0.8	 -2 -16	 – –	 +2 +16	 % mV
Ripple voltage	Measured across C_{OUT} where sense lines are tapped	–	7	15	mVpp
Line transient response	GSM burst induced line transient is represented by: Rbat = 350 mΩ, Istep = 2 A with 10 µs slew, and VPH_PWR capacitance = 100 µF	–	–	20	mVpp
CMC NPM or AMC NPM (multiphase)					
Phase current mismatch	Relative to the ideal balanced current	-25	–	+25	%
Ground current					
Ground current CMC NPM	No load, single phase	–	0.55	0.80	mA
Ground current per phase CMC NPM or AMC NPM	No load, multiphase	–	1.9	2.3	mA
Ground current CMC LPM	No load, single or multiphase (sleep configuration commanded LPM)	–	55	90	µA
Ground current per phase AMC LPM	No load, single or multiphase	–	80	110	µA

Table 3-11 FT-SMPS performance specifications (cont.)

Parameter	Comments [1, 2, 3]	Min	Typ	Max	Units
CMC NPM or AMC load transient (any number of phases)					
Response to load transient (undershoot/overshoot)	2 A load step per phase [5] Transient step ~100 ns, 1 V output [6]	-50	–	+80	mV
CMC LPM or AMC LPM, CPC, or APC (any number of phases)					
DC output voltage accuracy	Including MBG, make tolerance, line and load regulation, and temperature (-30°C to 125°C) ■ VSET ≥ 0.8 V ■ VSET < 0.8 V	 -2 -16	 – –	 +4 +32	 % mV
Ripple voltage	Measured across C_{OUT} where sense lines are tapped ■ Single phase ■ Multiphase	 – –	 25 20	 40 35	 mVpp mVpp
CMC LPM (any number of phases)					
Rated load current	–	–	0.8	–	A
Transition specifications					
Phase-adding warm up time	NPM CPC change in phase count	–	25	–	µs
Phase current settling time	Time to achieve phase-current match (steady state loading, all active phases in CCM, and change in phase count)	–	–	200	µs
Other general characteristics					
Enable settling time	V_{OUT} slewing to within 1% of the final value	–	200	–	µs
Voltage stepper (undershoot/overshoot)	1 LSB step slewing	-5	–	+5	mV
Peak output impedance	1 kHz–1 MHz	–	–	40	mΩ
Discharge impedance	–	–	32	–	Ω

1. General specifications for the FTS 2.5 apply overall operating conditions of supply, temperature, process, and component variances except where noted.
2. Default components are assumed (470 nH, 2 × 22 µF per phase) along with deployed configurations for the APQ8096SGE chipset lineup.
3. Where parametric performance is influenced by external components, baseline components are assumed. Values listed are the component's specified values, not the derated values. De-rating must be accounted for to ensure robustness. The initial assumption is 50% de-rating on capacitors pending further assessment of specific component selections (a rough allowance for temperature, tolerance, and voltage de-rating).
4. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.
5. Based on APQ8096SGE power-grid requirement, not all PM8996 FT-SMPS are required to support a 2 A load step. Exceptions for the PM8996 device are as follows: 1.5 A for S1, S6 and S2, 0.9 A for S8, and 1 A for S12.
6. + 100 mV maximum overshoot for V_{OUT} < 0.7 V.

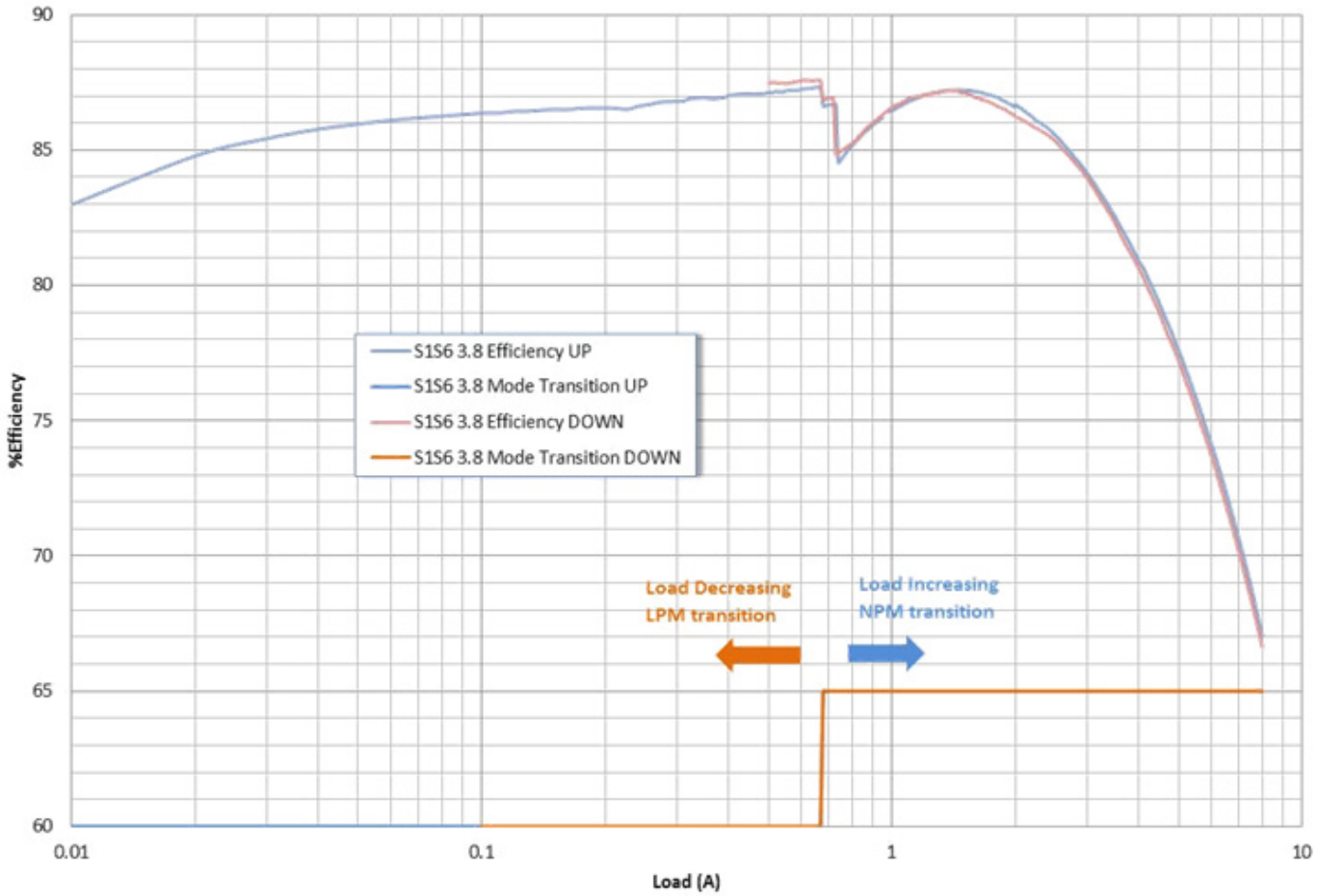


Figure 3-5 PM8994/PM8996 dual-phase S1/S6 efficiency plot (VBAT = 3.8 V and Vout = 1 V)

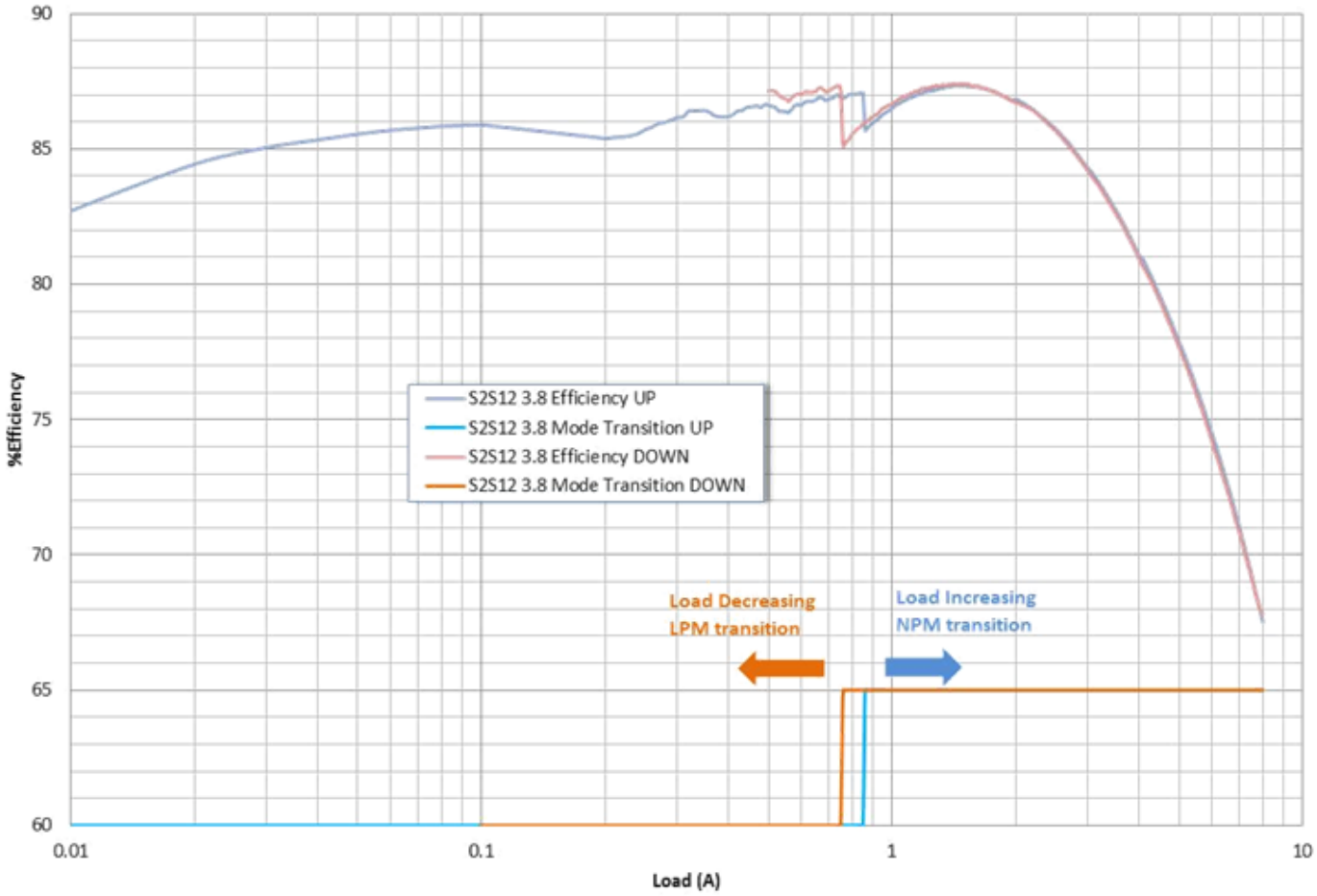


Figure 3-6 PM8994/PM8996 dual-phase S2/S12 efficiency plot (VBAT= 3.8 V and Vout = 1 V)

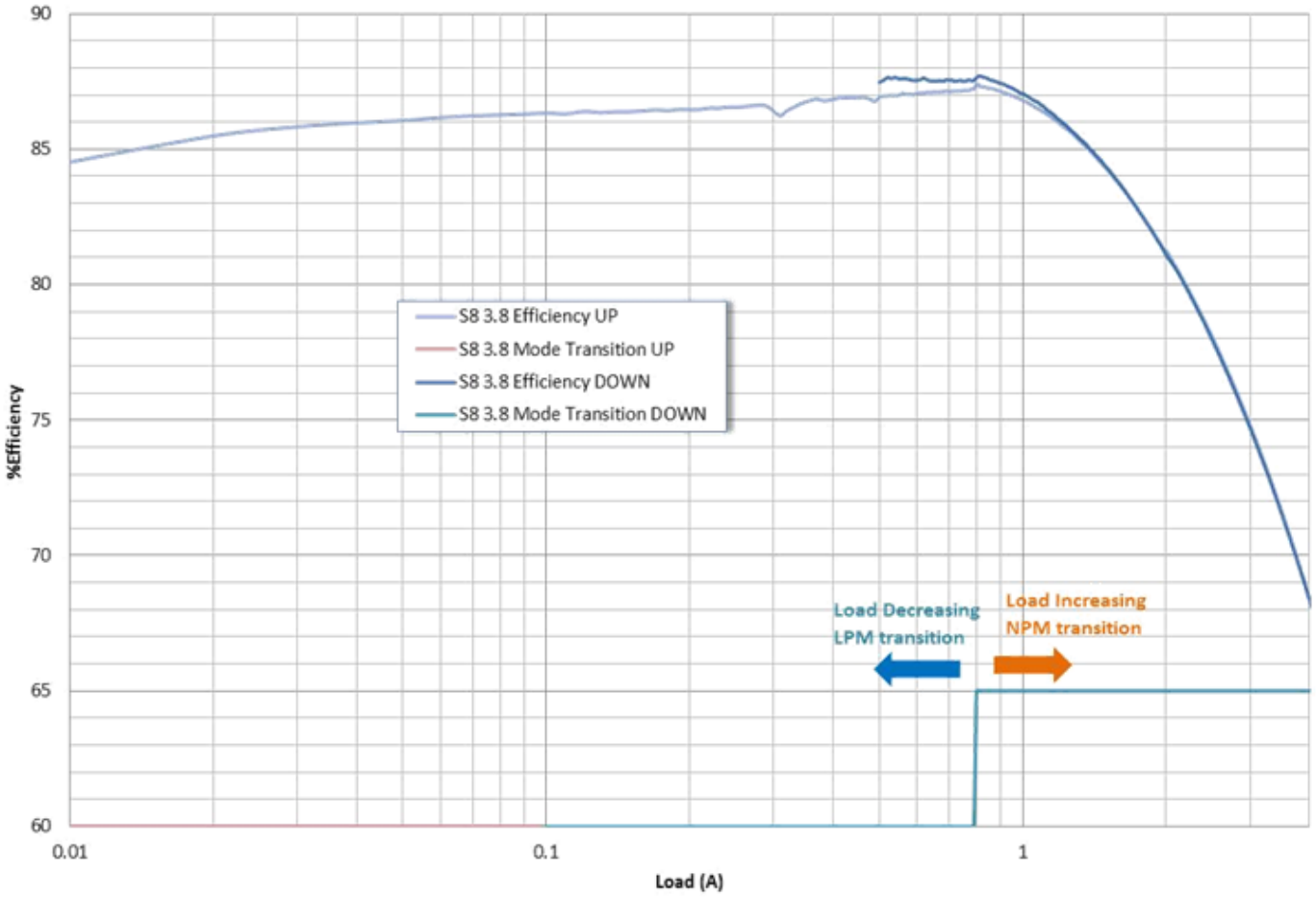


Figure 3-7 PM8994/PM8996 S8 efficiency plot (VBAT = 3.8 V and Vout = 1 V)

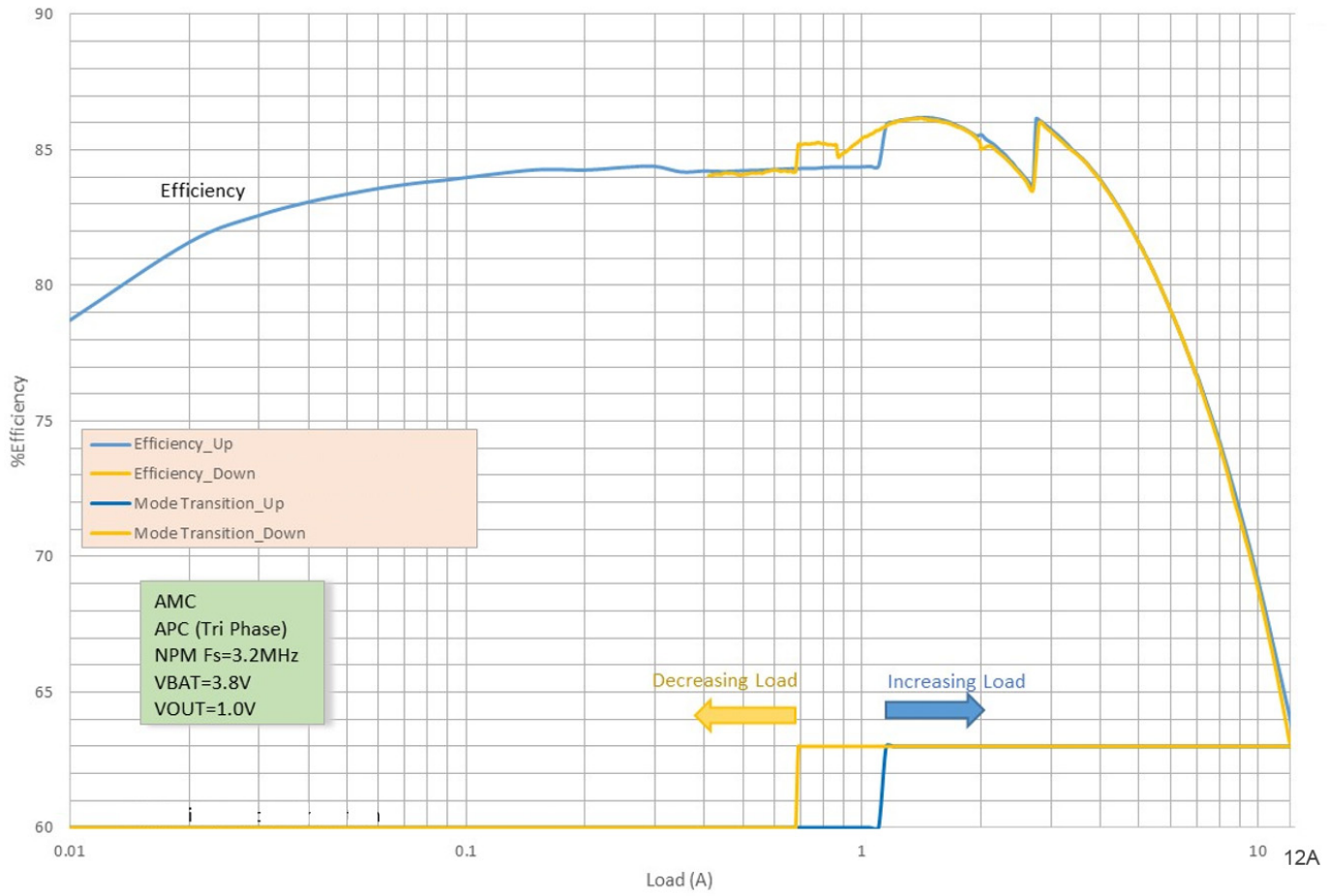


Figure 3-8 PM8994/PM8996 tri-phase S9/S10/S11 efficiency plot (VBAT = 3.8 V and Vout = 1 V)

3.6.4 Linear regulators

Thirty-two low dropout linear regulator designs are implemented within the PMIC:

- NMOS rated for 1200 mA (N1200)
- PMOS rated for 600 mA (P600)
- NMOS rated for 300 mA (N300)
- PMOS rated for 300 mA (P300)
- PMOS rated for 150 mA (P150)
- PMOS rated for 50 mA (P50)
- PMOS for on-chip clock circuits (VREG_L5 for RF_CLK buffers and VREG_L7 for XO circuits)
  - Since these two LDOs are not used off-chip, most of their performance specifications are not published.
  - Each has a no-load ground current of 80 µA maximum.

All other LDO performance specifications are presented in Table 3-12.

Table 3-12 LDO performance specifications

Parameter	Comments [7]	Min	Typ	Max	Units
Output voltage ranges					
Programmable range					
All NMOS	12.5 mV steps	0.750	–	1.5375	V
All PMOS	25 mV steps from 0.75–1.525 V; 50 mV steps from 1.50–4.90 V	1.500	–	4.900	V
Rated load current (I_rated), normal [1]	Continuous current delivery				
N1200		–	–	1200	mA
P600		–	–	600	mA
N300		–	–	300	mA
P300		–	–	300	mA
P150		–	–	150	mA
P50		–	–	50	mA
Rated load current, low-power mode [1]	Continuous current delivery				
All LDOs except N1200 and P50 types		–	–	10	mA
N1200		–	–	100	mA
P50		–	–	5	mA
Pass FET power dissipation	–	–	–	600	mW
Overall error at default voltage (includes DC voltage error, load and line regulations and errors due to temperature and process)					
Normal mode	NMOS and PMOS	-2	–	+2	%
Low-power mode	NMOS and PMOS	-4	–	+4	%
Overall error at non-default voltages (includes DC voltage error, load and line regulations and errors due to temperature and process)					
Normal mode		-3	–	+3	%
Low-power mode	NMOS and PMOS	-5	–	5	%
Temperature coefficient	–	-100	–	+100	ppm/°C
Transient settling time [2]	To within 1% of final value	20	100	200	µs
Transient overshoot/undershoot [2]					
Normal mode					
N1200	0.25 × I_rated to 0.75·I_rated load step	-4	–	+4	%
All PMOS LDOs	0.01 × I_rated to I_rated load step	-50	–	+70	mV
N300	0.01 × I_rated to I_rated load step	-3	–	+3	%
Low-power mode (all LDOs)	Same load steps as listed above	-3	–	+3	%
Dropout voltage [3, 4]	Both operating modes				
N1200 and N600		–	–	60	mV
All other LDOs		–	–	300	mV

Table 3-12 LDO performance specifications (cont.)

Parameter	Comments [7]	Min	Typ	Max	Units
Load regulation	V_in > V_out + 0.5 V; 0.01 × I_rated to I_rated				
Normal mode		–	–	0.3	%
Low-power mode		–	–	1.5	%
Line regulation [5]	–				
Normal mode		–	–	0.1	%/V
Low-power mode		–	–	0.5	%/V
Power-supply ripple rejection	PSRR				
Normal mode					
50 Hz–1 kHz		–	60	–	dB
1–10 kHz		–	50	–	dB
10–100 kHz		–	40	–	dB
100 kHz–1 MHz [6]	All LDOs except N1200 and N600	–	35	–	dB
	N1200 and N600	–	20	–	dB
Low-power mode					
50 Hz–1 kHz		–	40	–	dB
1–100 kHz	All LDOs except N1200 and N600	–	30	–	dB
	N1200 and N600	–	20	–	dB
Short-circuit current limiting	Normal mode				
N1200		1300	1800	2600	mA
N600		1000	1500	2000	mA
All PMOS LDOs	Limit = I_rated × factor listed	1.5	2.5	3.5	–
N300	Limit = I_rated × factor listed	2.0	3.0	4.0	–
Soft current limit during start up	Current above I_rated	–	–	100	mA

Table 3-12 LDO performance specifications (cont.)

Parameter	Comments [7]	Min	Typ	Max	Units
Ground current	–				
Normal mode, no load					
N1200		–	200	220	µA
N600		–	75	100	µA
P600		–	90	300	µA
P300		–	65	150	µA
N300		–	100	150	µA
P150		–	55	100	µA
P50		–	45	100	µA
Low-power mode, no load					
N1200		–	26	30	µA
N600		–	15	22	µA
All PMOS LDOs		–	5	6	µA
N300		–	12	15	µA
With load, either mode					
All PMOS and NMOS LDOs		–	–	0.5	%
Bypass mode					
All NMOS LDOs		–	8	10	µA
All PMOS LDOs		–	–	1	µA
Bypass mode on-resistance					
N1200		–	12	20	mΩ
N600		–	28	40	mΩ
N300		–	–	1	Ω
P50		–	3.3	5	Ω
P150		–	1.1	1.7	Ω
P300		–	0.55	0.83	Ω
P600		–	0.28	0.42	Ω
Pull-down current	–	–	20	–	mA

1. Rated current is the current at which all specifications are met. Higher currents are allowed during normal operation, but more headroom will be needed to maintain performance. The low-power mode's current rating should not be exceeded; if so, switch to the normal mode.
2. The stated transient response performance is achieved regardless of the transitory mode – turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.
3. LDO voltage dropout measurement:
   – Program the LDO for its intended operating voltage (V_set_d).
   – Measure the output voltage; call this value V_set_m.
   – Adjust the load such that the LDO delivers its rated output current (I_rated).
   – Adjust the input voltage until V_in = V_set_m + 0.5 V.
   – Decrease V_in until V_out drops 100 mV (until V_out = V_set_m – 0.1 V); call the resulting input value V_in_do and call this output value V_out_do.
   – The voltage drop across the regulator under this condition is the dropout voltage (V_do = V_in_do – V_out_do).
   – The LDO can bypass mode where the output could potentially be lower than its input voltage. The input voltage to the LDO should be greater than 1 V when in the bypass mode.

4. The dropout voltage is specified at full rated current of the LDO. The voltage headroom required to maintain the LDO in regulation depends on the load current of the LDO. The current that an LDO can provide needs to be derated based on the headroom. For example, the 600 mA PMOS LDO has a dropout voltage of 300 mV. When headroom is 150 mV, the PMOS LDO can provide 600 * (150/300) = 300 mA current without going out of regulation.
5. Line regulation is the output variation due to a changing input voltage, calculated as the output voltage change in percent divided by the input voltage change. The input voltage changes are:
   – From 1.10–1.80 V for N1200 LDOs
   – From 3.35–4.35 V for PMOS LDOs
   – From 1.80–2.80 V for N300 and N600 LDOs
6. 100 kHz–1 MHz data is based on simulations only.
7. All specifications apply over the device's operating conditions, load current range, and capacitor ESR range, unless noted otherwise.

3.6.5 Voltage switches

The PM8994/PM8996 device has two low-voltage switches. Switch performance specifications are listed in Table 3-13.

Table 3-13 Voltage switch performance specifications

Parameter	Comments	Min	Typ	Max	Units
Low-voltage switches (LVS)					
Input voltage range	–	1.200	–	1.875	V
Rated current (I_rated)	–	–	100 or 300	–	mA
Slew rate (switch output node)	–	–	–	100	mV/µs
Switch output ready	Soft start plus gate full enhancement	100	300	1200	µs
Overcurrent threshold	Threshold = I_rated x factor listed	1.3	1.5	2.6	–
On resistance (pad-to-pad)	LVS1 (300 mA) LVS2 (100 mA)	–	–	0.15 0.45	Ω Ω
Ground current Sleep mode Normal mode, no load	Switch on, support functions disabled	 – –	 – –	 1 40	 µA µA
Pull-down discharge time	Switch turned off	–	0.5	2	ms
Maximum load capacitance	–	–	–	1	µF

3.6.6 Internal voltage-regulator connections

Some regulator supply voltages and/or outputs are connected internally to power other PMIC circuits. These circuits will not operate properly unless their supplies are correct; this requires:

1. Certain regulator supply voltages must be delivered at the right value.
2. Corresponding regulator sources must be enabled and set to the proper voltages.

These requirements are summarized in Table 3-14.

Table 3-14 Internal voltage regulator connections

Feature	Regulator	Default	Notes
GPIO and MPP	VREG_L12	1.8 V	–
	VREG_S4	1.8 V	–
	VREG_L19	2.8 V	Only MPP[5:8]
	VPH_PWR	3.6 V	–
Clocks	VDD_APQ_IO	1.8 V	Sleep clock pad (VIO)
	VREG_XO	1.8 V	XO core
	VREG_RF_CLK	1.8 V	–
	VREG_L12 [1]	1.8 V	Low-power output buffers (BBCLK)
Poweron	VDD_APQ_IO	1.8 V	PON_RESET_N and I/O (VIO)
SPMI	VDD_APQ_IO	1.8 V	SPMI pad (VIO)
AMUX XO/HKADC supply	VREG_L8	1.8 V	–

1. BBCLK buffer supply L12 is forced on by BBCLKx_EN

3.7 General housekeeping

The PMIC includes many circuits that support handset-level housekeeping functions – various tasks that must be performed to keep the handset in order. Integration of these functions reduces the external parts count and the associated size and cost. Housekeeping functions include an analog switch matrix, multiplexers, and voltage scaling; an HK/XO ADC circuit; system clock circuits; a real-time clock for time and alarm functions; and over-temperature protection.

3.7.1 Analog multiplexer and scaling circuits

A set of analog switches, analog multiplexers, and voltage-scaling circuits select and condition a single analog signal for routing to the on-chip HK/XO ADC. The multiplexer and scaling functions are summarized in Table 3-15.

Table 3-15 Analog multiplexer and scaling functions

Ch #	Description	Typical input range (V) [4]	Scaling	Typical output range (V)
0 to 3	–	–	–	–
4	AMUX_0 pad (mid V)	0.15 to 3 × (VL8 - 0.05)	1/3	0.15–(VL8 - 0.05)
5	VCOIN pad	2.0–3.25	1/3	0.67–1.08
6	–	–	–	–
7	VPH_PWR pad	2.5–4.75	1/3	0.83–1.50
8	Die-temperature monitor	0.4–0.9	1	0.4–0.9
9	0.625 V reference voltage	0.625	1	0.625
10	1.25 V reference voltage	1.25	1	1.25
11 to 13	–	–	–	–
14, 15 [1]	GND_REF, VDD_ADC	Direct connections to ADC for calibration		
16 to 19	MPP_01 to MPP_04 pads	0.1–1.7	1	0.1–1.7
20 to 23	MPP_05 to MPP_08 pads	0.1–1.7	1	0.1–1.7
24 to 31	–	–	–	–
32 to 35	MPP_01 to MPP_04 pads	0.3–4.5	1/3	0.1–1.7
36 to 39	MPP_05 to MPP_08 pads	0.3–4.5	1/3	0.1–1.7
40 to 49	–	–	–	–
50	XO_THERM pad direct	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
51 to 53	AMUX_1 to AMUX_3 pad	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
54	AMUX_HW_ID pad	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
55, 56	AMUX_4, AMUX_5 pad	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
57	AMUX_0 pad (low V)	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
58	AMUX_PU1 pad	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
59	–	–	–	–
60	XO_THERM through AMUX pad	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
61, 62	–	–	–	–
63	Module power off [2]	–	–	–
114	XO_THERM pad direct [3]	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
115 to 117	AMUX_1 to AMUX_3 pad [3]	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
118	AMUX_HW_ID pad [3]	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
119 to 120	AMUX_4, AMUX_5 pad [3]	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
121	AMUX_0 pad (low V) [3]	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
124	XO_THERM through AMUX pad [3]	0.1–(VL8 - 0.1)	1	0.1–(VL8 - 0.1)
255	Module power off	–	–	–

1. Channels 14 and 15 are for ADC calibration purposes; these signals do not connect to the AMUX input, but rather connect to the ADC input directly.
2. Channel 63 should be selected when the analog multiplexer is not being used; this prevents the scalers from loading the inputs.

3. These AMUX inputs come from off-chip thermistor circuits. The PMIC includes pull up options such that thermistor circuits can share a pull up resistor, thereby reducing the number of external resistors.
4. Input voltage must not exceed the highest of the following supply voltages: VCOIN or VDD. The term VL8 is the VREG_L8 output voltage (connected internally).

NOTE: Gain and offset errors are different through each analog multiplexer channel. Each path should be calibrated individually over its valid gain and offset settings for best accuracy.

Performance specifications pertaining to the analog multiplexer and its associated circuits are listed in Table 3-16.

Table 3-16 Analog multiplexer performance specifications

Parameter	Comments [2]	Min	Typ	Max	Units
Supply voltage (VL8)	Connected internally to VREG_L8	–	1.8	–	V
Output voltage range	–				
Full specification compliance		0.10	–	VL8 – 0.10	V
Degraded accuracy at edges		0.05	–	VL8 – 0.05	V
Input referred offset errors	–				
Channels with × 1 scaling		-2.0	–	+2.0	mV
Channels with 1/3 scaling		-1.5	–	+1.5	mV
Channels with 1/6 scaling		-3.0	–	+3.0	mV
Gain errors, including scaling	Excludes VREG_L8 output error				
Channels with × 1 scaling		-0.20	–	+0.20	%
Channels with 1/3 scaling		-0.15	–	+0.15	%
Channels with 1/6 scaling		-0.30	–	+0.30	%
Integrated nonlinearity (INL)	Input referred to account for scaling	-3	–	+3	mV
Input resistance	Input referred to account for scaling				
Channels with × 1 scaling		10	–	–	MΩ
Channels with 1/3 scaling		1	–	–	MΩ
Channels with 1/6 scaling		0.5	–	–	MΩ
Channel-to-channel isolation	1 V AC input at 1 kHz	50	–	–	dB
Output settling time [1]	C_{load} = 28 pF	–	–	25	µs
Output noise level	f = 1 kHz	–	–	2	µV/Hz [1, 2]

1. The AMUX output and a typical load is modeled in Figure 3-10. After S1 closes, the voltage across C2 settles within the specified settling time.

2. Multiplexer offset error, gain error, and INL are measured as shown in Figure 3-9. Supporting comments:
   - The non-linearity curve is exaggerated for illustrative purposes.
   - Input and output voltages must stay within the ranges stated in Table 3-15; voltages beyond these ranges result in nonlinearity, and are beyond specification.
   - Offset is determined by measuring the slope of the endpoint line (m) and calculating its Y-intercept value (b):
     Offset = b = y_1 - m × x_1
   - Gain error is calculated from the ideal response and the endpoint line as the ratio of their two slopes (in percentage):
     Gain_error = [(slope of endpoint line)/(slope of ideal response) - 1] × 100%
   - INL is the worst-case deviation from the endpoint line. The endpoint line removes the gain and offset errors to isolate nonlinearity:
     INL(min) = min[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]
     INL(max) = max[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]

Table 3-17 AMUX input to ADC output end-to-end accuracy

AMUX Ch #	Function	Typical input range		Auto. scaling	Typical output range		AMUX input to ADC output end-to-end accuracy, RSS [1, 2] (%)				AMUX input to ADC output end-to-end accuracy, WCS [1, 3] (%)				Recommended method of calibration for the channel [4]
							Without calibration		Internal calibration		Without calibration		Internal calibration		
		Min (V)	Max (V)		Min (V)	Max (V)	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	
4	AMUX_0 pad (mid V)	0.3	5.1	1/3	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Ratiometric
5	VCOIN pad	2	3.25	1/3	0.67	1.08	3.1	2.13	0.68	0.51	5.72	4.21	1.41	1.05	Absolute
6	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
7	VPH_PWR pad	2.5	4.5	1/3	0.83	1.5	2.63	1.88	0.59	0.47	5.01	3.76	1.24	0.94	Absolute
8	Die-temperature monitor	0.4	0.9	1	0.4	0.9	4.81	2.49	1	0.57	8.06	4.8	1.98	1.19	Absolute
9	0.625 V reference voltage	0.625	0.625	1	0.625	0.625	3.27	3.27	0.71	0.71	5.95	5.95	1.47	1.47	Absolute – part of calibration
10	1.25 V reference voltage	1.25	1.25	1	1.25	1.25	2.05	2.05	0.5	0.5	4.08	4.08	1.01	1.01	Absolute – part of calibration
14–15	GND_REF, VDD_ADC	Direct connections to ADC for calibration					–	–	–	–	–	–	–	–	–
16–19	MPP_01 to MPP_04 pad	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Absolute or ratiometric depending on application
20–23	MPP_05 to MPP_08 pads	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Absolute or ratiometric depending on application
24–31	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
32–35	MPP_01 to MPP_04 pad	0.3	5.1	1/3	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Absolute or ratiometric, depending on application
36–39	MPP_05 to MPP_08 pad	0.3	5.1	1/3	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Absolute or ratiometric, depending on application
40–49	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
50	XO_THERM pad direct	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Ratiometric
51–53	AMUX_1 to AMUX_3 pad	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Absolute or ratiometric, depending on application

Table 3-17 AMUX input to ADC output end-to-end accuracy (cont.)

AMUX Ch #	Function	Typical input range		Auto. scaling	Typical output range		AMUX input to ADC output end-to-end accuracy, RSS [1, 2] (%)				AMUX input to ADC output end-to-end accuracy, WCS [1, 3] (%)				Recommended method of calibration for the channel [4]
							Without calibration		Internal calibration		Without calibration		Internal calibration		
		Min (V)	Max (V)		Min (V)	Max (V)	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	
54	AMUX_HW_ID pad	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Ratiometric
55–56	AMUX_4, AMUX_5 pad	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Absolute or ratiometric, depending on application
57	AMUX_0 pad (low V)	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Ratiometric
58	AMUX_PU1 pad	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Ratiometric
59	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
60	XO_THERM pad through AMUX	0.1	1.7	1	0.1	1.7	18.42	1.79	3.66	0.46	25.64	3.58	6.22	0.9	Ratiometric
61–62	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
63	Module power off	–	–	–	–	–	–	–	–	–	–	–	–	–	–
114	XO_THERM pad direct	–	–	–	–	–	–	–	–	–	–	–	–	–	–
115 to 117	AMUX_1 to AMUX_3 pad 1	–	–	–	–	–	–	–	–	–	–	–	–	–	–
118	AMUX_HW_ID pad 1	–	–	–	–	–	–	–	–	–	–	–	–	–	–
119 to 120	AMUX_4, AMUX_5 pad 1	–	–	–	–	–	–	–	–	–	–	–	–	–	–
121	AMUX_0 pad (low V) 1	–	–	–	–	–	–	–	–	–	–	–	–	–	–
124	XO_THERM through AMUX pad 1	–	–	–	–	–	–	–	–	–	–	–	–	–	–

1. The minimum and maximum accuracy values correspond to the minimum and maximum input voltage to the AMUX channel.
2. Accuracy based on root sum square (RSS) of the individual errors.
3. Accuracy is based on worst-case straight sum (WCS) of all errors.
4. Absolute uses 0.625 V and 1.25 V MBG voltage reference as calibration points. Ratiometric uses the GND_XO and VREF_XO_THM as the calibration points.

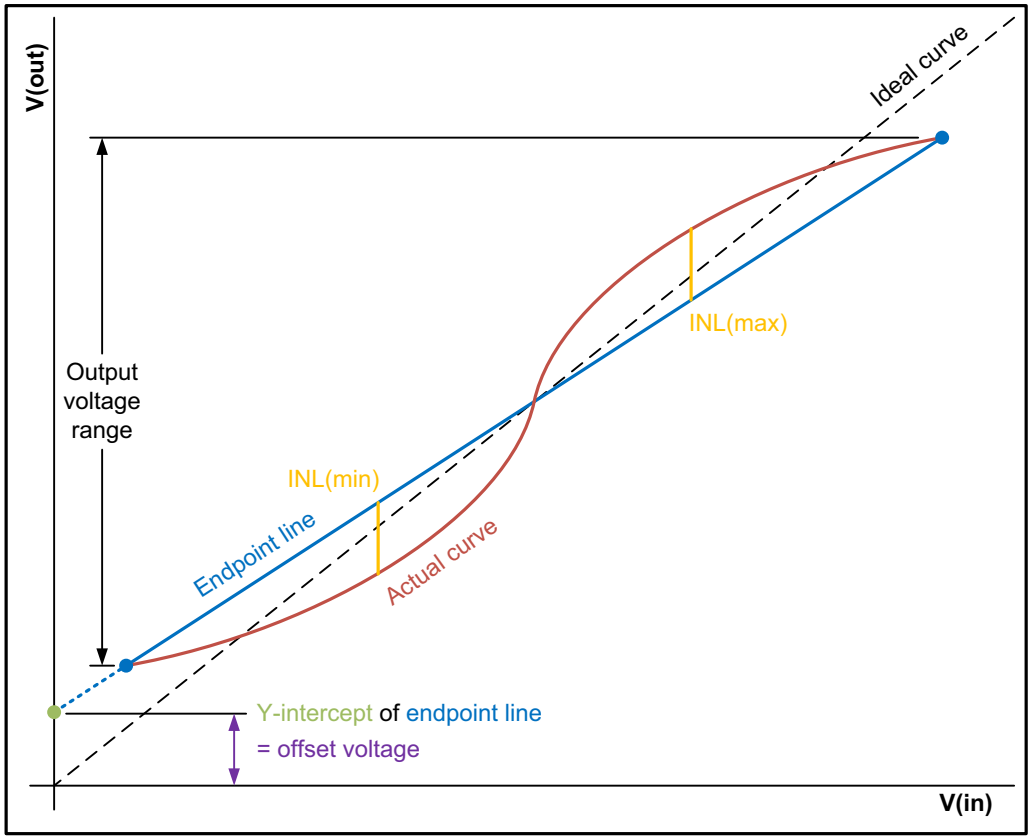


Figure 3-9 Multiplexer offset and gain errors

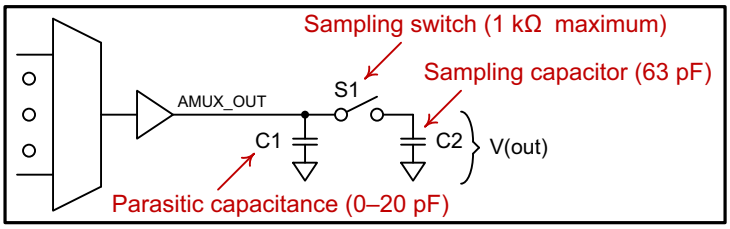


Figure 3-10 Analog multiplexer load condition for settling time specification

3.7.2 HK/XO ADC circuit

The analog-to-digital converter circuit is shared by the housekeeping (HK) and 19.2 MHz crystal oscillator (XO) functions. A 2:1 analog multiplexer selects which source is applied to the ADC:

- The HK source – the analog multiplexer output discussed in Section 3.7.1; or
- The XO source – the thermistor network output that estimates the 19.2 MHz crystal temperature

HK/XO ADC performance specifications are listed in Table 3-18.

Table 3-18 HK/XO ADC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage	Connected internally to VREG_L8	–	1.8	–	V
Resolution	–	–	–	15	bits
Analog-input bandwidth	–	–	100	–	kHz
Sample rate	XO/8	–	2.4	–	MHz
Offset error	Relative to full-scale	-1	–	+1	%
Gain error	Relative to full-scale	-1	–	+1	%
INL	15-bit output	-8	–	+8	LSB
DNL	15-bit output	-4	–	+4	LSB

3.7.3 System clocks

The PMIC includes several clock circuits whose outputs are used for general housekeeping functions, and elsewhere within the handset system. These circuits include a 19.2 MHz XO with multiple controllers and buffers, an MP3 clock output, an RC oscillator, and sleep-clock outputs. Performance specifications for these functions are presented in the following subsections.

3.7.3.1 19.2 MHz XO circuits

An external crystal is supplemented by on-chip circuits to generate the intended 19.2 MHz reference signal. Using an external thermistor network, the on-chip ADC, and advanced temperature compensation software, the PMIC eliminates the large and expensive VCTCXO module required by previous-generation chipsets. The XO circuits initialize and maintain valid pulse waveforms, and measure time intervals for higher-level handset functions. Multiple controllers manage the XO warmup and signal buffering, and generate the intended clock outputs (all derived from one source):

- Low-power baseband output BB_CLK1 – enabled by a dedicated control pad BB_CLK1_EN; this output is used as the APQ clock signal.
- Low-power baseband output BB_CLK2 – enabled internally or can be enabled via a properly configured GPIO.
- Low-noise baseband output LN_BB_CLK – enabled internally or can be enabled via a properly configured GPIO.

The XTAL_19M_IN and XTAL_19M_OUT pads are incapable of driving a load – the oscillator is significantly disrupted if either pad is externally loaded.

As described in Section 3.7.3.3, an RC oscillator is used to drive some clock circuits until the XO source is established.

The 19.2 MHz XO circuit and related performance specifications are listed in Table 3-19.

Table 3-19 XO controller, buffer, and circuit performance specifications

Parameter	Comments	Min	Typ	Max	Units
XO circuits					
Operating frequency	Set by external crystal	–	19.2	–	MHz
Frequency accuracy after RF calibration	25°C -30 to +85°C	-3 -15	– –	3 15	ppm ppm
Start-up time		–		10	ms
Supply voltage = VREG_XO (VREG_L7)	Input buffer and core XO circuits	–	1.80	–	V
XTAL_19M_IN/XTAL_19M_OUT voltage	A high-impedance or differential probe is required to accurately measure the XTAL_19M_IN and XTAL_19M_OUT voltages	0.6	–	1.8	Vpp
Divided down XO clock outputs: DIV_CLKx					
Buffer output impedance	–				
at low GPIO drive strength		30	42	64	Ω
at medium GPIO drive strength		21	30	44	Ω
at high GPIO drive strength		17	22	35	Ω
Phase noise	–	–		–	
at 100 Hz			-85		dBc/Hz
at 1 kHz			-95		dBc/Hz
at 10 kHz			-100		dBc/Hz
at 100 kHz			-105		dBc/Hz
at 250 kHz			-105		dBc/Hz
at 500 kHz			-105		dBc/Hz

3.7.3.2 MP3 clock

GPIOs can be configured as a 2.4 MHz clock output to support MP3 in a low-power mode. This clock is a divided-down version of the 19.2 MHz XO signal, so its most critical performance features are defined within the XO table (Table 3-19). Output characteristics (voltage levels, drive strength, etc.) are defined in Section 3.4.

3.7.3.3 RC oscillator

The PMIC includes an on-chip RC oscillator that is used during start up, and as a backup to other oscillators. Pertinent performance specifications are listed in Table 3-20.

Table 3-20 RC oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Oscillation frequency	–	14	19.2	24	MHz
Duty cycle	–	30	50	70	%
Divider in SLEEP_CLK path	–	–	586	–	–
Power-supply current	–	–	–	80	µA

3.7.3.4 Sleep clock

The sleep clock is generated one of three ways:

- Using the 19.2 MHz XO circuit and dividing its output by 586 to create a 32.7645 kHz signal. This signal is used as the start-up sleep clock, and as a backup if source 1 or 2 fails.
- Using the on-chip 19.2 MHz RC oscillator instead of the XO signal. This results in a much less accurate and less stable 32.7645 kHz signal that is used for backup only; it is never used in normal modes.

Table 3-21 Sleep clock performance specifications

Parameter	Comments	Min	Typ	Max	Units
Period jitter (RMS)	XO/586 source; as defined in JDSE6	–	–	10	ns
Duty cycle	XO/586 source	–	50	–	%
Tolerance	XO/586 source	-12	–	+12	ppm

Related specifications presented elsewhere include:

- 19.2 MHz XO circuits (Section 3.7.3.1)
- 19.2 MHz RC oscillator (Section 3.7.3.3)
- Output characteristics (voltage levels, drive strength, etc.), as defined in Section 3.4

3.7.4 Real-time clock

The real-time clock (RTC) functions are implemented by a 32-bit real-time counter and one 32-bit alarm; both are configurable in one-second increments. The primary input to the RTC circuits is the selected sleep-clock source (calibrated low-frequency oscillator, or divided-down 19.2 MHz XO). Even when the phone is off, the selected oscillator and RTC continue to run off the main battery.

If the main battery is present, and an SMPL event occurs, RTC contents are corrupted. As power is restored, the RTC pauses and skips a few seconds. The phone must reacquire system time from the network to resume the usual RTC accuracy. Similarly, if the main battery is not present and the voltage at VCOIN drops too much, RTC contents are again corrupted. In either case, the RTC reset interrupt is generated. A different interrupt is generated if the oscillator stops, also causing RTC errors.

If RTC support is needed when battery is removed, a qualified coin-cell or super capacitor is required on VCOIN pad of the PMIC. If only SMPL support is needed when battery is removed, a 47 µF capacitor with at least 10 µF effective capacitance at 3 V is required on VCOIN pad of the PMIC.

Pertinent RTC specifications are listed in Table 3-22.

Table 3-22 RTC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Tuning resolution	With known calibrated source	–	3.05	–	ppm
Tuning range	–	-192	–	+192	ppm
Accuracy					
XO/586 as RTC source	Phone on	–	–	24	ppm
CalRC as RTC source	Phone off, valid battery present	–	–	50	ppm
	Phone off, valid coin cell present [1]			200	ppm

1. Assumes a maximum ESR of coin cell/super capacitor is 1 kΩ. For a maximum ESR of 2 kΩ, the accuracy is 500 ppm.

Table 3-23 Qualified coincell/super capacitor specifications

Parameter	Comments	Min	Typ	Max	Units
Operating temperature	–	-30	25	60	°C
Storage range	–	-30	–	85	°C
Rated voltage	–	3.1	3.2	3.3	V
Effective series resistance (ESR) [1]	–	–	–	2000	Ω
Effective capacitance of super capacitor [2]	0.5 hour runtime	12	–	–	mF
	1 hour runtime	24	–	–	mF

1. Effective series resistance (ESR) is the worst-case ESR of the unit tested at worst case temperate after four years of typical usage. A typical use case is a unit biased constantly with 3.2 V DC voltage at 25°C.
2. With shorter run time expectancy, the effective capacitance requirement can be scaled.

3.7.5 Over-temperature protection (smart thermal control)

The PMIC includes over-temperature protection in stages, depending on the level of urgency as the die temperature rises:

- Stage 0 – normal operating conditions (less than 105°C).

Temperature hysteresis is incorporated, such that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMIC will power up immediately.

3.8 User interfaces

In addition to housekeeping functions, the PMIC also includes these circuits in support of common handset-level user interfaces: two light pulse generators; LED current drivers (and control signals for external current drivers).

3.8.1 Light pulse generators

The PMIC includes a 6-channel light pulse generator (LPG) circuit. Since the LPG function is entirely embedded within the PMIC, performance specifications are not appropriate. The LPG outputs can be used to control external current drivers through up to six GPIOs (discussed in Section 3.8.2).

3.8.2 LPG controllers (digital driver outputs)

Up to six GPIOs can be configured as LPG controllers: LPG channel 1 connects to GPIO_04, LPG2 to GPIO_05, LPG3 to GPIO_07, LPG4 to GPIO_08, LPG5 to GPIO_09, and LPG6 to GPIO_10. Output characteristics (voltage levels, drive strength, etc.) are defined in Section 3.4.

3.8.3 Current drivers

Even MPPs can be configured as current sinks; see Section 3.11 for pertinent specifications.

3.9 IC-level interfaces

The IC-level interfaces include poweron circuits; the SPMI; interrupt managers; and miscellaneous digital I/O functions like level translators, detectors, and controllers. Parameters associated with these IC-level interface functions are specified in the following subsections. GPIO and MPP functions are also considered part of the IC-level interface functional block, but they are specified in their own sections (Section 3.10 and Section 3.11, respectively).

3.9.1 Poweron circuits and the power sequences

Dedicated circuits continuously monitor several events that might trigger a poweron sequence. If any of these events occur, the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled. The PM8994/PM8996 device complements the PMI8994/PMI8996 device to meet the system’s power management needs. The regulators that are included during the initial poweron sequence are determined by the hardware configuration controls (OPT[2:1]), as defined in Section 3.9.2. An example sequence is shown in Figure 3-11, followed by pertinent timing characteristics in Table 3-24.

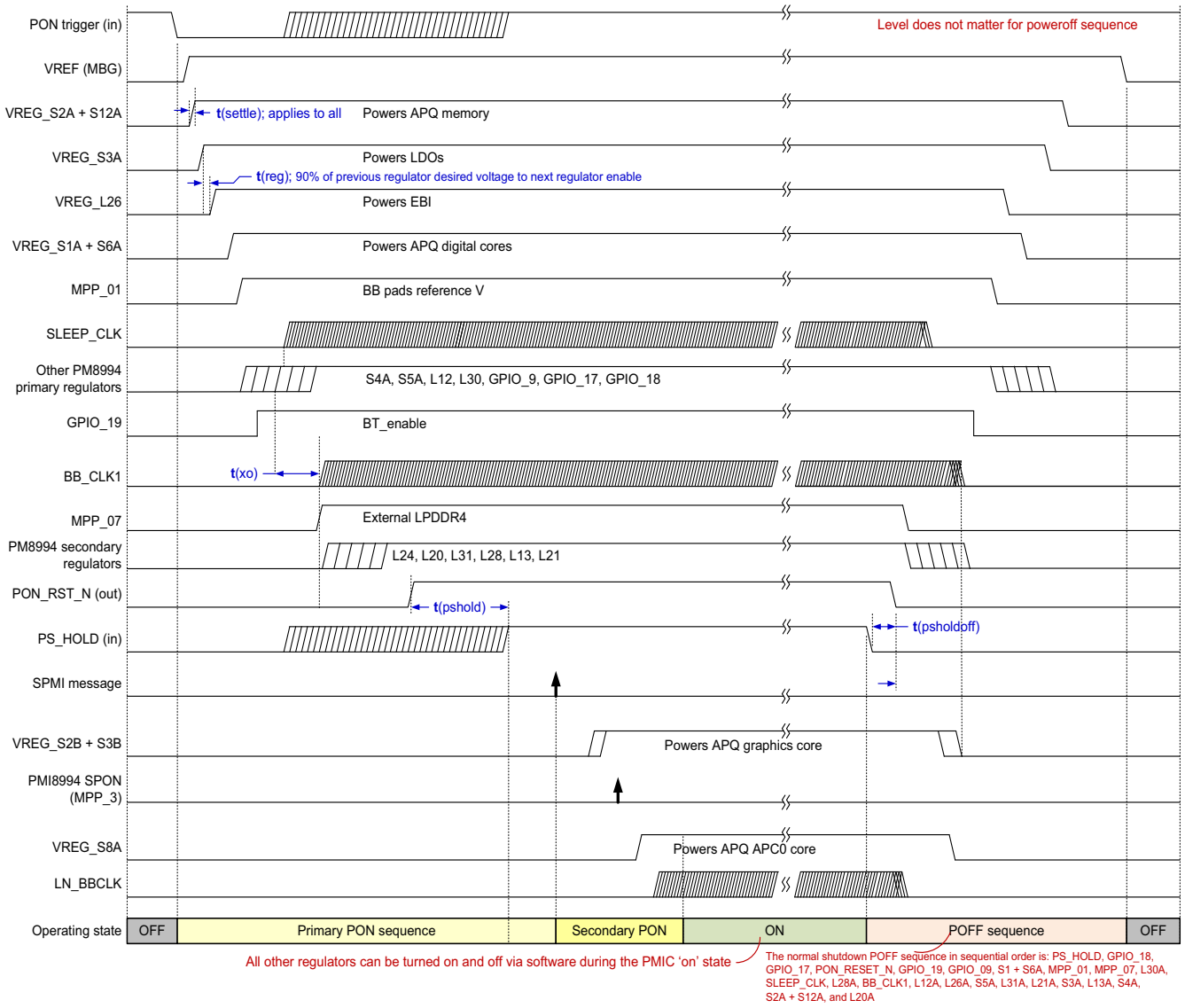


Figure 3-11 Example poweron sequence (APQ8094/APQ8096SGE chipset)

NOTE: The power off sequence is not drawn to scale in Figure 3-11. See the red text at the bottom of the diagram for the correct power off sequence.

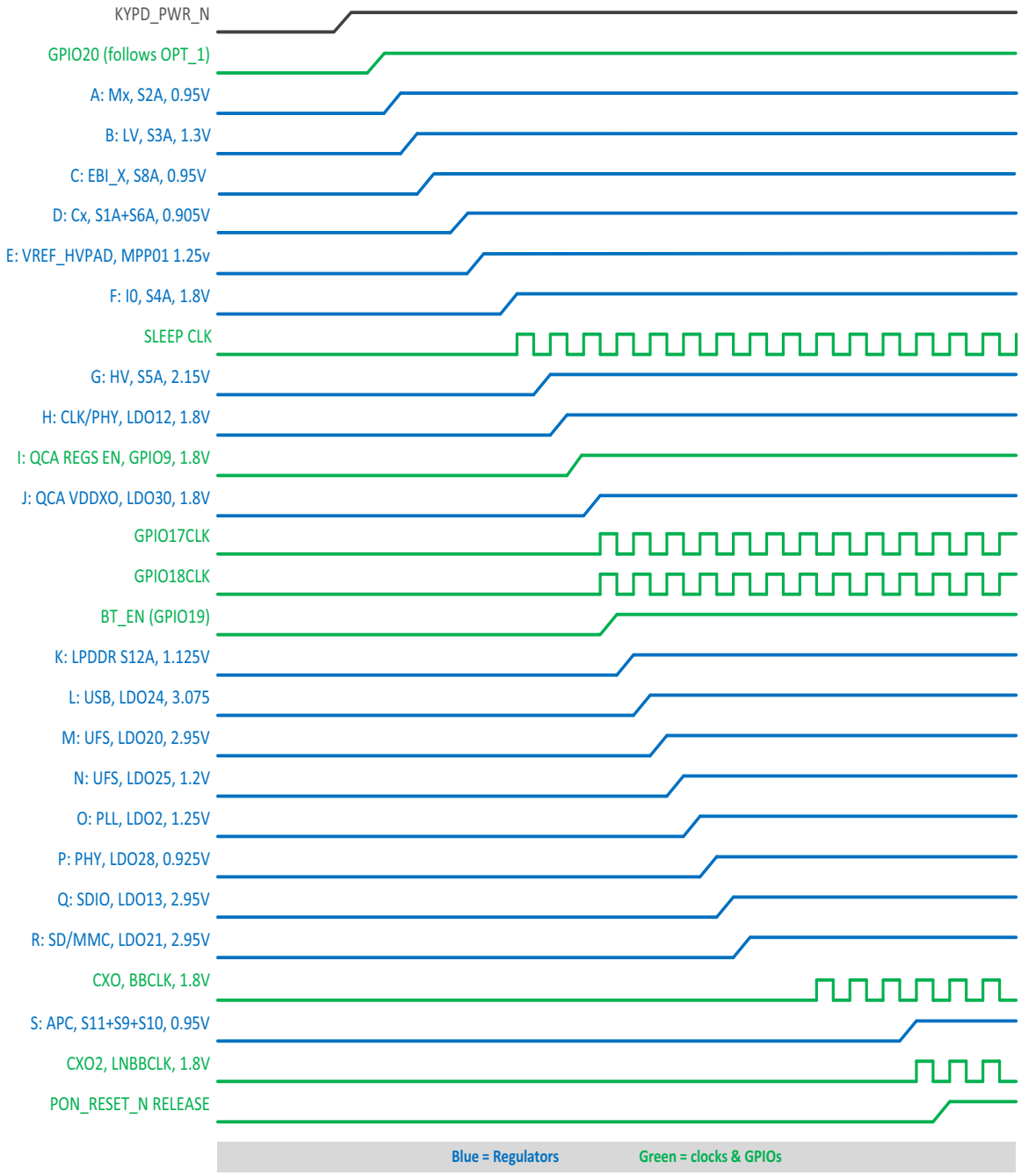


Figure 3-12 Example poweron sequence (APQ8094/APQ8096SGE chipset)

Table 3-24 Poweron timing specifications

Parameter [1]	Comments	Min	Typ	Max	Units
t_{settle} [2]	Regulator settling time	20	–	300	µs
t_{reg} [2, 3]	Inter-regulator turn on time	–	128	–	µs
t_{xo}	XO warm-up time	12	15	18	ms
t_{ps_hold} [4, 5] Default timeout Qualcomm® WiPower™ Wireless Charging Technology timeout	PS_HOLD timeout	 133 665	 200 1000	 240 1200	 ms ms
$t_{ps\_hold\_off}$	Delay from PS_HOLD drop to PON_RESET_N going low	90	–	250	µs
t_{off}	Time between regulator disable signals	200	256	600	µs

1. Timing is derived from the divided-down XO clock source (32.7645 kHz typical); otherwise, its tolerance depends on the RC clock tolerance.
2. Each regulator will settle to within its stated regulator accuracy within the stated regulator settling time. The specified values require the recommended load capacitors. If extra capacitance is used, the settling times can be significantly longer for both t_{settle} and t_{reg}. PM8996's S2B has a longer start-up configuration, with 1.2 msec typical settling time.
3. t_{reg} is measured from 90% of intended voltage out of the previous regulator to the next regulator enable.
4. PS_HOLD timeout is 1 sec during poweron sequence if poweron trigger reason is PON_1 and PON_OPTION_BITS register WIPWR_DEBOUNCE_DLY field is set. PS_HOLD timeout is 200 ms during poweron sequence for other poweron trigger reasons. PS_HOLD timeout is 200 ms for warm reset sequence.
5. PS_HOLD timeout is the time after which the PMIC will turn off, if PS_HOLD is not yet driven high enough by the system device.

The I/Os to/from the poweron circuits are basic digital control signals that must meet the voltage-level requirements stated in Section 3.4. The KPD_PWR_N and CBL_PWR_N inputs are pulled up to an internal voltage (dVdd). Additional poweron-circuit performance specifications are listed in Table 3-24.

3.9.2 OPT[2:1] hardwired controls

Two pads (OPT_2 and OPT_1) must be hardwired to ground or VDD, or be left open (high-impedance state or Hi-Z); this yields nine possible combinations. Table 3-25 lists the parameters that OPT[2:1] pads decide.

Table 3-25 Hardware configuration options

Option pad	Parameter	Configuration
OPT_1	Chipset poweron/off sequence	
GND		Reserved
Hi-Z		Reserved
VDD		
OPT_2	Chipset poweron/off sequence	
GND		Reserved
Hi-Z		Reserved
VDD		

Each chipset that uses the PM8994/PM8996 device must set the OPT pads correctly for their particular application; the APQ8094/APQ8096SGE device-based reference designs use these settings:
OPT_[2:1] = GND, GND.

3.9.3 SPMI and the interrupt managers

The SPMI is a bidirectional, two-line digital interface that meets the voltage and current level requirements stated in Section 3.4.

3.9.4 Undervoltage (UVLO) lockout

The handset supply voltage (VDD) is monitored continuously by a circuit that automatically turns off the device at severely low VDD conditions. UVLO events do not generate interrupts. UVLO-related voltage and timing specifications are listed in Table 3-26.

Table 3-26 UVLO performance specifications

Parameter	Comments	Min	Typ	Max	Units
Rising threshold voltage [1, 2]	Programmable value 50 mV steps	1.675	2.825	3.225	V
Hysteresis [1]	175 mV setting	125	175	225	mV
	300 mV setting	250	300	350	mV
Falling threshold voltage [3]	175 mV hysteresis setting	1.500	2.650	3050	V
	300 mV hysteresis setting	1.375	2.525	2.925	V
	425 mV hysteresis setting	1.200	2.400	2.800	V
UVLO detection interval	–	–	1	–	µs

1. Default UVLO rising threshold is 2.725 V and hysteresis is 175 mV. For handset application, the UVLO rising threshold and hysteresis are reconfigured in SBL to 2.825 V and 425 mV respectively. It is not recommended that customers change the UVLO settings.
2. The minimum time from valid battery or system power applied to initial PON trigger applied is known as the UVLO rising threshold debounce timer which is 16 ms (set in register 0x888 bits <2:0>). Therefore, the VBAT/VPH_PWR must be above the UVLO rising threshold (2.825 V default) for greater than 16 ms before the PMIC will accept the PON trigger.
3. The UVLO rising threshold is programmable. UVLO falling threshold = UVLO rising threshold - UVLO hysteresis. For a default, UVLO rising threshold setting of 2.725 V and hysteresis setting of 175 mV, the UVLO falling threshold is 2.550 V.

3.10 General-purpose input/output specifications

The 22 general-purpose input/output (GPIO) ports are digital I/Os that can be programmed for a variety of configurations (Table 3-27). Performance specifications for the different configurations are included in Section 3.4.

NOTE: Unused GPIO pads should be configured as inputs with 10 µA pull-down.

Table 3-27 Programmable GPIO configurations [1]

Configuration type	Configuration description
Input	1. No pull-up 2. Pull-up (1.5, 30, or 31.5 µA) 3. Pull-down (10 µA) 4. Keeper
Output	Open-drain or CMOS Inverted or non-inverted Programmable drive current; see Table 3-28 for options.
Input/output pair	Requires two GPIOs. Input and output stages can use different power supplies, thereby implementing a level translator. See Table 2-1 for supply options.

1. Available pad voltages are:
   V_G0 = VPH_PWR
   V_G1 = VPH_PWR
   V_G2 = VREG_S4 (1.8 V)
   V_G3 = VREG_L12 (1.8 V)

GPIOs default to digital input with 10 µA pull-down at poweron. Before they can be used for their intended purposes, they need to be configured for use.

GPIOs are designed to run at a 4 MHz rate to support high-speed applications. The supported rate depends on the load capacitance and IR drop requirements. If the application specifies load capacitance, then the maximum rate is determined by the IR drop. If the application does not require a specific IR drop, then the maximum rate can be increased by increasing the supply voltage, and adjusting the drive strength according to the actual load capacitance.

3.11 Multipurpose pad specifications

The PM8994/PM8996 device includes eight multipurpose pads (MPPs), and they can be configured for any of the functions specified within Table 3-28. All MPPs are Hi-Z at poweron. During poweron, PBS programs MPP_01 as analog output which is used as a reference.

Table 3-28 Multipurpose pad performance specifications [1]

Parameter	Comments	Min	Typ	Max	Units
MPP configured as digital input [2]					
Logic high input voltage	–	0.65 × V_M	–	–	V
Logic low input voltage	–	–	–	0.35·V_M	V
MPP configured as digital output [2]					
Logic high output voltage	$I_{out} = I_{OH}$	V_M - 0.45	–	V_M	V
Logic low output voltage	$I_{out} = I_{OL}$	0	–	0.45	V
MPP configured as bidirectional I/O [3]					
Nominal pull up resistance	Programmable range [4]	0.6	–	30	kΩ
Maximum frequency	–	200	–	–	kHz
Switch on resistance	–	–	20	50	Ω
Power-supply current	–	–	6	7	µA
MPP configured as analog input (analog multiplexer input)					
Input current	–	–	–	100	nA
Input capacitance	–	–	–	10	pF
MPP configured as analog output (buffered VREF output)					
Output voltage error	-50 µA to +50 µA	–	–	30	mV
Temperature variation	Due to buffer only; does not include VREF variation (see Table 3-9)	-0.03	–	+0.03	%
Load capacitance	–	–	–	25	pF
Power-supply current	–	–	0.17	0.20	mA
MPP configured as level translator					
Maximum frequency	–	4	–	–	MHz
MPPs configured as current drivers (even MPPs only)					
Power supply voltage	–	–	VDD	–	V
Output current	Programmable in 5 mA increments	5	–	40	mA
Output current accuracy	Any programmed current value	-20	–	+20	%
Dropout voltage	V_IN - V_OUT with I_OUT within the accuracy limits of its current setting	–	–	1000	mV
Leakage current	Driver disabled	–	105	115	nA

1. Available pad voltages are:
   V_M0 = VPH_PWR
   V_M1 = VPH_PWR for MPP_01 to MPP_04, or VREG_L19 for MPP_05 to MPP_08
   V_M2 = VREG_S4 (1.8 V)
   V_M3 = VREG_L12 (1.8 V)
2. Input and output stages can use different power supplies, thereby implementing a level translator. Other specifications are included in Section 3.4.
3. MPP pairs are listed in Table 3-29.
4. Pull-up resistance is programmable to values of 0.6 kΩ, 10 kΩ, 30 kΩ, or open.

NOTE: Only odd MPPs (MPP_01, MPP_03, MPP_05, and MPP_07) can be configured as analog outputs. Only even MPPs (MPP_02, MPP_04, MPP_06, and MPP_08) have current sink capability.

Table 3-29 MPP pairs

MPP # <–> MPP #
1 <–> 2
3 <–> 4
5 <–> 6
7 <–> 8

4 Mechanical information

4.1 Device physical dimensions

The PM8994/PM8996 device is available in the 225 WLNSP that includes ground pads for improved grounding, mechanical strength, and thermal continuity. The 225 WLNSP has a 6.21 mm × 6.16 mm body with a maximum height of 0.55 mm. Pad 1 is located by an indicator mark on the top of the package. A simplified version of the 225 WLNSP outline drawing is shown in Figure 4-1.

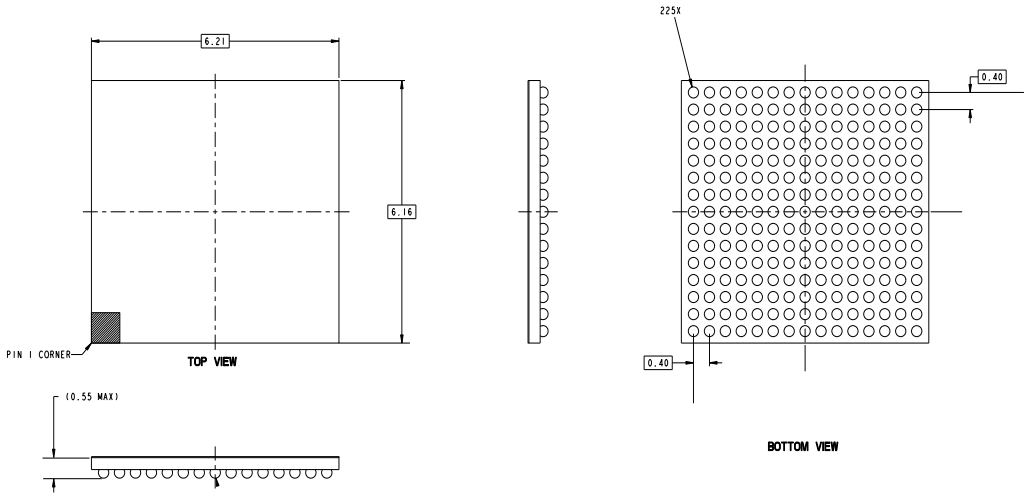


Figure 4-1 225 WLNSP (6.21 × 6.16 × 0.55 mm) package outline drawing

NOTE: This is a simplified outline drawing.

4.2 Part marking

4.2.1 Specification-compliant devices

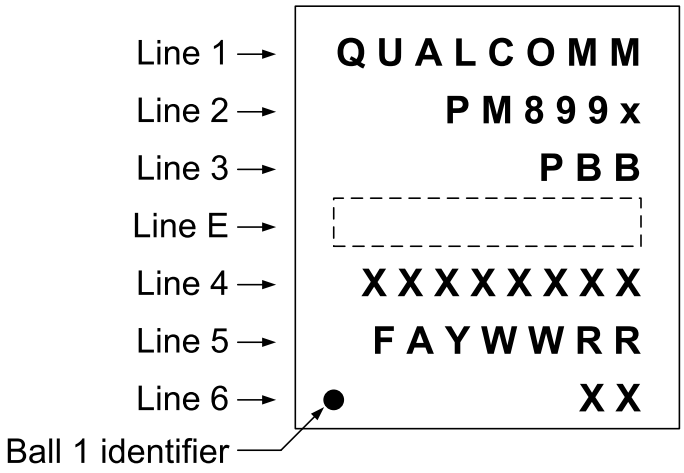


Figure 4-2 PM8994/PM8996 part marking (top view – not to scale)

Table 4-1 Part marking line descriptions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	PM899x	QTI product name ■ x = 4 for PM8994, x = 6 for PM8996
3	PBB	P = product configuration code ■ See Table 4-2 for assigned values. BB = feature code ■ See Table 4-2 for assigned values.
E	Blank or random	Additional content as necessary
4	XXXXXXXXX	XXXXXXXXX = traceability information

Table 4-1 Part marking line descriptions (cont.)

Line	Marking	Description
5	FAYWWRR	F = supply source code ■ F = A for SMIC ■ F = B for GLOBALFOUNDRIES A = assembly site code ■ A = E for ASE, Taiwan ■ A = U for Amkor, China ■ A = M for JCET StatsChipPac, Singapore ■ A = Y for Amkor, Taiwan Y = single digit year code WW = work week (based on calendar year) RR = product revision ■ See Table 4-2 for assigned values
6	• XX	• = ball 1 identifier XX = traceability information

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3 and explained below.

Device ID code ►	AA-AAAA	— P	— CCC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pads	Package type	Shipping package	Product version	Source code	Feature code
Example ►	PM-8994	— 0	— 225	WLNSP	— TR	— 00	— 0	— VV
Example ►	PM-8996	— 0	— 225	WLNSP	— TR	— 00	— 0	— VV
Feature code (BB) may not be included when identifying older devices.								

Figure 4-3 Device identification code

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code details

PM8994/PM8996 variant	P value	RR value	Hardware ID number	S value [3]	BB value [4]
PM8994 CS [1]	0	02	2.0	0	VV
PM8996 CS [2]	0	02	2.0	0	01

1. PM8994 CS parts have the same PRR code. All devices with date code YYWW = 1451 (or later) are of CS quality.
2. PM8996 CS devices are compatible with the new APQ8096SGE power-grid changes for VDD_EBI (VREG_S8A) and VDD_APC (VREG_S9A_S10A_S11A).
3. 'S' is the source configuration code that identifies all of the qualified die-fabrication source combinations available at the time a particular sample type was shipped.
4. 'BB' is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants.

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface-mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-3.

Table 4-3 MSL ratings summary

MSL	Out-of-bag floor life	Comments	PMIC rating [1]
1	Unlimited	≤ 30°C/85% RH	**PM8994/PM8996**
2	1 year	≤ 30°C/60% RH	–
2a	4 weeks	≤ 30°C/60% RH	–
3	168 hours	≤ 30°C/60% RH	–
4	72 hours	≤ 30°C/60% RH	–
5	48 hours	≤ 30°C/60% RH	–
5a	24 hours	≤ 30°C/60% RH	–
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH	–

1. The PM8994/PM8996 device's MSL rating is temporary; it will be updated after qualification.

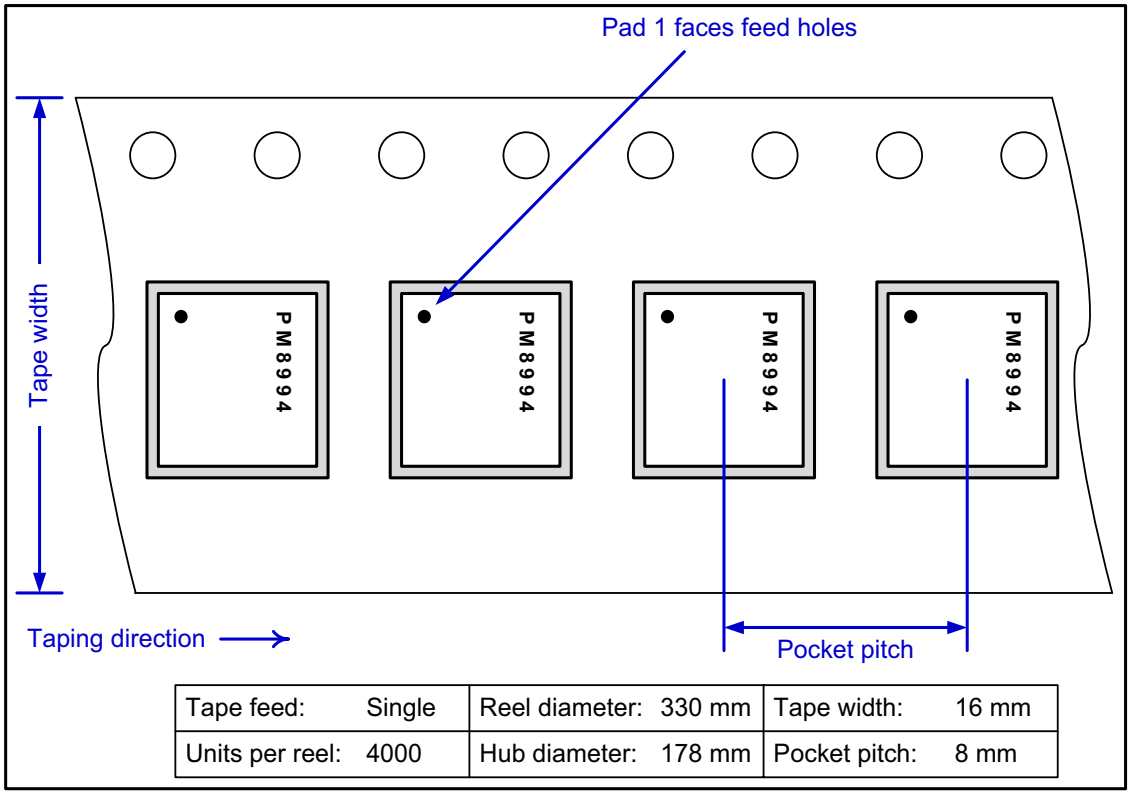
QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PM8994/PM8996 device is classified as MSL1; the qualification temperature was 250ºC.*** This qualification temperature (250°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.3 for more details).

5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards. A simplified sketch of the PM8994/PM8996 device's tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	16 mm
Units per reel:	4000	Hub diameter:	178 mm	Pocket pitch:	8 mm

Figure 5-1 Carrier tape drawing with part orientation (example for PM8994)

NOTE: Figure 5-1 also applies to the PM8996 device.

Tape-handling recommendations are shown in Figure 5-2.

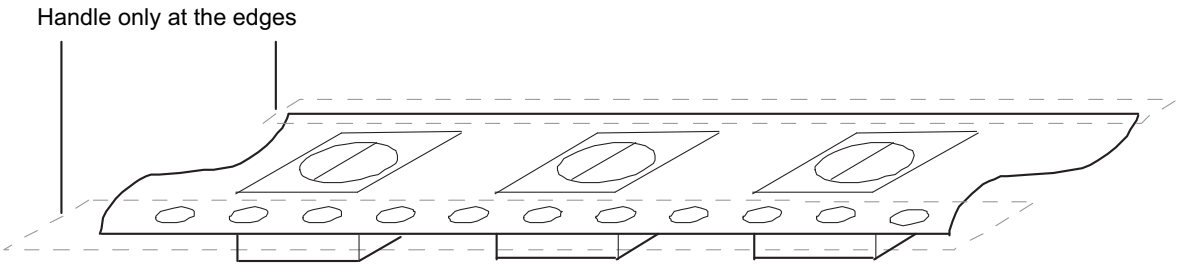


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PM8994/PM8996 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

Wafer-level packages such as the 225 WLNSP should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Section 7.1 for the PM8994/PM8996 device's ESD ratings.

6 PCB mounting guidelines

6.1 RoHS compliance

The device is lead-free and RoHS-compliant. Its Sn/Ag/Cu solder balls use SAC405 composition. QTI defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. QTI package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all QTI IC products are described in the *IC Package Environmental Roadmap* (80-VA832-1).

6.2 SMT parameters

This section describes QTI board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land-pattern and stencil recommendations presented in this section are based on QTI internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

QTI recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land-pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solder-able area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter, to ensure consistent solder-joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). QTI recommends square apertures for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as shown and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil; otherwise, paste deposits may bridge.

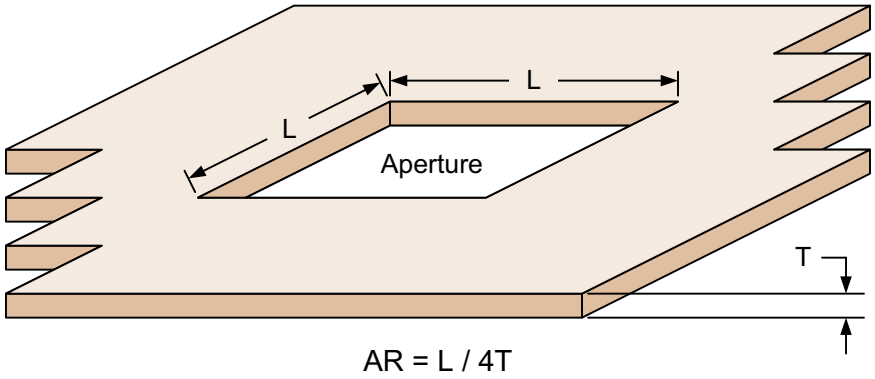


Figure 6-1 Stencil printing aperture area ratio (AR)

Guidelines for an acceptable relationship between L and T are listed below, and are shown in Figure 6-2:

- R = L/4T > 0.65 – best
- 0.60 ≤ R ≤ 0.65 – acceptable
- R < 0.60 – not acceptable

Stencil Aperture L (µm)	Stencil thickness, T (µm)							
	75	80	85	90	95	100	105	110
210	0.70	0.66	0.62	0.58	0.55	0.53	0.50	0.48
220	0.73	0.69	0.65	0.61	0.58	0.55	0.52	0.50
230	0.77	0.72	0.68	0.64	0.61	0.58	0.55	0.52
240	0.80	0.75	0.71	0.67	0.63	0.60	0.57	0.55
250	0.83	0.78	0.74	0.69	0.66	0.63	0..60	0.57
260	0.87	0.81	0.76	0.72	0.68	0.65	0.62	0.59

Figure 6-2 Acceptable solder-paste geometries

QTI provides an example PCB land pattern and stencil design for the 225 WLNSP package.

6.2.2 Reflow profile

Reflow profile conditions typically used by QTI for lead-free systems are listed in Table 6-1, and are shown in Figure 6-3.

Table 6-1 QTI typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/s maximum
Soak	Flux activation	150–190°C	60–75 s
Ramp	Transition to liquidus (solder-paste melting point)	190–220°C	< 30 s
Reflow	Time above liquidus	220–245°C [1]	50–70 s
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/s maximum

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

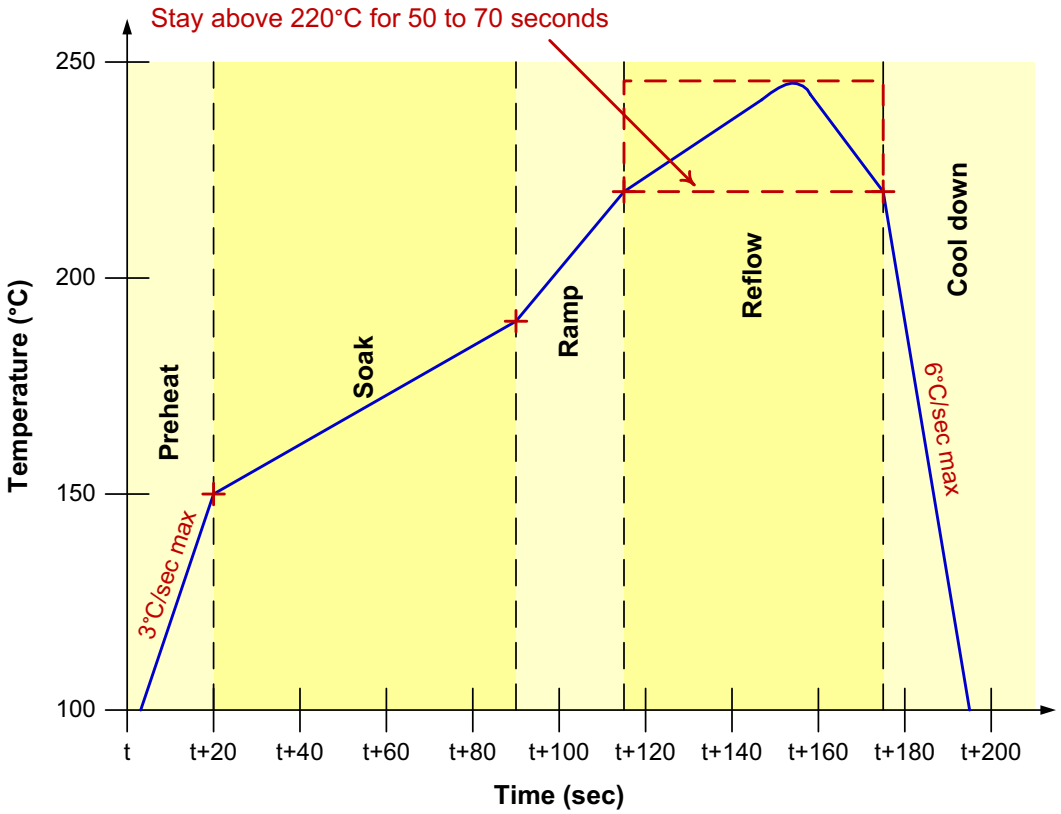


Figure 6-3 QTI typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document, and without explanation, they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

1. Section 4.4 – *Device moisture-sensitivity level*

   PM8994/PM8996 devices are classified as MSL1 at 250°C. The temperature (250°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained in #2 below.

2. Section 7.1 – *Reliability qualifications summary*

   One of the tests conducted for device qualification is the moisture resistance test. QTI follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5 °C (255°C to 260 °C).

3. Section 6.2.2 – *Reflow profile*

   During a production board's reflow process, the temperature seen by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections. However, it must not go so high that the device might be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (250°C or more).

6.2.4 SMT process verification

QTI recommends verification of the SMT process prior to high-volume board assembly, including:

- Inline solder-paste deposition monitoring
- Reflow-profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

7 Part reliability

7.1 Reliability qualifications summary

Table 7-1 Silicon reliability results (SMIC)

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-D Use condition: temperature: 85°C, voltage: 5.0 V Total samples from three different wafer lots	341	DPPM < 1000 [1] Cumulative FITs < 25 FITs [1]
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	341	> 40 [1]
ESD – human-body model (HBM) rating: JESD22-A114-F Total samples from one wafer lot	3	2000 V
ESD – charged-device model (CDM) rating: JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Passed
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: each VDD pad, stress at 1.5 × V_{dd} maximum per device specification; temperature: 85°C; total samples from one wafer lot	6	Passed

1. Cumulative FITs from multiple products under the SMIC-S1, 0.18 µm process.

Table 7-2 Package reliability results (SMIC)

Tests, standards, and conditions	ASE assembly source sample size	ATC assembly source sample size	SCS assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020 Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	480	480	480	Passed
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (cph) **Preconditioning:** JESD22-A113 MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	240	240	240	Passed
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	240	240	240	Passed
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 264 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots at each SAT Data bridge from 224 WLNSP 6.21 × 6.16 mm package	150	150	150	Passed

Table 7-2 Package reliability results (SMIC) (cont.)

Tests, standards, and conditions	ASE assembly source sample size	ATC assembly source sample size	SCS assembly source sample size	Result
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500 and 1000 hours Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	240	240	240	Passed
Flammability **Note**: Flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs are mounted are rated V-0 (better than V-1).	–	–	–	–
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	75	75	75	Passed
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT Data bridge from 224 WLNSP 6.21 × 6.16 mm package	30	30	30	Passed
Internal/external visual Total samples from three different assembly lots at each SAT Data bridge from 224 WLNSP 6.21 × 6.16 mm package	75	75	75	Passed

Table 7-3 Silicon reliability results (GLOBALFOUNDRIES)

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-D Use condition: temperature: 85°C, voltage: 5.0 V Total samples from three different wafer lots	231	DPPM < 1000 [1] Cumulative FITs < 25 FITs [1]
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	231	> 40 [1]
ESD – human-body model (HBM) rating: JESD22-A114-F Total samples from one wafer lot	3	2000 V
ESD – charged-device model (CDM) rating: JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Passed
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: each VDD pad, stress at 1.5 × V_{dd} maximum per device specification; temperature: 85°C; total samples from one wafer lot	6	Passed

1. Cumulative FITs from multiple products under the SMIC-S1, 0.18 µm process.

Table 7-4 Package reliability results (GLOBALFOUNDRIES)

Tests, standards, and conditions	ASE assembly source sample size	ATC assembly source sample size	SCS assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020 Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	480	480	480	Passed
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (cph) **Preconditioning:** JESD22-A113 MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	240	240	240	Passed
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	240	240	240	Passed
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 264 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots at each SAT Data bridge from 224 WLNSP 6.21 × 6.16 mm package	150	150	150	Passed

Table 7-4 Package reliability results (GLOBALFOUNDRIES) (cont.)

Tests, standards, and conditions	ASE assembly source sample size	ATC assembly source sample size	SCS assembly source sample size	Result
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500 and 1000 hours Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	240	240	240	Passed
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs are mounted are rated V-0 (better than V-1).	–	–	–	–
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT Some data bridged from 224 WLNSP 6.21 × 6.16 mm package	75	75	75	Passed
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT Data bridge from 224 WLNSP 6.21 × 6.16 mm package	30	30	30	Passed
Internal/external visual Total samples from three different assembly lots at each SAT Data bridge from 224 WLNSP 6.21 × 6.16 mm package	75	75	75	Passed

7.2 Qualification sample descriptions

Device characteristics

Device name:	PM8994/PM8996
Package type:	225 WLNSP
Package body size:	6.21 mm × 6.16 mm × 0.55 mm
Lead count:	225
Lead composition:	SAC405
Fab process:	0.18 μm CMOS
Fab sites:	SMIC, GLOBALFOUNDRIES
Assembly sites:	ASE, Amkor, and JCET StatsChipPac
Solder ball pitch:	0.4 mm

EXHIBIT 1

PLEASE READ THIS LICENSE AGREEMENT ("AGREEMENT") CAREFULLY. THIS AGREEMENT IS A BINDING LEGAL AGREEMENT ENTERED INTO BY AND BETWEEN YOU (OR IF YOU ARE ENTERING INTO THIS AGREEMENT ON BEHALF OF AN ENTITY, THEN THE ENTITY THAT YOU REPRESENT) AND QUALCOMM TECHNOLOGIES, INC. ("QTI" "WE" "OUR" OR "US"). THIS IS THE AGREEMENT THAT APPLIES TO YOUR USE OF THE DESIGNATED AND/OR ATTACHED DOCUMENTATION AND ANY UPDATES OR IMPROVEMENTS THEREOF (COLLECTIVELY, "MATERIALS"). BY USING, ACCESSING, DOWNLOADING OR COMPLETING THE INSTALLATION OF THE MATERIALS, YOU ARE ACCEPTING THIS AGREEMENT AND YOU AGREE TO BE BOUND BY ITS TERMS AND CONDITIONS. IF YOU DO NOT AGREE TO THESE TERMS, QTI IS UNWILLING TO AND DOES NOT LICENSE THE MATERIALS TO YOU. IF YOU DO NOT AGREE TO THESE TERMS YOU MUST DISCONTINUE AND YOU MAY NOT USE THE MATERIALS OR RETAIN ANY COPIES OF THE MATERIALS. ANY USE OR POSSESSION OF THE MATERIALS BY YOU IS SUBJECT TO THE TERMS AND CONDITIONS SET FORTH IN THIS AGREEMENT.

1.1 License. Subject to the terms and conditions of this Agreement, including, without limitation, the restrictions, conditions, limitations and exclusions set forth in this Agreement, Qualcomm Technologies, Inc. ("QTI") hereby grants to you a nonexclusive, limited license under QTI's copyrights to use the attached Materials; and to reproduce and redistribute a reasonable number of copies of the Materials. You may not use Qualcomm Technologies or its affiliates or subsidiaries name, logo or trademarks; and copyright, trademark, patent and any other notices that appear on the Materials may not be removed or obscured. QTI shall be free to use suggestions, feedback or other information received from You, without obligation of any kind to You. QTI may immediately terminate this Agreement upon your breach. Upon termination of this Agreement, Sections 1.2-4 shall survive.

1.2 Indemnification. You agree to indemnify and hold harmless QTI and its officers, directors, employees and successors and assigns against any and all third party claims, demands, causes of action, losses, liabilities, damages, costs and expenses, incurred by QTI (including but not limited to costs of defense, investigation and reasonable attorney's fees) arising out of, resulting from or related to: (i) any breach of this Agreement by You; and (ii) your acts, omissions, products and services. If requested by QTI, You agree to defend QTI in connection with any third party claims, demands, or causes of action resulting from, arising out of or in connection with any of the foregoing.

1.3 Ownership. QTI (or its licensors) shall retain title and all ownership rights in and to the Materials and all copies thereof, and nothing herein shall be deemed to grant any right to You under any of QTI's or its affiliates' patents. You shall not subject the Materials to any third party license terms (e.g., open source license terms). You shall not use the Materials for the purpose of identifying or providing evidence to support any potential patent infringement claim against QTI, its affiliates, or any of QTI's or QTI's affiliates' suppliers and/or direct or indirect customers. QTI hereby reserves all rights not expressly granted herein.

1.4 **WARRANTY DISCLAIMER**. YOU EXPRESSLY ACKNOWLEDGE AND AGREE THAT THE USE OF THE MATERIALS IS AT YOUR SOLE RISK. THE MATERIALS AND TECHNICAL SUPPORT, IF ANY, ARE PROVIDED "AS IS" AND WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS OR IMPLIED. QTI ITS LICENSORS AND AFFILIATES MAKE NO WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THE MATERIALS OR ANY OTHER INFORMATION OR DOCUMENTATION PROVIDED UNDER THIS AGREEMENT, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR AGAINST INFRINGEMENT, OR ANY EXPRESS OR IMPLIED WARRANTY ARISING OUT OF TRADE USAGE OR OUT OF A COURSE OF DEALING OR COURSE OF PERFORMANCE. NOTHING CONTAINED IN THIS AGREEMENT SHALL BE CONSTRUED AS (I) A WARRANTY OR REPRESENTATION BY QTI, ITS LICENSORS OR AFFILIATES AS TO THE VALIDITY OR SCOPE OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT OR (II) A WARRANTY OR REPRESENTATION BY QTI THAT ANY MANUFACTURE OR USE WILL BE FREE FROM INFRINGEMENT OF PATENTS, COPYRIGHTS OR OTHER INTELLECTUAL PROPERTY RIGHTS OF OTHERS, AND IT SHALL BE THE SOLE RESPONSIBILITY OF YOU TO MAKE SUCH DETERMINATION AS IS NECESSARY WITH RESPECT TO THE ACQUISITION OF LICENSES UNDER PATENTS AND OTHER INTELLECTUAL PROPERTY OF THIRD PARTIES.

1.5 **LIMITATION OF LIABILITY**. IN NO EVENT SHALL QTI, QTI'S AFFILIATES OR ITS LICENSORS BE LIABLE TO YOU FOR ANY INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES, INCLUDING BUT NOT LIMITED TO ANY LOST PROFITS, LOST SAVINGS, OR OTHER INCIDENTAL DAMAGES, ARISING OUT OF THE USE OR INABILITY TO USE, OR THE DELIVERY OR FAILURE TO DELIVER, ANY OF THE MATERIALS, OR ANY BREACH OF ANY OBLIGATION UNDER THIS AGREEMENT, EVEN IF QTI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE FOREGOING LIMITATION OF LIABILITY SHALL REMAIN IN FULL FORCE AND EFFECT REGARDLESS OF WHETHER YOUR REMEDIES HEREUNDER ARE DETERMINED TO HAVE FAILED OF THEIR ESSENTIAL PURPOSE. THE ENTIRE LIABILITY OF QTI, QTI's AFFILIATES AND ITS LICENSORS, AND THE SOLE AND EXCLUSIVE REMEDY OF YOU, FOR ANY CLAIM OR CAUSE OF ACTION ARISING HEREUNDER (WHETHER IN CONTRACT, TORT, OR OTHERWISE) SHALL NOT EXCEED US$10.

2. **COMPLIANCE WITH LAWS; APPLICABLE LAW**.

Any litigation or other dispute resolution between You and Us arising out of or relating to this Agreement, or Your relationship with Us will take place in the Southern District of California, and You and QTI hereby consent to the personal jurisdiction of and exclusive venue in the state and federal courts within that District with respect any such litigation or dispute resolution. This Agreement will be governed by and construed in accordance with the laws of the United States and the State of California, except that body of California law concerning conflicts of law. This Agreement shall not be governed by the United Nations Convention on Contracts for the International Sale of Goods, the application of which is expressly excluded.

3. **CONTRACTING PARTIES**. If the Materials are downloaded on any computer owned by a corporation or other legal entity, then this Agreement is formed by and between QTI and such entity. The individual accepting the terms of this Agreement represents and warrants to QTI that they have the authority to bind such entity to the terms and conditions of this Agreement.

4. **MISCELLANEOUS PROVISIONS**. This Agreement, together with all exhibits attached hereto, which are incorporated herein by this reference, constitutes the entire agreement between QTI and You and supersedes all prior negotiations, representations and agreements between the parties with respect to the subject matter hereof. No addition or modification of this Agreement shall be effective unless made in writing and signed by the respective representatives of QTI and You. The restrictions, limitations, exclusions and conditions set forth in this Agreement shall apply even if QTI or any of its affiliates becomes aware of or fails to act in a manner to address any violation or failure to comply therewith. You hereby acknowledge and agree that the restrictions, limitations, conditions and exclusions imposed in this Agreement on the rights granted in this Agreement are not a derogation of the benefits of such rights. You further acknowledges that, in the absence of such restrictions, limitations, conditions and exclusions, QTI would not have entered into this Agreement with You. Each party shall be responsible for and shall bear its own expenses in connection with this Agreement. If any of the provisions of this Agreement are determined to be invalid, illegal, or otherwise unenforceable, the remaining provisions shall remain in full force and effect. This Agreement is entered into solely in the English language, and if for any reason any other language version is prepared by any party, it shall be solely for convenience and the English version shall govern and control all aspects. If You are located in the province of Quebec, Canada, the following applies: The Parties hereby confirm they have requested this Agreement and all related documents be prepared in English.