

MOS FIELD EFFECT TRANSISTOR 2SK4075

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4075 is N-channel MOS FET designed for high current switching applications.

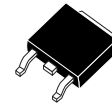
ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4075-ZK-E1-AY	Pure Sn (Tin)	Tape	TO-252 (MP-3ZK)
2SK4075-ZK-E2-AY		2500 p/reel	typ. 0.27 g

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 6.7 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 30 \text{ A)}$
 $R_{DS(on)2} = 10 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 15 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2900 \text{ pF TYP.}$
- Logic level drive type

(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±60	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±180	A
Total Power Dissipation (T _C = 25°C)	P _{T1}	52	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current ^{Note2}	I _{AS}	28	A
Single Avalanche Energy ^{Note2}	E _{AS}	78	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 20 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	R _{th(ch-C)}	2.4	°C/W
Channel to Ambient Thermal Resistance	R _{th(ch-A)}	125	°C/W

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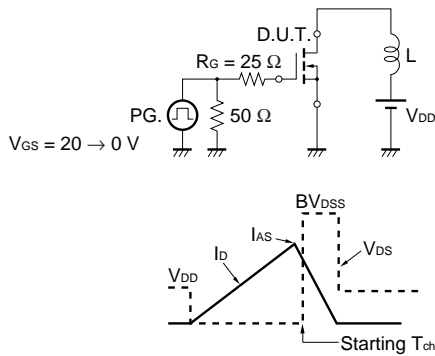
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

<R>

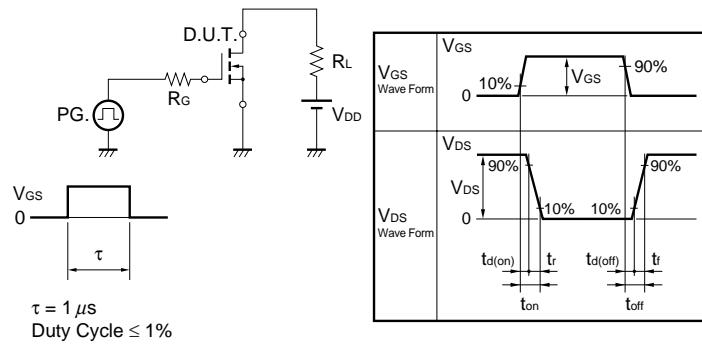
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 15 A	9.3			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 30 A		5.2	6.7	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 15 A		7.2	10	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		2900		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		450		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		293		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V		18		ns
Rise Time	t _r	I _D = 30 A		16		ns
Turn-off Delay Time	t _{d(off)}	V _{GS} = 10 V		54		ns
Fall Time	t _f	R _G = 0 Ω		9		ns
Total Gate Charge	Q _G	V _{DD} = 32 V		54		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		11		nC
Gate to Drain Charge	Q _{GD}	I _D = 60 A		15		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 60 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 60 A, V _{GS} = 0 V		33		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		33		nC

Note Pulsed

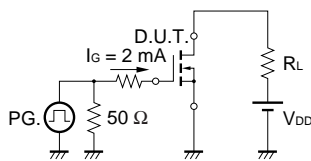
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

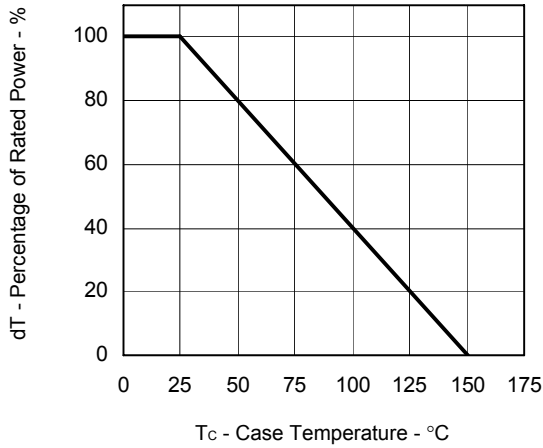


TEST CIRCUIT 3 GATE CHARGE

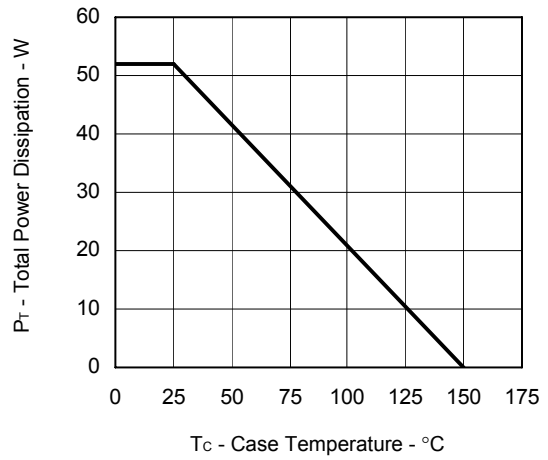


TYPICAL CHARACTERISTICS (T_A = 25°C)

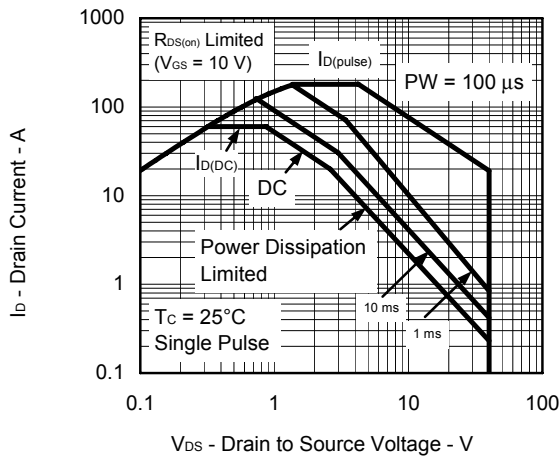
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



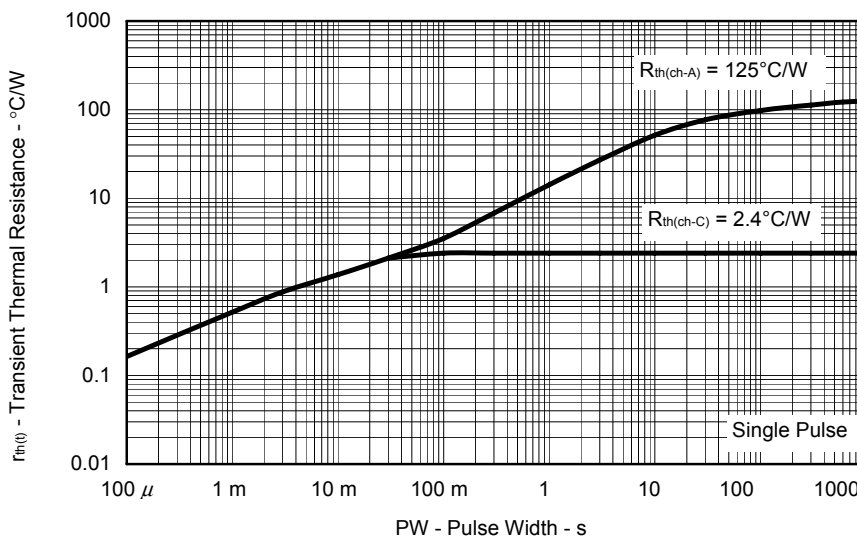
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



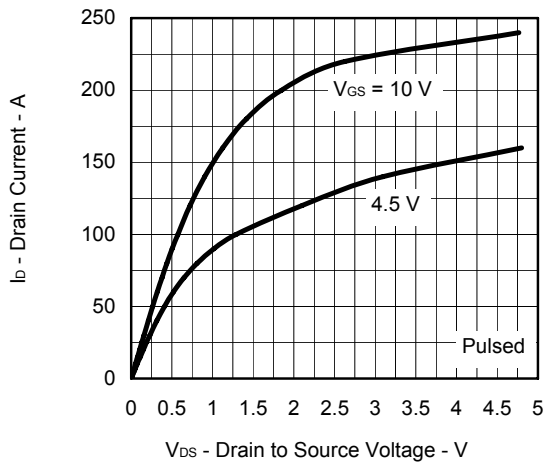
FORWARD BIAS SAFE OPERATING AREA



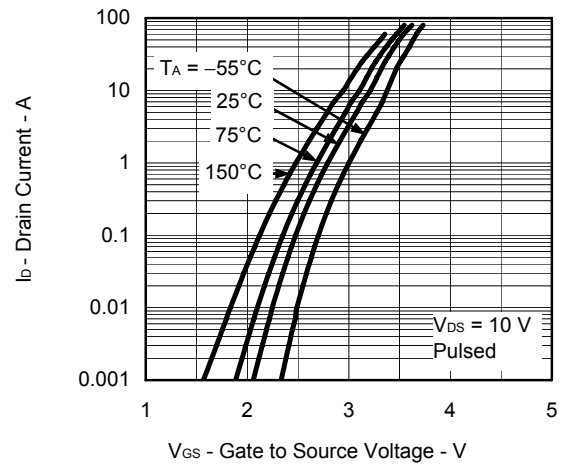
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



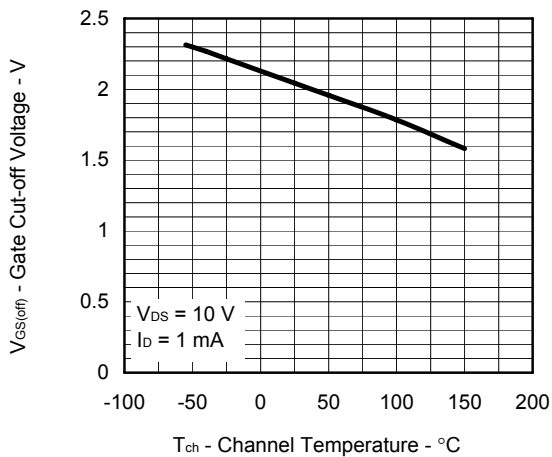
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



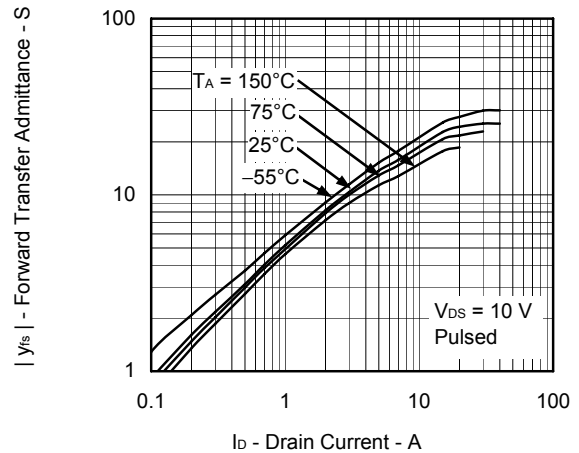
FORWARD TRANSFER CHARACTERISTICS



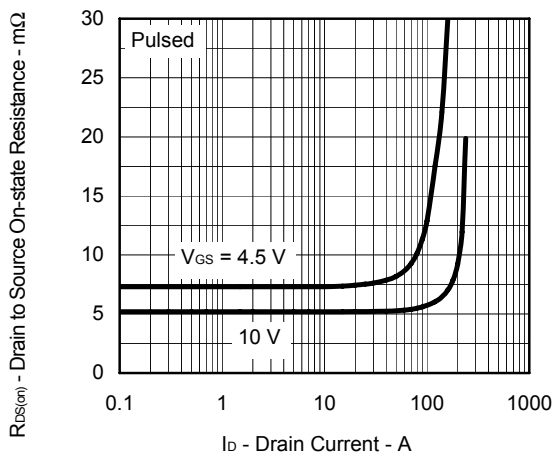
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



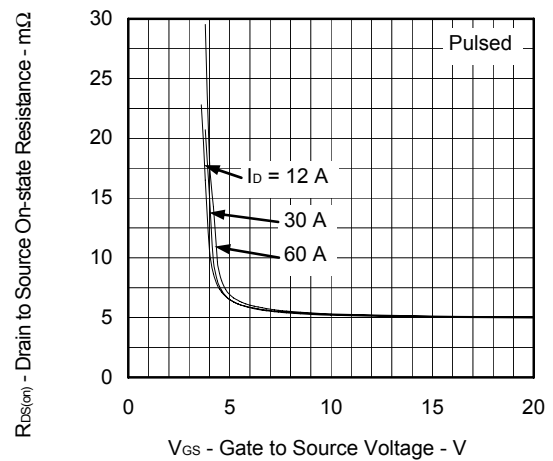
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



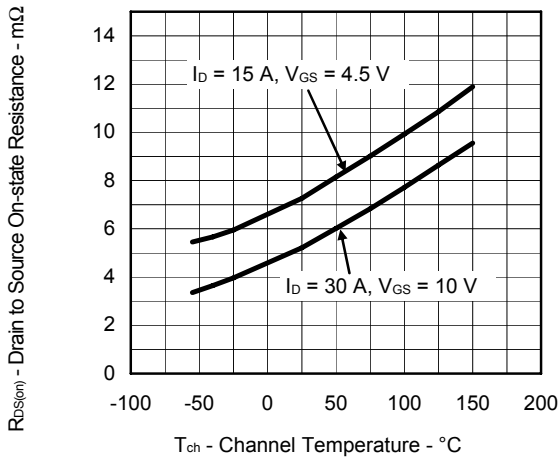
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



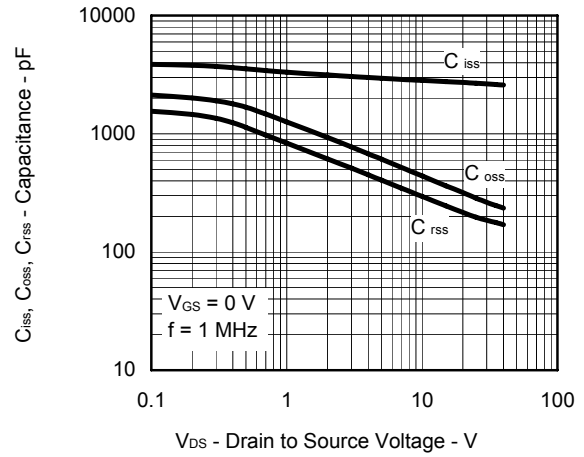
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



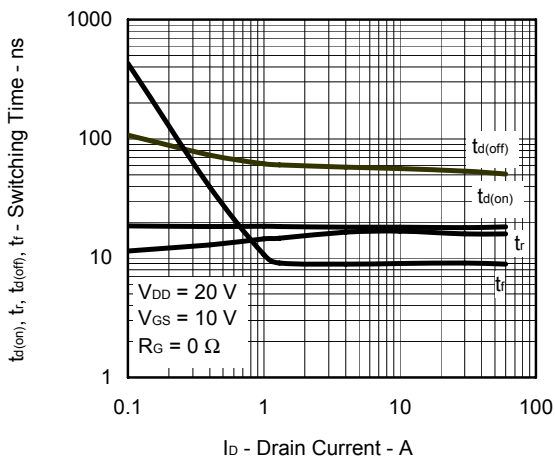
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



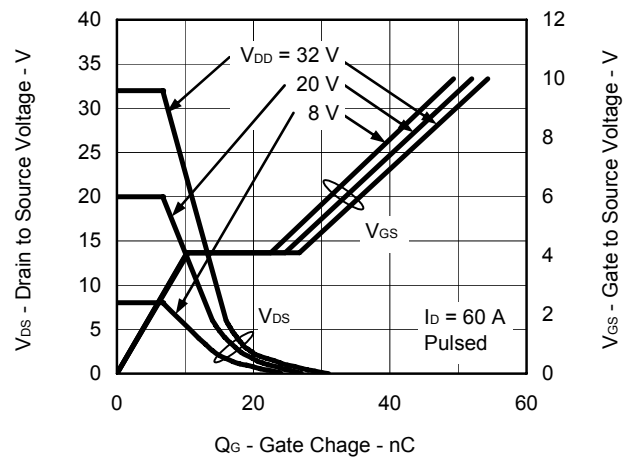
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



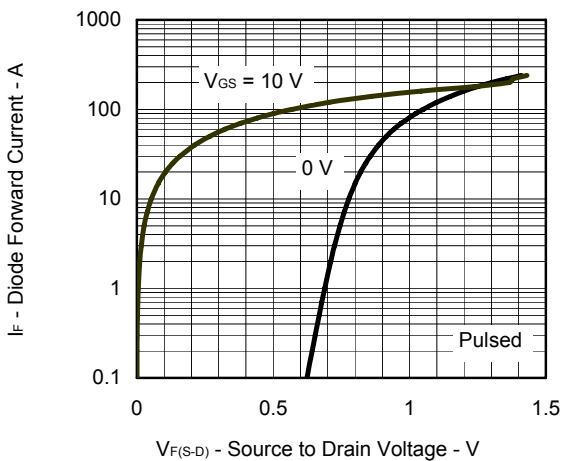
SWITCHING CHARACTERISTICS



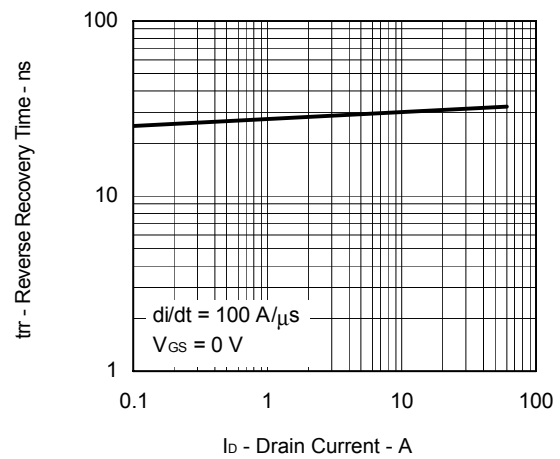
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

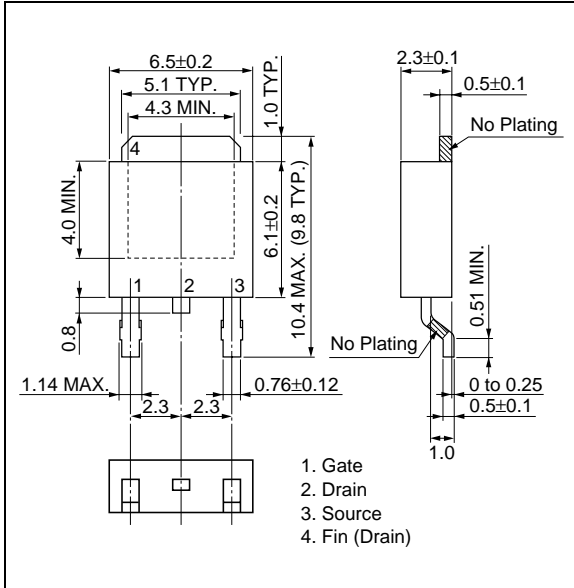


REVERSE RECOVERY TIME vs. DRAIN CURRENT

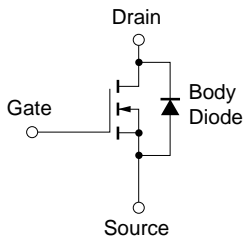


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



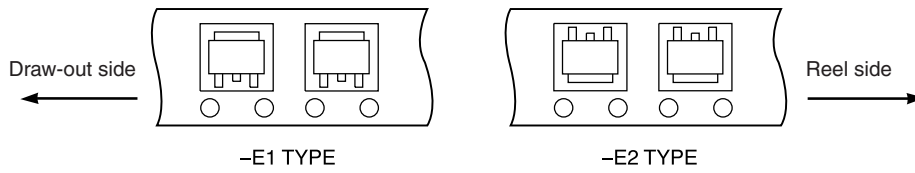
EQUIVALENT CIRCUIT



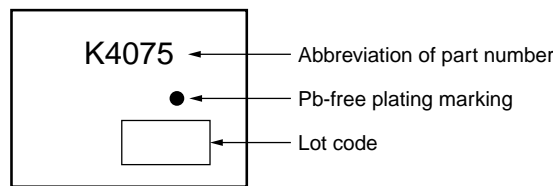
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The 2SK4075 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).

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